

NON-VOLATILE MEMORY USING PYRAMIDAL NANOCRYSTALS AS ELECTRON STORAGE ELEMENTS

TECHNICAL FIELD

[0001] The present disclosure relates generally to the manufacture of semiconductor devices, and more particularly, to the manufacture of integrated circuits having non-volatile memory devices.

BACKGROUND

[0002] Non-volatile memory (NVM) technology has faced challenges in attempting to improve the writing/reading speed and injection efficiency of hot carriers into the tunneling oxide of a memory cell. Non-volatile memory (NVM) devices that utilize a channel hot electron (CHE) injection process are inefficient. This inefficiency results in a low writing speed and a need for a large area to adequately perform a hot electron injection process. Non-volatile memory (NVM) devices that utilize a Fowler-Nordheim tunneling process are efficient. However, the Fowler-Nordheim tunneling process has a low read performance.

This means that there is a fundamental limit on the speed and scaling of conventional non-volatile memory (NVM) devices.

[0003] FIGURE 1 illustrates a schematic diagram of a prior art memory cell 100 of an electrically erasable programmable read only memory (EEPROM) device. Memory cell 100 includes one P-channel metal oxide semiconductor (PMOS) transistor 110 and one P-channel metal oxide semiconductor (PMOS) capacitor 120. The PMOS capacitor 120 is formed by connecting together the source, drain and substrate of a PMOS transistor.

[0004] The PMOS transistor 110 may be referred to as PMOS program transistor 110, while the PMOS capacitor 120 may be referred to as PMOS control capacitor 120. The gate of the PMOS program transistor 110 and the gate of the PMOS control capacitor 120 are connected together (i.e., shorted together) and are isolated from the other active elements. The shorted gates of the PMOS program transistor 110 and the PMOS control capacitor 120 are collectively referred to as a "floating gate" 130. Charges (in amounts that represent either a zero ("0") representation or a one ("1") representation) may be written to the floating gate 130. In order to avoid well bias interference, the PMOS program transistor 110 and the PMOS control capacitor 120 are each located in a separate N well.

[0005] The prior art memory cell 100 is written to by injecting drain avalanche hot electrons into the floating gate 130. For PMOS operation (as shown in FIGURE 1) a low voltage is applied to the control gate and drain of PMOS control capacitor 120 and a high voltage is applied to the source/well of PMOS program transistor 110. The channel of PMOS program transistor 110 is turned on and hot electrons are generated at the high electric field region at the drain junction (designated " V_{INJ} " in FIGURE 1). With positive voltage on the control gate of PMOS control transistor 120, some hot electrons with high energy will pass through the silicon-silicon dioxide (Si-SiO_2) potential barrier and be injected into the floating gate 130.

[0006] The prior art memory cell 100 is erased by applying a high voltage to the control gate of the PMOS control transistor 120 and to the ground drain and source of the PMOS program transistor 110. Electrons on the floating gate 130 will pass through the gate oxide between the floating gate 130 and the control gate of the PMOS control capacitor 120 by Fowler-Nordheim (FN) tunneling process and into the substrate. A description of the physics of the Fowler-Nordheim (FN) tunneling process is set forth in United States Patent No. 5,225,362, which is incorporated herein by

reference.

[0007] FIGURE 2 illustrates a prior art structure 200 that illustrates the use of a plurality of silicon nanocrystals 210 on the surface of a tunnel oxide 220 grown on a silicon substrate. The silicon nanocrystals 210 function as the "floating gate." The tunnel oxide 220 and the silicon nanocrystals 210 are covered with a gate oxide 230. A control gate 240 is located above the gate oxide 230.

[0008] During the erase process, electrons will pass from the silicon nanocrystals 210 through the gate oxide 230 to the control gate 240 by the Fowler-Nordheim (FN) tunneling process. The silicon nanocrystals 210 facilitate the passage of the electrons through the gate oxide 230.

[0009] Prior art silicon nanocrystals 210 are typically either spherical or hemispherical. A typical hemispherical silicon nanocrystal geometry is shown in FIGURE 2. The hemispherical silicon nanocrystal geometry exposes the largest cross-section to the tunnel oxide 220 and provides the most efficient charge injection from the substrate (not shown). The erase process is less efficient likely because the electric field is uniformly distributed on the top surface of the silicon nanocrystals 210.

[0010] Accordingly, there is a need in the art for an improved non-volatile memory (NVM) device (and method of manufacture) that increases the erase efficiency while at the same time maintaining the advantages that are provided by the hemispherical silicon nanocrystals.

SUMMARY

[0011] In accordance with one advantageous embodiment, a non-volatile memory device is provided that comprises a floating gate and a plurality of pyramidal silicon nanocrystals that are associated with the floating gate. Electrons are stored on the pyramidal silicon nanocrystals. When the non-volatile memory device performs an erase process, the electrons tunnel from the plurality of pyramidal silicon nanocrystals through a gate oxide layer to a control gate of the non-volatile memory device.

[0012] A peak at the top of each pyramidal silicon nanocrystal concentrates an electrical field at the peak to facilitate electron tunneling. This allows the erase process to be performed at a lower tunneling voltage and at a lower tunneling time than that of prior art devices.

[0013] The foregoing has outlined rather broadly the features and technical advantages of the present disclosure so that those skilled in the art may better understand the detailed description that follows. Additional features and advantages of the disclosure will be described hereinafter that form the subject of the claims.

Those skilled in the art should appreciate that they may readily use the conception and the specific embodiment disclosed as a basis

for modifying or designing other structures for carrying out the same purposes described herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure in its broadest form.

[0014] Before undertaking the Detailed Description below, it may be advantageous to set forth definitions of certain words and phrases used throughout this patent document: the terms "include" and "comprise," as well as derivatives thereof, mean inclusion without limitation; the term "or," is inclusive, meaning and/or; the phrases "associated with" and "associated therewith," as well as derivatives thereof, may mean to include, be included within, interconnect with, contain, be contained within, connect to or with, couple to or with, be communicable with, cooperate with, interleave, juxtapose, be proximate to, be bound to or with, have, have a property of, or the like; and the term "controller" means any device, system or part thereof that controls at least one operation, such a device may be implemented in hardware, firmware or software, or some combination of at least two of the same. It should be noted that the functionality associated with any particular controller may be centralized or distributed, whether

locally or remotely. Definitions for certain words and phrases are provided throughout this patent document, those of ordinary skill in the art should understand that in many, if not most instances, such definitions apply to prior uses, as well as future uses, of such defined words and phrases.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] For a more complete understanding of the present disclosure, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, wherein like numbers designate like objects, and in which:

[0016] FIGURE 1 illustrates a schematic diagram of a prior art memory cell of an electrically erasable programmable read only memory (EEPROM) device;

[0017] FIGURE 2 is a diagram illustrating a cross sectional side view of a prior art structure having a plurality of hemispherical silicon nanocrystals on the surface of a tunnel oxide of a floating gate;

[0018] FIGURE 3 is a diagram illustrating a cross sectional side view of a structure used to manufacture the plurality of prior art hemispherical silicon nanocrystals shown in FIGURE 2;

[0019] FIGURE 4 is a diagram illustrating a cross sectional side view showing how a plurality of prior art hemispherical silicon nanocrystals are formed from the structure shown in FIGURE 3;

[0020] FIGURE 5 is a transmission electron microscope (TEM)

photograph of a prior art hemispherical silicon nanocrystal;

[0021] FIGURE 6 is a diagram illustrating a cross sectional side view of a structure that illustrates a plurality of pyramidal silicon nanocrystals on the surface of a tunnel oxide of a floating gate in accordance with the present disclosure;

[0022] FIGURE 7 is a diagram illustrating a cross sectional side view of a structure used to manufacture the plurality of pyramidal silicon nanocrystals shown in FIGURE 6;

[0023] FIGURE 8 is a diagram illustrating a cross sectional side view showing an intermediate step in the manufacture of a plurality of pyramidal silicon nanocrystals;

[0024] FIGURE 9 is a diagram illustrating a cross sectional side view showing how a plurality of pyramidal silicon nanocrystals are formed from the structure shown in FIGURE 8;

[0025] FIGURE 10 is a transmission electron microscope (TEM) photograph of a plurality of pyramidal silicon nanocrystals; and

[0026] FIGURE 11 is a diagram illustrating a flowchart of an advantageous embodiment of a method of manufacturing pyramidal silicon nanocrystals in accordance with the present disclosure.

DETAILED DESCRIPTION

[0027] FIGURES 3 through 11 and the various embodiments used to describe the principles of the present disclosure in this patent document are by way of illustration only and should not be construed in any way to limit the scope of the invention. Those skilled in the art will understand that these principles may be implemented in any type of suitably arranged non-volatile memory (NVM) device.

[0028] To simplify the drawings the reference numerals from previous drawings will sometimes not be repeated for structures that have already been identified.

[0029] To better provide a thorough explanation of the technical advantages, a general description of the manufacture of prior art hemispherical silicon nanocrystals will first be given.

[0030] FIGURE 3 is a diagram illustrating a cross sectional side view of an intermediate structure 300 used in the manufacture of the prior art hemispherical silicon nanocrystals 210 shown in FIGURE 2. A silicon substrate 310 is provided with a tunnel oxide layer 320 formed (e.g., grown) on or over the silicon substrate 310. A layer of amorphous silicon 330 (also referred to as a-silicon 330) is formed (e.g., deposited) over the tunnel oxide

layer 320 and a rapid thermal anneal (RTA) process is performed to form a plurality of hemispherical silicon nanocrystals 410 by agglomeration, as shown in FIGURE 4.

[0031] FIGURE 5 is a transmission electron microscope (TEM) photograph of a prior art hemispherical silicon nanocrystal. As shown in FIGURE 5, the length of the base of the hemispherical silicon nanocrystal is approximately nine nanometers (9 nm) and the height is approximately five nanometers (5 nm). In general, a pyramidal silicon nanocrystal may have a base that is in a range of approximately eight nanometers (8 nm) to fifteen nanometers (15nm) and may have a height that is in a range of approximately eight nanometers (8 nm) to fifteen nanometers (15 nm).

[0032] FIGURE 6 is a diagram illustrating a cross sectional side view of a structure 600 that illustrates a plurality of pyramidal silicon nanocrystals 610 disposed on the surface of a tunnel oxide 620 of a floating gate. The tunnel oxide 620 and the pyramidal silicon nanocrystals 610 are covered with a gate oxide 630. A control gate 640 is positioned above the gate oxide 630. Because the silicon nanocrystals 610 are three dimensional structures they are described as being pyramidal. Transmission electron microscope (TEM) pictures show that the silicon

nanocrystals 610 have a non-rounded point (or vertex) at the top. The silicon nanocrystals 610 can be generally described as polyhedral nanocrystals with an upwardly pointing vertex.

[0033] During the erase process, electrons present on the silicon nanocrystals will pass from the tips of pyramidal silicon nanocrystals 610 through the gate oxide 630 to the control gate 640 by the Fowler-Nordheim (FN) tunneling process. The configuration and structure of the pyramidal silicon nanocrystals 610 facilitate the passage of the electrons through the gate oxide 630.

[0034] The shape of the pyramidal silicon nanocrystals 610 provides a nanocrystal peak thereon which is located adjacent to the control gate 640. It will be appreciated that electrons are able to tunnel through the gate oxide 630 from a peak of a pyramidal silicon nanocrystal 610 at a lower applied voltage than required using the prior art hemispherical silicon nanocrystal 210. This is because of the concentration of field lines at the peak of the pyramidal silicon nanocrystal 610 and the control gate 640. In contrast, the electric field lines in the case of a prior art hemispherical silicon nanocrystal 210 are more uniformly distributed over the top surface of the hemispherical silicon nanocrystal 210. The pyramidal geometry facilitates electron

tunneling and allows a reduction in erase voltage as compared to prior art erase voltages. This also allows the erase time to be reduced compared to prior art erase times.

[0035] In addition, it will be appreciated that the thickness of the gate oxide 630 may be chosen or selected to prevent program disturb and read disturb effects. The use of pyramidal-shaped silicon nanocrystals improves the efficiency of the erase process (in terms of lower erase voltages and lower erase times) while essentially maintaining the advantages provided by the prior art hemispherical silicon nanocrystals 210.

[0036] FIGURE 7 is a diagram illustrating a cross sectional side view of an intermediate structure 700 used in the manufacture of the pyramidal-shaped silicon nanocrystals 610 shown in FIGURE 6. A silicon substrate 710 is provided with a tunnel oxide layer 720 formed (e.g., grown) on or over the silicon substrate 710. A layer of a-silicon 730 is formed (e.g., deposited) over the tunnel oxide layer 720 to form the resulting structure 700, as shown in FIGURE 7.

[0037] An oxide deposition process is performed to form a deposited oxide layer 820 over a plurality of brick-shaped (e.g., rectangular-shaped or rectangular cuboid) silicon nanocrystals 810,

as shown in FIGURE 8. The oxide deposition process is followed by a rapid thermal anneal (RTA) process and a furnace anneal. The a-silicon 730 and the tunnel oxide 720 can be sputtered or CVD deposited. The rapid thermal anneal (RTA) can be done at a temperature between eight hundred degrees Celsius (800°C) and nine hundred degrees Celsius (900°C) for up to sixty seconds (60 sec). The furnace anneal can be fifteen minutes (15 min) of annealing at a temperature of one thousand fifty degrees Celsius (1050°C). During the anneal, the a-silicon 730 recrystallizes to form the nanocrystals 810.

[0038] An anneal process, such as a steam anneal process, is performed to form the pyramidal-shaped silicon nanocrystals 910 from the brick-shaped (e.g., rectangular-shaped or rectangular cuboid) silicon nanocrystals 810. In one embodiment, the anneal process includes wet oxidation at a temperature of approximately nine hundred and fifty degrees Celsius (950 °C) in a fifteen to twenty percent (15%-20%) diluted water vapor for about fifteen minutes.

[0039] The resulting structure 900 and the resulting pyramidal-shaped silicon nanocrystals 910 after stripping off the top oxide are shown in FIGURE 9. A gate oxide layer (not shown in FIGURE 9)

is then formed over the tunnel oxide 720 and the pyramidal silicon nanocrystals 910. A control gate layer (not shown in FIGURE 9) is then formed over the gate oxide layer.

[0040] The sequence of processing as described herein is compatible with conventional processing for nanocrystal non-volatile memory (NVM) formation. The size of the pyramidal silicon nanocrystals 910 depends on the layer thicknesses and the anneal conditions. In one advantageous embodiment of the invention, the size and thickness of the pyramidal silicon nanocrystals 910 is approximately ten nanometers (10 nm).

[0041] FIGURE 10 is a transmission electron microscope (TEM) photograph 1000 of a plurality of pyramidal silicon nanocrystals 610, 910. The pyramidal silicon nanocrystals 610, 910 shown in FIGURE 10 are of a suitable size for non-volatile memory (NVM) applications. In one embodiment, the pyramidal silicon nanocrystals 610 have a base having a length of about twelve nanometers (12 nm) and a height of about fourteen nanometers (14 nm). Other suitable dimensions may be utilized.

[0042] FIGURE 11 is a diagram illustrating a flowchart 1100 of an advantageous embodiment of a method of manufacturing the pyramidal silicon nanocrystals 610, 910. The flowchart 1100

summarizes the manufacturing steps that have been previously described.

[0043] A silicon substrate 710 is provided (step 1110), a tunnel oxide layer 720 is formed thereover (step 1120), and a layer of a-silicon 730 is formed over the tunnel oxide layer 720 (step 1130). A series of deposition and anneal steps is performed to form the pyramidal-shaped silicon nanocrystals. In one embodiment, this process includes an oxide deposition process and a rapid thermal anneal (RTA) process which forms a plurality of brick-shaped (e.g., rectangular-shaped or rectangular cuboid) silicon nanocrystals 810 (step 1140) and an anneal process (e.g., steam anneal) that subsequently forms the pyramidal-shaped silicon nanocrystals 910 from the brick-shaped (e.g., rectangular-shaped or rectangular cuboid) silicon nanocrystals (step 1150).

[0044] A gate oxide layer is formed over the tunnel oxide layer 720 and the pyramidal silicon nanocrystals 910 (step 1160) and a control gate layer is formed over the gate oxide layer (step 1170).

[0045] It will be understood that well known processes have not been described in detail and have been omitted for brevity. Although specific steps, structures and materials may have been described, the present disclosure may not be limited to these

specifics, and others may be substituted as is well understood by those skilled in the art.

[0046] While this disclosure has described certain embodiments and generally associated methods, alterations and permutations of these embodiments and methods will be apparent to those skilled in the art. Accordingly, the above description of example embodiments does not define or constrain this disclosure. Other changes, substitutions, and alterations are also possible without departing from the spirit and scope of this disclosure, as defined by the following claims.

WHAT IS CLAIMED IS:

1. A non-volatile memory device that comprises:
a floating gate that comprises at least one pyramidal silicon nanocrystal.
2. The non-volatile memory device that is set forth in Claim 1 wherein the at least one pyramidal silicon nanocrystal is located on a tunnel oxide layer of the floating gate.
3. The non-volatile memory device that is set forth in Claim 2 comprising a gate oxide layer that is formed over the tunnel oxide layer and over the at least one pyramidal silicon nanocrystal.
4. The non-volatile memory device that is set forth in Claim 3 wherein electrons tunnel through the gate oxide layer from the at least one pyramidal silicon nanocrystal.

5. The non-volatile memory device that is set forth in Claim 1 wherein the at least one pyramidal silicon nanocrystal wherein the at least one pyramidal silicon nanocrystal has a base that is in a range of approximately eight nanometers (8 nm) to fifteen nanometers (15nm) and has a height that is in a range of approximately eight nanometers (8 nm) to fifteen nanometers (15 nm).

6. The non-volatile memory device that is set forth in Claim 1 further comprising:

a tunnel oxide layer;

wherein the floating gate that comprises the at least one pyramidal silicon nanocrystal is formed over the tunnel oxide layer; and

a gate oxide layer that is formed over the tunnel oxide layer and over the at least one pyramidal silicon nanocrystal.

7. The non-volatile memory device that is set forth in Claim 6 wherein electrons tunnel through the gate oxide layer from the at least one pyramidal silicon nanocrystal.

8. The non-volatile memory device that is set forth in Claim 7 wherein the pyramidal silicon nanocrystal comprises a peak that concentrates an electrical field at the peak of the pyramidal silicon nanocrystal.

9. The non-volatile memory device that is set forth in Claim 8 wherein the peak of the pyramidal silicon nanocrystal allows electrons to tunnel through the gate oxide layer at a lower tunneling voltage than that required for electrons tunneling from a hemispherical silicon nanocrystal.

10. The non-volatile memory device that is set forth in Claim 8 wherein the peak of the pyramidal silicon nanocrystal allows electrons to tunnel through the gate oxide layer with a shorter tunneling time than that required for electrons tunneling from a hemispherical silicon nanocrystal.

11. The non-volatile memory device that is set forth in Claim 6 wherein the at least one pyramidal silicon nanocrystal has a base that is in a range of approximately eight nanometers (8 nm) to fifteen nanometers (15nm) and has a height that is in a range of approximately eight nanometers (8 nm) to fifteen nanometers (15 nm) .

12. A method of operating a non-volatile memory device wherein the method comprises the steps of:

providing at least one pyramidal silicon nanocrystal that is associated with a floating gate of the non-volatile memory device;

performing an erase operation in which electrons tunnel through a gate oxide layer of the non-volatile memory device from the at least one pyramidal silicon nanocrystal.

13. The method that is set forth in Claim 12 wherein the pyramidal silicon nanocrystal comprises a peak that concentrates an electrical field at the peak of the pyramidal silicon nanocrystal.

14. The method that is set forth in Claim 13 wherein the peak of the pyramidal silicon nanocrystal allows electrons to tunnel through the gate oxide layer at a lower tunneling voltage than that required for electrons tunneling from a hemispherical silicon nanocrystal.

15. The method that is set forth in Claim 13 wherein the peak of the pyramidal silicon nanocrystal allows electrons to tunnel through the gate oxide layer with a shorter tunneling time that that required for electrons tunneling from a hemispherical silicon nanocrystal.

16. A method of operating a non-volatile memory device, wherein the method comprises the steps of:

providing non-volatile memory device having a floating gate;

providing in association with the floating gate a plurality of pyramidal silicon nanocrystals operable for storing electrons; and

performing an erase operation in which the electrons tunnel through a gate oxide layer of the non-volatile memory device from the plurality of pyramidal silicon nanocrystals.

17. The method that is set forth in Claim 16 wherein each of the plurality of pyramidal silicon nanocrystals comprises a peak that concentrates an electrical field at the peak of the pyramidal silicon nanocrystal.

18. The method that is set forth in Claim 17 wherein the peaks of the pyramidal silicon nanocrystals allow electrons to tunnel through the gate oxide layer at a lower tunneling voltage than that required for electrons tunneling from a hemispherical silicon nanocrystal.

19. The method that is set forth in Claim 17 wherein the peaks of the pyramidal silicon nanocrystals allow electrons to tunnel through the gate oxide layer with a shorter tunneling time than that required for electrons tunneling from a hemispherical silicon nanocrystal.

20. The method as set forth in Claim 13 wherein each of the plurality of pyramidal silicon nanocrystals has a base that is in a range of approximately eight nanometers (8 nm) to fifteen nanometers (15nm) and has a height that is in a range of approximately eight nanometers (8 nm) to fifteen nanometers (15 nm).