

Abstract of the Disclosure

A memory system is organized as a matrix including a memory cell at each intersection of a bit line with write and read word lines. Each memory cell comprises a first FET 20 having its gate coupled to a write word line and its drain coupled to a bit line, a second FET 22 having its source coupled to the bit line and its drain coupled to a read word line, and first and second negative resistance devices 24,26 coupled in series between a supply voltage and a substrate voltage, the common point SN of the series-connected negative resistance devices being coupled to the source of the first FET and to the gate of the second FET. Preferably, the first FET 20 is a p-channel device, the second FET 22 is an n-channel device, and the first and second negative resistance devices 24,26 are RTDs. In a second embodiment, a memory system has a memory cell at each intersection of a bit line with a word line. The memory cell comprises an FET having its gate coupled to a word line and one of its drain and source electrodes coupled to a bit line, first and second negative resistance devices 44,46 coupled in series between a supply voltage and a substrate voltage, the common point SN of the series-connected negative resistance devices being coupled to the other of the drain and source electrodes, and a capacitance 48 coupled between the common point of the series-connected negative resistance devices.

