CLAIMS

WHAT IS CLAIMED:

1. A method of forming a semiconductor device, the method comprising:

forming a material layer stack above a first device region (202A) and a second device region (202B), said material layer stack comprising a dielectric base layer (252), a high-k dielectric material (253) formed on said dielectric base layer (252) and metal-containing material (207) formed on said high-k dielectric material (253);

performing a heat treatment (208) so as to diffuse a metal species from said metal-containing material (207) to an interface formed by said dielectric base layer (252) and said high-k dielectric material (253);

forming a dielectric layer (251B) selectively above said second device region (202B) after performing said heat treatment (208); and

forming a first gate electrode structure (250A) above said first device region (202A) and a second gate electrode structure (250B) above said second device region (202B), said first gate electrode structure comprising said dielectric base layer (252) and said high-k dielectric material (253) as a first gate dielectric and said second gate electrode structure comprising said dielectric base layer (252), said high-k dielectric material (253) and said dielectric layer (251B) as a second gate dielectric.

2. The method of claim 1, wherein forming said dielectric layer (251B) selectively above said second device region (202B) comprises removing said metal-containing material (207) selectively above said second device region (202B), depositing said dielectric layer above said first and second device region and removing said dielectric layer selectively from above said first device region (202A) by using said metal-containing material (207) as an etch stop.

3. The method of claim 1, further comprising removing said metal-containing material (207) after forming said dielectric layer (251B) selectively above said second device region (202B) and forming a second metal-containing material (255) above said first and second device regions.

4. The method of claim 1, wherein forming said material layer stack comprises forming a first metal-containing material on said high-k dielectric material (253) and forming a work function adjusting species (254A) on said first metal-containing material (207).

5. The method of claim 2, wherein said metal-containing material (207) comprises titanium nitride.

6. The method of claim 1, further comprising forming a first transistor (260A) in said first device region (202A) on the basis of said first gate electrode structure (250A) and forming a second transistor (260B) in said second device region (202B) on the basis of said second gate electrode structure (250B), wherein said first and second transistors have substantially the same threshold voltage.

7. The method of claim 1, further comprising removing said metal-containing material (207) from above said first and second device regions and forming a second metal-containing material selectively above said first device region (202A) prior to forming said dielectric layer (251B) selectively above said second device region (202B).

8. The method of claim 7, further comprising forming an electrode material on said second metal-containing material above said first device region (202A) and forming said electrode material on said dielectric layer above said second device region (202B).

9. A method, comprising:

forming a dielectric base layer (252) above a first semiconductor region (202A) and a second semiconductor region (202B) of a semiconductor device;

forming a high-k dielectric material (253) on said dielectric base layer (252) above said first and second semiconductor regions, said dielectric base layer (252) and said high-k dielectric material (253) forming an interface;

forming a work function adjusting species (254A) at said interface above said first and second semiconductor regions;

forming a dielectric material (251B0 on said high-k dielectric material (253) selectively above said second semiconductor region (202B); and

forming a first gate electrode structure (250A) above said first semiconductor region (202A) and a second gate electrode structure (250B) above said second semiconductor region (202B).

10. The method of claim 9, further comprising forming a metal-containing material layer on said high-k dielectric material (253) and on said dielectric material.

11. The method of claim 9, further comprising forming a metal-containing material selectively on said high-k dielectric material (253) and forming an electrode material on said metal-containing material and on said dielectric material.

12. The method of claim 9, wherein forming said work function adjusting species (254A) at said interface comprises forming a material layer comprising said work function adjusting species (254A) on said high-k dielectric layer (253) and annealing said semiconductor device.

13. The method of claim 12, further comprising removing said material layer and forming a metal-containing material selectively on said high-k dielectric material (253) above said first semiconductor region (202A).

14. The method of claim 13, wherein said material layer and said metal-containing material comprises titanium nitride.

15. A semiconductor device, comprising:

a first gate electrode structure (250A) formed above a first semiconductor region (202A) and comprising a first dielectric base layer (252), a first high-k dielectric material (253) formed on said first dielectric base layer (252) and a metal-containing electrode material formed on said first high-k dielectric material (253); and

a second gate electrode structure (250B) formed above a second semiconductor region (202B) and comprising a second dielectric base layer, a second high-k dielectric material formed on said

second dielectric base layer and a dielectric layer formed on said second high-k dielectric material.

16. The semiconductor device of claim 15, wherein said first and second dielectric base layers have the same material composition and wherein said first and second high-k dielectric material have the same material composition.

17. The semiconductor device of claim 15, wherein said metal-containing electrode material comprises titanium nitride.

What is claimed:

1. A method of forming a semiconductor device, the method comprising: forming a material layer stack above a first device region and a second device region, said material layer stack comprising a dielectric base layer, a high-k dielectric material formed on said dielectric base layer and metal-containing material formed on said high-k dielectric material; performing a heat treatment so as to diffuse a metal species from said metal-containing material to an interface formed by said dielectric base layer and said high-k dielectric material; forming a dielectric layer selectively above said second device region after performing said heat treatment; and forming a first gate electrode structure above said first device region and a second gate electrode structure above said second device region, said first gate electrode structure comprising said dielectric base layer and said high-k dielectric material as a first gate dielectric and said second gate electrode structure comprising said dielectric base layer, said high-k dielectric material and said dielectric layer as a second gate dielectric.

2. The method of claim 1, wherein forming said dielectric layer selectively above said second device region comprises removing said metal-containing material selectively above said second device region, depositing said dielectric layer above said first and second device region and removing said dielectric layer selectively from above said first device region by using said metal-containing material as an etch stop.

3. The method of claim 2, wherein said metal-containing material comprises titanium nitride.

4. The method of claim 3, wherein removing said dielectric layer selectively from above said second device region further comprises performing a wet chemical etch process on the basis of hydrofluoric acid.

5. The method of claim 1, further comprising removing said metal-containing material after forming said dielectric layer selectively above said second device region and forming a second metal-containing material above said first and second device regions.

6. The method of claim 1, wherein forming said material layer stack comprises forming a first metal-containing material on said high-k dielectric material and forming a work function adjusting species on said first metal-containing material.

7. The method of claim 1, wherein said dielectric base layer comprises silicon and oxygen.

8. The method of claim 1, wherein said dielectric layer comprises silicon dioxide.

9. The method of claim 1, further comprising forming a first transistor in said first device region on the basis of said first gate electrode structure and forming a second transistor in said second device region on the basis of said second gate electrode structure, wherein said first and second transistors have substantially the same threshold voltage.

10. The method of claim 1, further comprising removing said metal-containing material from above said first and second device regions and forming a second metal-containing material

selectively above said first device region prior to forming said dielectric layer selectively above said second device region.

11. The method of claim 10, further comprising forming an electrode material on said second metal-containing material above said first device region and forming said electrode material on said dielectric layer above said second device region.

12. The method of claim 11, further comprising forming a transistor in said first device region on the basis of said first gate electrode structure and forming a resistor in said second device region on the basis of said second gate electrode structure.

13. A method, comprising: forming a dielectric base layer on a first semiconductor region and a second semiconductor region of a semiconductor device; forming a high-k dielectric material on said dielectric base layer above said first and second semiconductor regions, said dielectric base layer and said high-k dielectric material forming an interface; forming a work function adjusting species at said interface above said first and second semiconductor regions; forming a dielectric material on said high-k dielectric material selectively above said second semiconductor region; and forming a first gate electrode structure on said first semiconductor region and a second gate electrode structure on said second semiconductor region.

14. The method of claim 13, further comprising forming a metal-containing material layer on said high-k dielectric material and on said dielectric material.

15. The method of claim 14, further comprising forming a semiconductor electrode material on said metal-containing material.

16. The method of claim 13, further comprising forming a metal-containing material selectively on said high-k dielectric material and forming an electrode material on said metal-containing material and on said dielectric material.

17. The method of claim 13, wherein forming said work function adjusting species at said interface comprises forming a material layer comprising said work function adjusting species on said high-k dielectric layer and annealing said semiconductor device.

18. The method of claim 17, further comprising removing said material layer and forming a metal-containing material selectively on said high-k dielectric material above said first semiconductor region.

19. The method of claim 18, wherein said material layer and said metal-containing material comprises titanium nitride.

20. A semiconductor device formed in accordance with any one of the preceding claims.