

PATENT SPECIFICATION

(11) 1 534 521

- (21) Application No. 50854/75 (22) Filed 11 Dec. 1975
 (31) Convention Application No. 50/000103
 (32) Filed 6 Jan. 1975 in
 (33) Japan (JP)
 (44) Complete Specification published 6 Dec. 1978
 (51) INT CL² H03K 19/08
 (52) Index at acceptance
 H3T 1CX 2E 2J 4C 4X



(54) AN INPUT CIRCUIT FOR A MISFET
 INTEGRATED CIRCUIT

(71) We, HITACHI LIMITED of 1-5-1 Marunouchi, Chiyoda-ku, Tokyo, Japan, a body corporate organized according to the laws of Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to an input circuit for a largescale integrated circuit (hereinafter referred to as a "LSI") which is composed of insulated gate field-effect transistors (hereinafter referred to as "MISFETs").

In general, a small-size electronic desk top calculator has its control circuit constructed as an LSI.

A circuit for driving a numeral display device in a small-sized electronic desk top calculator requires a high voltage output, and therefore previously could not be manufactured in an LSI. With the progress of the semiconductor integrated circuit technology, it has become possible to build up within the LSI a numeral display circuit providing a high voltage output.

However, a new problem has arisen. In an electronic desk top calculator, an output signal of the display device need sometimes be employed as an input for various reasons, for example, the necessity for diminishing the number of external lead-out terminals. Since, in the past, the output signal level of LSIs was small, it presented no problem to apply the signal directly as an input. However, in case where the output signal has a high voltage signal level, as described above, such problems as the dielectric breakdown of the gate of an input MISFET may occur.

In order to simplify a key input circuit of an electronic desk top calculator, we have designed a key input circuit which does away with the need to provide an encoder circuit for transforming a key input signal into a binary code, as has previously been necessary. As shown in Figure 2 of the accompanying drawing, in this circuit, gate

circuits G1 to G4 are controlled by a key input which is synchronized with a digital signal, the digital signal being an output of a semiconductor integrated circuit 1, and serving to drive a numeral display device 2. A count pattern of a digit counter circuit 4 which has passed through the gate circuits G1 to G4 is fed into an input buffer register 6 as a key input pattern.

The circuit also includes a decoder circuit 5 for forming the digital signal, and high voltage output circuits DR1 to DRn connected between the decoder circuit 5 and the numeral display device 2.

In the key input circuit, the signal received through a key switch 3 is the digital signal for driving the numeral display device 2, and therefore is a high voltage signal as previously explained. An input circuit 7 on which the signal is to be impressed is therefore liable to suffer destruction of the gate of a constituent MISFET because of the high amplitude signal level (30 to 35 V) delivered to the numeral display device 2. It is necessary to prevent such destruction without exerting any influence on the signal level.

According to the present invention there is provided an input circuit for a MISFET integrated circuit including: a first enhancement type MISFET which is connected between an input terminal and a power supply terminal for said input circuit; and second and third MISFETs, said second MISFET being connected between said input terminal and the gate electrode of the third MISFET, the gate electrode of the second MISFET being connected to said power supply terminal, the output from said input circuit being derived across said third MISFET.

An embodiment of the present invention will now be described, by way of example, with reference to Figure 1 of the accompanying drawing, which is a circuit diagram of an input circuit for an electronic desk top calculator.

Referring to Figure 1, the input circuit includes MISFETs M1 to M6, resistor R1,

8

R2 and RL, a display device 2 and a key switch 3.

In the event that a high amplitude signal V_{DISP} (30 V to 35 V) which is controlled by the MISFETs M5 and M6 and which serves to drive the display device 2 is again received as an input to an input terminal IN through the key switch 3, the high amplitude signal is impressed on the driving MISFET M4, constituting the input circuit, through the following circuit in order to prevent dielectric breakdown of the gate of the driving MISFET M4 of the input circuit caused by the high amplitude signal.

Between the input terminal IN on which the high amplitude signal is impressed and a terminal V_{GG} of a low supply voltage (14 volts) for the input circuit, the MISFET M1 of enhancement type and the resistor R1 are connected in series, the gate electrode of the MISFET M1 being connected to the supply terminal V_{GG} . Between the input terminal IN and the gate electrode of the driving MISFET M4 of the input circuit, the resistor R2 and the MISFET M2 are connected in series, the gate electrode of the MISFET M2 being connected to the supply terminal V_{GG} .

The resistors R1 and R2 which are connected in series with the respective MISFETs M1 and M2, are provided in order to protect the MISFETs M1 and M2 from dielectric breakdown. The resistors may have a value of resistance of approximately 1 to 2 Kohms, and can be made up as defused regions within a single semiconductor substrate by impurity diffusion at the same time as the step of diffusing and forming the source and drain electrodes of the MISFETs. The MISFET M2 may be either of the enhancement type or of the depletion type.

A load MISFET M3 is provided in series with the MISFET M4 across a second power supply V_{DD} , the gate electrode of the MISFET M3 being connected to the first power supply V_{GG} .

With the input circuit of the above construction, when a high level signal is applied to the input terminal IN, the input side electrode (usually acting as the source electrode) of the MISFET M1 experiences a signal of level greater than that of the power supply side electrode (usually acting as the drain electrode), and the electrodes act conversely. That is, the input side becomes the drain electrode and the power supply side the source electrode for the duration of the high level signal. Since the source and the gate electrodes are accordingly at an identical potential, the MISFET M1 turns "off" and permits no current to flow between the input terminal IN and the supply terminal V_{GG} . Thus, the

voltage V_{DISP} to be impressed on the display device can be maintained at a high level.

On the other hand, the voltage level applied to the gate of the driving MISFET M4 of the input circuit does not become greater than $V_{GG} - V_{th2}$ because of the MISFET M2, whose gate electrode is supplied with the low supply voltage V_{GG} . Here, V_{th2} denotes the threshold voltage of the MISFET M2. In consequence, when the MISFET M2 is a transistor of the enhancement type the above voltage becomes $|V_{GG} - V_{th2}|$, whilst when it is a transistor of the depletion type, the above voltage becomes $|V_{GG} + V_{th2}|$. That is, the voltage level which is impressed on the gate of the MISFET M4 is determined only by the supply voltage and the threshold voltage of the MISFET M2. Thus, no high voltage is impressed on the gate electrode of the driving MISFET M4, and gate dielectric breakdown of the MISFET M4 is prevented.

The MISFET M1 also functions to determine the voltage level which is impressed on the driving MISFET M4 when the key switch 3 is "off".

In a modified form of the input circuit, the resistors R1 and R2 for the protection of the MISFETs M1 and M2 to which the high voltage is applied, are externally-mounted resistors instead of the diffused resistors. It is obvious that, when protection of the gate insulations of the MISFETs M1 and M2 is not required, the protective resistors R1 and R2 are unnecessary.

The above described input circuit can be extensively utilized, not only in electronic desk top calculators, but also in general circuits in which a high amplitude signal level to be impressed on an LSI is lowered only within the LSI.

Attention is drawn to our Application No. 47136/75 (Serial No. 1,524,558).

WHAT WE CLAIM IS:—

1. An input circuit for a MISFET integrated circuit including: a first, enhancement type MISFET, which is connected between an input terminal and a power supply terminal for said input circuit; and second and third MISFETs, said second MISFET being connected between said input terminal and the gate electrode of the third MISFET, the gate electrode of the second MISFET being connected to said power supply terminal, the output from said input circuit being derived across said third MISFET.

2. An input circuit according to claim 1, wherein the gate electrode of the first MISFET is connected to said power supply terminal.

3. An input circuit according to claim 1 or 2, further including: a first resistor



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R2 and RL, a display device 2 and a key switch 3.

In the event that a high amplitude signal V_{DISP} (30 V to 35 V) which is controlled by the MISFETs M5 and M6 and which serves to drive the display device 2 is again received as an input to an input terminal IN through the key switch 3, the high amplitude signal is impressed on the driving MISFET M4, constituting the input circuit, through the following circuit in order to prevent dielectric breakdown of the gate of the driving MISFET M4 of the input circuit caused by the high amplitude signal.

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The resistors R1 and R2 which are connected in series with the respective MISFETs M1 and M2, are provided in order to protect the MISFETs M1 and M2 from dielectric breakdown. The resistors may have a value of resistance of approximately 1 to 2 Kohms, and can be made up as defused regions within a single semiconductor substrate by impurity diffusion at the same time as the step of diffusing and forming the source and drain electrodes of the MISFETs. The MISFET M2 may be either of the enhancement type or of the depletion type.

A load MISFET M3 is provided in series with the MISFET M4 across a second power supply V_{DD} , the gate electrode of the MISFET M3 being connected to the first power supply V_{GG} .

With the input circuit of the above construction, when a high level signal is applied to the input terminal IN, the input side electrode (usually acting as the source electrode) of the MISFET M1 experiences a signal of level greater than that of the power supply side electrode (usually acting as the drain electrode), and the electrodes act conversely. That is, the input side becomes the drain electrode and the power supply side the source electrode for the duration of the high level signal. Since the source and the gate electrodes are accordingly at an identical potential, the MISFET M1 turns "off" and permits no current to flow between the input terminal IN and the supply terminal V_{GG} . Thus, the

voltage V_{DISP} to be impressed on the display device can be maintained at a high level.

On the other hand, the voltage level applied to the gate of the driving MISFET M4 of the input circuit does not become greater than $V_{GG} - V_{th2}$ because of the MISFET M2, whose gate electrode is supplied with the low supply voltage V_{GG} . Here, V_{th2} denotes the threshold voltage of the MISFET M2. In consequence, when the MISFET M2 is a transistor of the enhancement type the above voltage becomes $|V_{GG} - V_{th2}|$, whilst when it is a transistor of the depletion type, the above voltage becomes $|V_{GG} + V_{th2}|$. That is, the voltage level which is impressed on the gate of the MISFET M4 is determined only by the supply voltage and the threshold voltage of the MISFET M2. Thus, no high voltage is impressed on the gate electrode of the driving MISFET M4, and gate dielectric breakdown of the MISFET M4 is prevented.

The MISFET M1 also functions to determine the voltage level which is impressed on the driving MISFET M4 when the key switch 3 is "off".

In a modified form of the input circuit, the resistors R1 and R2 for the protection of the MISFETs M1 and M2 to which the high voltage is applied, are externally-mounted resistors instead of the diffused resistors. It is obvious that, when protection of the gate insulations of the MISFETs M1 and M2 is not required, the protective resistors R1 and R2 are unnecessary.

The above described input circuit can be extensively utilized, not only in electronic desk top calculators, but also in general circuits in which a high amplitude signal level to be impressed on an LSI is lowered only within the LSI.

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2. An input circuit according to claim 1, wherein the gate electrode of the first MISFET is connected to said power supply terminal.

3. An input circuit according to claim 1 or 2, further including: a first resistor

9

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- connected in series between the first MISFET and the input terminal; and a second resistor connected in series between the second MISFET and the input terminal.
- 5 4. An input circuit according to any one of the preceding claims, wherein a fourth MISFET is connected in series with the third MISFET across a second power supply, the gate electrode of the fourth MISFET being connected to the first power supply terminal.
- 10 5. A key input circuit for a numeral display device, incorporating an input circuit according to any one of the preceding claims. 15
6. An input circuit for a MISFET integrated circuit constructed and arranged to operate substantially as described herein, with reference to and as illustrated in Figure 1 of the accompanying drawing. 20

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Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1978
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from
which copies may be obtained.

