

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
2 October 2003 (02.10.2003)

PCT

(10) International Publication Number
WO 03/081779 A1

(51) International Patent Classification⁷: H03L 7/08,
7/091, 7/099, H04L 7/033, G06F 1/08, H03K 5/135

(21) International Application Number: PCT/US03/07707

(22) International Filing Date: 12 March 2003 (12.03.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/100,803 18 March 2002 (18.03.2002) US

(71) Applicant: GENESIS MICROCHIP, INC. [US/US];
2150 Gold Street, Alviso, CA 95002 (US).

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

(71) Applicant and

(72) Inventor: GRUSHIN, Stanislav [RU/US]; 1562 Birchmeadow Court, San Jose, CA 95131 (US).

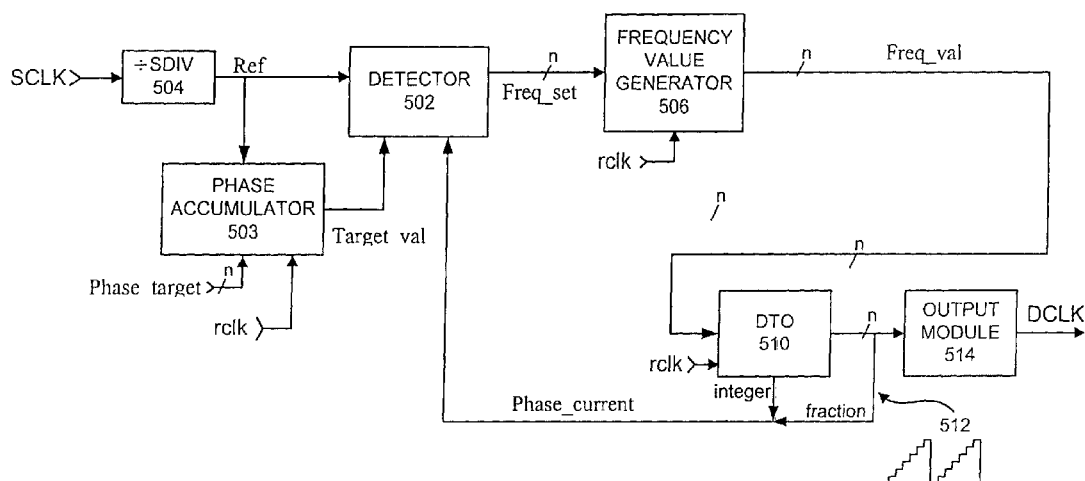
(74) Agent: FERRAZANO, Michael, J.; Beyer Weaver & Thomas, LLP, P.O. BOX 778, Berkeley, CA 94704-0778 (US).

Published:

— with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: FREQUENCY CONVERTER AND METHODS OF USE THEREOF



(57) Abstract: An all-digital frequency conversion apparatus is provided that achieves frequency conversion using a simple phase detector and integer and fractional phase feedback information from a digital oscillator output. In an embodiment, a target phase accumulator unit (503) generates a target phase signal to the phase detector unit (502). The target phase accumulator unit receives inputs from a reference signal input (rclk), and a target phase input value. The digital phase detector unit receives the reference signal, a current phase feedback input signal, and the target phase input signal. The phase detector unit outputs a frequency setting signal to a frequency value generator unit (506). The detector output is based on the difference between the current phase and the target phase. A frequency value generator unit is configured to output a frequency value signal to a digital oscillator unit (510) that generates a corresponding digital output signal that is directly fed back to the current phase feedback input of the phase detector unit. A method, computing system, and software product that implement the present invention are also provided.