

VERTICAL SYNCHRONISING CONTROL CIRCUIT

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This invention relates to vertical synchronising control circuits.

According to one aspect of the present invention there is provided vertical synchronising control circuit comprising: a vertical
10 synchronising control signal forming circuit for dividing a clock signal and for producing a first control signal and a vertical synchronising control signal in synchronism with an external vertical synchronising signal; a gate circuit for selectively passing said external vertical synchronising signal; and a
15 detector circuit for producing a second control signal when the passage of the external vertical synchronising signal through the gate circuit is detected, the gate circuit being connected to receive the first and second control signals, and the vertical synchronising control signal forming circuit being connected to
20 receive the external vertical synchronising signal that has passed through the gate circuit, the arrangement being such that the external vertical synchronising signal is allowed to pass through the gate circuit until the second control signal is fed thereto when the first control signal is fed thereto and the external
25 vertical synchronising signal is prevented from passing through

17

the gate circuit until the first control signal is fed thereto when the second control signal is fed thereto.

Preferably the vertical synchronising control circuit signal forming circuit includes a divider circuit arranged to divide the clock signal by n , where n is an integer to produce a signal having the same frequency as the external vertical synchronising signal.

According to a further aspect of the present invention there is provided a television receiver having a vertical synchronising control circuit as recited above.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figure 1 is a block diagram of a conventional vertical synchronising circuit;

Figure 2 is a timing chart showing the waveforms of signals appearing at various points in the conventional vertical synchronising control circuit;

Figure 3 is a block diagram of one embodiment of a vertical synchronising control circuit according to the present invention;

Figure 4 is a timing chart showing the waveforms of signals appearing at various points in the vertical synchronising control circuit of Figure 3 when an external vertical synchronising signal includes a noise component;

Figure 5 is a timing chart similar to Figure 4 when the external vertical synchronising signal disappears due, for example,

to a sudden change of field intensity;

Figure 6 is a circuit diagram of one embodiment of a television receiver including a vertical synchronising control circuit according to the present invention; and

5 Figure 7 is a timing chart showing the waveforms of signals appearing at various points in the television receiver of Figure 6.

In a convention vertical synchronising control circuit of a television receiver, a vertical synchronising control signal is
10 formed by dividing a signal having a frequency which is an integral number of times greater than the frequency of a horizontal synchronising signal. The vertical synchronising control signal is used for control of a display device such as, for example, a television receiver, instead of an external vertical synchronising
15 signal but is synchronised with the external vertical synchronising signal.

However, conventionally, the vertical synchronising control signal is directly synchronised with the external vertical synchronising signal separated from a composite TV signal as shown
20 in Figure 1.

Figure 1 is a block diagram of a conventional vertical synchronising control circuit having an input terminal 1 to which a clock signal which has a frequency $\underline{n}$ (where $\underline{n}$ is an integer) times the frequency f_H of a horizontal synchronising signal
25 (hereinafter referred to as "the $n f_H$ signal") and which is in

(19)

- 4 -

synchronism with a horizontal synchronising signal separated from a composite television signal. At external vertical synchronising signal is applied to an input terminal 2. A vertical synchronising control signal appears at an output terminal 3 of
5 a vertical synchronising control signal forming circuit 4. The nfH signal is fed to the vertical synchronising control signal forming circuit 4 from the input terminal 1. In the vertical synchronising control signal forming circuit 4, the nfH signal is divided to form a vertical synchronising control signal in
10 synchronism with the external vertical synchronising signal fed to the vertical synchronising control signal forming circuit 4 from the input terminal 2. The vertical synchronising control signal is delivered to the output terminal 3.

Figure 2 is a timing chart showing the waveforms at three
15 points A, B, C in the conventional vertical synchronising control circuit of Figure 1. Waveform A is the nfH signal which is fed to the vertical synchronising control signal forming circuit 4 from the input terminal 1. Waveform B is a signal after shaping the waveform of the external vertical synchronising signal
20 separated from the composite television signal, wherein T_0 is the period of the vertical synchronising signal and N_0 is a noise component. Waveform C is a vertical synchronising control signal formed by the vertical synchronising control signal forming circuit 4 wherein T_1 is a vertical blanking period and a delay
25 time including the vertical synchronising control signal required

for various kinds of display device, and N_1 is a vertical synchronising control signal in synchronism with the noise component No. Thus a vertical synchronising control signal is generated irrespective of the external vertical synchronising signal. As shown in Figure 2, the conventional vertical synchronising control circuit generates the vertical synchronising control signal in synchronism with not only the external vertical synchronising signal but also a noise component thereof. As a result, this conventional vertical synchronising control circuit has the disadvantage in that quality of a television display deteriorates as a result of unstable vertical synchronisation, due to the vertical synchronising control signal N_1 generated in synchronism with the noise component No of the external vertical synchronising signal.

Figure 3 is a block diagram of one embodiment of a vertical synchronising control circuit according to the present invention. Like parts in Figures 1 and 3 have been designated by the same reference numerals and will not be described in detail further. A gate circuit 5 controls the passage of the external vertical synchronising signal, and a detector circuit 6 detects the passage of the external vertical synchronising signal through the gate circuit 5 and delivers a control signal to the gate circuit. If the external vertical synchronising control signal disappears due to, for example, a sudden change of field intensity, the vertical synchronising control signal forming circuit 4 continues

to count the nfH signal with the same period as the vertical synchronising signal to deliver the vertical synchronising control signal and the output terminal 3 and a control signal to the gate circuit 5 which are the same as the vertical
5 synchronising signal in frequency.

Figures 4 and 5 are timing charts showing the waveforms at points A to F in the vertical synchronising control circuit of Figure 3. Waveform A is the nfH signal, waveform B indicates the signal after shaping the external vertical synchronising signal
10 separated from a composite television signal, waveform C indicates the control signal from the vertical synchronising control signal forming circuit 4 to the gate circuit 5 which allows the external vertical synchronising signal to pass through the gate circuit 5, waveform D indicates the control signal from the
15 detector circuit 6 to the gate circuit 5 inhibiting the external vertical synchronising signal from passing through the gate circuit 5, waveform E indicates the external vertical synchronising signal after it has passed through the gate circuit 5 and waveform F indicates the vertical synchronising control signal.

20 Figure 4 is a timing chart illustrating the case where the external vertical synchronising signal includes a noise component. The nfH signal is fed to the vertical synchronising control signal forming circuit 4 via the the input terminal 1. In the vertical synchronising control signal forming circuit 4, the nfH signal is
25 divided to deliver the control signal indicated by waveform C and

the vertical synchronising control signal indicated by waveform F. Herein, T_0 , indicated by waveform B, represents the period of the vertical synchronising signal and N_0 represents the noise component. When the control signal from the vertical synchronising control signal forming circuit 4 is fed to the gate circuit 5, the latter allows the external vertical synchronising signal from the input terminal 2 to pass during periods T_a . The detector circuit 6 detects the external vertical synchronising signal that has passed through the gate circuit 5 and delivers the control signal to the gate circuit. When this control signal is fed to the gate circuit, the external vertical synchronising signal is prevented from passing through the gate circuit 5 during periods T_b , that is, until the control signal from the vertical synchronising control signal forming circuit 4 is fed thereto. In this way, as shown by waveforms E, F, the noise component is blocked by the gate circuit 5. As a result, a stable and precise vertical synchronising control signal without a noise component can be obtained at the output terminal 3. Herein, in waveform F a delay time T_1 includes the vertical synchronising control signal which is necessary to the vertical blanking period.

Figure 5 is a timing chart illustrating the case where the external vertical synchronising signal disappears due to, for example, a sudden change of field intensity.

In the vertical synchronising control circuit, vertical synchronising control is not performed with the external vertical

synchronising signal but with the vertical synchronising control signal which is formed by dividing the nfH signal. Accordingly, even if the external vertical synchronising signal disappears, the vertical synchronising control signal forming circuit 4 counts
5 the nfH signal, and delivers a vertical synchronising control signal with the same period as that of the external vertical synchronising signal. In this case, if the vertical synchronising control signal is in synchronism with the previous external vertical synchronising signal, before the external vertical
10 synchronising signal disappears, a stable and precise vertical synchronising control signal can be obtained as shown in waveform F of Figure 5 just as in the case where the external vertical synchronising signal is present. $\bar{V}$ of waveform B of Figure 6 indicates the disappearance of the external vertical synchronising
15 signal.

When the external vertical synchronising signal re-appears the vertical synchronising control circuit will response immediately. That is, when the external vertical synchronising signal disappears the control signal is not produced by the detector circuit 6 as
20 the external vertical synchronising signal is not detected. As a result, the gate circuit 5 maintains the state where the external vertical synchronising signal is allowed to pass, which enables the external vertical synchronising signal to pass immediately through the gate circuit 5 when it re-appears at the
25 input terminal 2. Therefore, the vertical synchronising control

signal can be synchronised with the external vertical synchronizing signal. For example, although the external vertical synchronising signal often disappears when tuning a television receiver, it is possible to obtain a stable screen in synchronism with the external vertical synchronising signal immediately by using the vertical synchronising control circuit of Figure 3.

In Figures 4 and 5 one example of the timing of the control signals is given. The control signal from the vertical synchronising control signal forming circuit 4 can be produced at various timings, viz. not only before the expected time of the external vertical synchronising signal, but at the expected timing of the leading edge of the external vertical synchronising signal or after the expected timing when the external vertical synchronising signal has been already inputted. Further, the control signal from the detector circuit 6 can be produced at various timings, viz. not only at the timing of detecting the trailing edge of the external vertical synchronising signal, but at the timing of detecting the leading edge of the external vertical synchronising signal or at a timing when a fixed period has passed after the leading edge of the external vertical synchronising signal. Depending upon the timings of the control signals, the external vertical synchronising signal passed through the gate circuit 5 sometimes differs from that applied to the input terminal 2 in pulse width, but this is not materially significant.

Figure 6 illustrates one embodiment of a television receiver

including a vertical synchronising control circuit according to the present invention. The television receiver comprises an antenna 7, a video receiver circuit 8 where a signal of a desired channel is selected from among signals provided by the antenna 7, amplified and detected so producing a television signal or composite video signal, a synchronising separator circuit 9 for separating a composite synchronising signal from the television signal, a horizontal synchronising signal separator circuit 10 for separating a horizontal synchronising signal from the composite synchronising signal, a 2fH signal generating circuit 11 for generating a signal in synchronism with the horizontal synchronising signal, but having twice the frequency, a vertical synchronising signal separator circuit 12 for separating a vertical synchronising signal from the composite synchronising signal, and a wave shaping circuit 13 for shaping the waveform of the output of the vertical synchronising signal separator circuit 12. The vertical synchronising control signal forming circuit 4, shown in greater detail in Figure 6, is where the 2fH signal is counted and then a vertical synchronising control signal which is the same frequency as that of the vertical synchronising signal is formed.

The vertical synchronising control signal forming circuit 4 has inverters 16 to 19, AND gates 22, 23 and binary counters or flip-flops 29 to 38. The gate circuit 5 has an inverter 20, an AND gate 24, and NOR gates 27, 28. The detector circuit 6 has an inverter 21, an AND gate 25 and a delay flip-flop 39.

- 11 -

The vertical synchronising control signal forming circuit 4 also has a circuit 14 for forming a vertical synchronising control signal for a display device, the outputs of the flip-flops 29 to 38 being fed to the circuit 14. A clock signal is applied to clock input terminal 15.

Figure 7 is a timing chart showing the waveforms at points A, B, C, G, E, D in Figure 6. The 2fH signal (waveform A) is fed from the 2fH signal generating circuit 11 to the vertical synchronising control signal forming circuit 4. In the vertical synchronising control signal forming circuit 4, the 2fH signal is divided by 525 times per frame by the flip-flops 29 to 38 and the vertical synchronising control signal is formed in the circuit 14. A control signal which allows the external vertical synchronising signal to pass through the gate circuit 5 is formed by the AND gate 22. Waveform B indicates the output signal of the waveform shaping circuit 13, viz. the external vertical synchronising signal. When the control signal shown by waveform C, viz. the high-level output signal of the AND gate 22 is fed to the inverter 20 through the NOR gate 27, the output of the inverter 20 becomes high level as shown by waveform G. The inverter 20 maintains the output at high level until a control signal delivered from the detector circuit 6, viz. the high level output of the AND gate 25 is fed to the inverter 20 through the NOR gate 28. As shown by waveform E, the external vertical synchronising signal passes through the AND gate 24 during the period T_a when the output of the inverter 20

is high level. When the external vertical synchronising signal passes through the AND gate 24, the output of the OR gate 26 becomes high level and the flip-flops 29 to 38 are reset. At the same time, as the delay flip-flop 39 and the inverter 21 of the detector circuit 6 detects the fall of the external vertical synchronising signal, the output of the AND gate 25 becomes high level as shown by waveform D and the control signal from the detector circuit 6 is produced. When the control signal is delivered from the AND gate 25, the inverter 20 maintains the output of the AND gate 22 at low level during the period T_b , namely, until the output of the AND gate 22 becomes high level. As shown by waveform E, the external vertical synchronising signal is blocked by the AND gate 24 during the period T_b where the output of the inverter 20 is low level. In this way the noise component N_o as shown in waveform B is not included in the output of the AND gate 24 which prevents resetting of the flip-flops 29 to 38 by the noise component N_o and enables a stable and precise vertical synchronising control signal to be delivered from the output terminal 3 to a display device even if the external vertical synchronising signal includes a noise component.

If the external vertical synchronising signal disappears, the 2fH signal is counted 525 times per frame by the flip-flops 29 to 38 and the AND gate 23 delivers a high level output signal with the same period as that of the vertical synchronising signal to reset the flip-flops 29 to 38. Therefore, although the external



vertical synchronising signal has disappeared, it is possible to deliver the vertical synchronising control signal to a display device with the same frequency as that of the vertical synchronising signal. In this case, if the vertical synchronising control signal
5 is in synchronism with the previous external vertical synchronising signal before the external vertical synchronising signal disappeared, the vertical synchronising control signal becomes as stable and precise as in the case where the external vertical synchronising signal is present.

10 The television receiver described in relation to Figure 6 uses the M/NTSC system, viz., one of the standard systems of transmitting television signals. However, a vertical synchronising control circuit according to the present invention can also be used with other standard systems such as B/PAL system by changing the
15 vertical synchronising control signal forming circuit 4.

Further, the gate circuit 5 gives priority to the control signal from the vertical synchronising control signal forming circuit 4 over the control signal from the detector circuit 6, but a circuit construction which reverses the priority is possible. Moreover,
20 the detector circuit 6 is described above as detecting the trailing edge of the external vertical synchronising signal but it is possible to arrange that the detector circuit detects the leading edge of the external vertical synchronising signal by changing, for example, the timing of other signals. The $2f_H$ signal generating
25 circuit 11 in Figure 6 may be omitted and even so it is possible



to provide a vertical synchronising control circuit according to the present invention by varying the construction of the vertical synchronising control signal forming circuit 4.

5 A vertical synchronising control circuit according to the present invention can be used with any type of television receiver but is particularly advantageous when used in portable television receivers.



- 15 -

CLAIMS

1. A vertical synchronising control circuit comprising: a vertical synchronising control signal forming circuit for dividing a clock signal and for producing a first control signal and a vertical synchronising control signal in synchronism with an external vertical synchronising signal; a gate circuit for selectively passing said external vertical synchronising signal; and a detector circuit for producing a second control signal when the passage of the external vertical synchronising signal through the gate circuit is detected, the gate circuit being connected to receive the first and second control signals, and the vertical synchronising control signal forming circuit being connected to receive the external vertical synchronising signal that has passed through the gate circuit, the arrangement being such that the external vertical synchronising signal is allowed to pass through the gate circuit until the second control signal is fed thereto when the first control signal is fed thereto and the external vertical synchronising signal is prevented from passing through the gate circuit until the first control signal is fed thereto when the second control signal is fed thereto.
2. A vertical synchronising control circuit as claimed in claim 1 in which the vertical synchronising control signal forming circuit includes a divider circuit arranged to divide the clock signal by n , where n is an integer to produce a signal having the same frequency



- 16 -

as the external vertical synchronising signal.

3. A vertical synchronising control circuit substantially as herein described with reference to and as shown in Figures 3 to 5 of the accompanying drawings.

5 4. A television receiver having a vertical synchronising control circuit as claimed in any preceding claim.

5. A television receiver as claimed in claim 4 and substantially as herein described with reference to and as shown in Figures 6 and 7 of the accompanying drawings.
