

(15)

2116333

-1-

"A dynamic random access memory"

The present invention relates to a dynamic RAM (random access memory) which is constructed of a MOS (metal-oxide-semiconductor) integrated circuit.

5 The dynamic RAM (hereinafter referred to as a "D-RAM") includes a plurality of memory cells for storing information. The memory cell is constructed of, for example, a capacitor for storing the information in the form of charges,
10 and an insulated-gate field effect transistor (hereinafter referred to as a "MOSFET" or "MOS transistor") for selecting an address.

In the D-RAM which is formed on a semiconductor substrate, the charges stored in the
15 capacitor within the memory cell decrease with time on account of leakage current. In other words, the information stored in the memory cell is lost with the lapse of time.

In order to keep the correct information
20 stored in the memory cell, it is necessary to perform the so-called refresh operation in which the information stored in the memory cell is read out before lost, is amplified and is rewritten into the same memory cell.

The refresh operation of memory cells in a D-RAM of 64 kilobits is carried out by a circuit having a self-refresh function as described in, for example, a Japanese magazine "Denshi Gijutsu (Electronics Technology)", Vol. 23, No. 3, pp. 30-33. The D-RAM described in the literature has an external terminal for the refresh control. When a refresh control signal $\overline{\text{REF}}$ of predetermined level is applied to the external terminal, a plurality of memory cells within the D-RAM are automatically refreshed. In this case, however, the external terminal for the refresh control must be located in the D-RAM so that the cost of the device increases in correspondence with the number of external terminals.

The D-RAM of 64 kilobits referred to above is designed to operate with a single power source. Moreover, it has a reduced number of external terminals (e.g. 16) by adopting an address multiplex system. That is, it is encased in a package of 16 pins.

The memory capacities of D-RAMs have become large with the progress of semiconductor integrated circuit technology. It has accordingly become possible to manufacture a D-RAM having a large capacity of, e.g. 256 kilobits.

(17)

-3-

However, the number of bits of address signals required for the D•RAM of such large capacity as 256 kilobits increases as compared with that for the D•RAM of 64 kilobits. Therefore, even
5 when the multiplex system is adopted for the D•RAM of 256 kilobits, it is difficult to install this D•RAM on the same package of 16 pins as that of the D•RAM of 64 kilobits. More specifically, the D•RAM of 256 kilobits employing the address multi-
10 plex system requires 9 pins of address signal terminals, 2 pins of address strobe signal terminals ($\overline{RAS}$, $\overline{CAS}$), 1 pin of read/write signal terminal ($\overline{WE}$), 1 pin of output signal terminal (D_{OUT}), 1 pin of input signal terminal (D_{in}) and 2 pins of power source
15 terminals, and only these pins total 16. Therefore, the D•RAM of 256 kilobits becomes incompatible with the D•RAM of 64 kilobits and is very difficult of use on the user side.

In order to permit the self-refresh operation
20 as described above, the D•RAM needs to be supplied with the refresh control signal. Therefore, a special external circuit for forming the refresh control signal $\overline{REF}$ must be located outside the D•RAM. The increase of such external circuit is undesirable.
25 Moreover, the signal $\overline{REF}$ to be supplied to the external

terminal of the D·RAM is delayed comparatively greatly in this case, which leads to the disadvantage that the access cycle of the memory becomes longer than is necessary. More specifically, the wiring in
5 a printed circuit board on which the D·RAM is installed, has a comparatively large wiring capacitance and thus forms a heavy load. The signal delay accordingly develops in the wiring. This results in the restriction that the signal $\overline{\text{REF}}$ to be supplied to
10 the D·RAM cannot be made quickly.

A D·RAM is used as the memory of, for example, a computer. A central processing unit (hereinbelow, termed "CPU"), which is central to data processing in the computer, has its operation
15 controlled on the basis of system clocks. Accordingly, an access to the D·RAM by the CPU is permitted at a periodical timing which is determined by the operating characteristics of the CPU, the system clocks etc. As a result, the timing at which the
20 CPU can access the D·RAM is periodically set. This can be so deemed that the access to the D·RAM by the CPU is controlled by a timing signal having the certain period (a timing signal having the same period as a memory access period). Part A in Figure
25 8 of the accompanying drawings shows a waveform

diagram of a timing signal AC which stipulates the memory access period of the CPU for the D-RAM.

The start of the access to the D-RAM by the CPU is not effected when the timing signal AC is at

5 a high level, and it is allowed only when the timing signal AC falls. Information is written into or read out from the accessed memory address of the D-RAM when the timing signal AC is at a low level.

The CPU accesses the D-RAM once in one
10 or more cycles of the timing signal AC in accordance with a program. In the case where the CPU accesses the D-RAM in two cycles of the timing signal AC, by way of example the D-RAM is not accessed in the fall of the signal AC in the first cycle but is
15 accessed in the fall of the signal AC in the next cycle.

Various internal circuits in the D-RAM such as a decoder, sense amplifier, input buffer, output buffer and timing generator circuit, are
20 constructed of dynamic circuits with a view to reducing the power dissipation. Various circuit nodes in the dynamic circuits are put into precharged states in advance, and are changed to respectively proper levels in the subsequent active periods of
25 time.

The precharging time intervals of the various internal circuits in the D-RAM are set within a time interval during which the D-RAM is not accessed by the CPU. The precharging makes it possible to shorten the access time of the D-RAM. The time interval of writing or reading information in the D-RAM is determined by a time interval during which the D-RAM is accessed by the CPU. The access period of the D-RAM consisting of the two time intervals is changed in proportion to that number of cycles of the timing signal AC which is determined by the program. Accordingly, the time interval for the precharging in the access period is changed in a predetermined relationship proportional to that number of cycles of the timing signal AC which is determined by the program.

The period of the timing signal AC, namely the basic period of the memory access becomes longer in a computer of low operating speed, for example, a microcomputer, than in a large-sized computer of high operating speed because the operating speed of a CPU in the former is low and also the frequencies of system clocks are low. Accordingly, the time interval during which the D-RAM is not accessed by the CPU, in other words, the time interval which the CPU gives the D-RAM in order to precharge the internal circuits thereof, becomes longer.

(21)

- 7 -

The time interval T_p actually required for precharging the internal circuits of the D-RAM has shortened with the advancement of semiconductor integrated circuit technology. The precharging time interval T_{PR} given to the D-RAM by the CPU has therefore become longer than the time interval T_p which is actually required by the internal circuits of the D-RAM. That is, the time of the difference between both the time intervals has become long.

5 The difference time has no significance for the D-RAM and is, so to speak, a dead time.

It is an object of the present invention to overcome the above disadvantages and to provide a D-RAM in which the refresh of a plurality of memory cells is automatically effected without increasing the number of external terminals, and which is capable of performing at a high speed.

15

According to the present invention, there is provided a dynamic random access memory which has memory cells that need to be periodically refreshed, internal circuits that are brought into their precharged states and thereafter into their operating states, and an external terminal which is supplied with an address strobe signal and which is accessed in response to the address strobe signal being made a first level; said dynamic random access memory including:

20

25

(a) a pulse generator which generates refresh pulses upon detecting the address strobe signal being made a second level different from the first level; and

(b) an address counter which forms refresh address data by counting the refresh pulses output from the pulse generator;

whereby a refresh timing of the memory cells specified by said address counter is determined solely by the refresh pulses output from the pulse generator, the generator itself being rendered operative when the address strobe signal is at said second level, without the need for an external terminal dedicated exclusively to refresh control.

The automatic refresh circuit performs the operations of the first precharging the internal circuits of the D RAM (time interval T_p), subsequently refreshing desired memory cells (time interval T_R), and thereafter executing the precharging again (time interval T_p). These operations of the automatic refresh circuit are performed within the time interval T_{PR} which is afforded to the D RAM by the CPU in order to precharge the internal circuits.

Owing to the provision of the automatic refresh circuit, the refresh of the desired memory cells in the D RAM is carried out within the dead time. Therefore, the CPU can access the D RAM in the effect, as a static RAM (hereinbelow, termed "S RAM"). In addition, this D RAM dispenses with the control signal REF for the external refresh control as required in the foregoing D RAM having

2

- 9 -

the self-refresh function. Therefore, it is not necessary to provide any special external circuit outside the D-RAM. In the D-RAM, capacitances such as parasitic capacitances which are coupled to wiring leads formed in the internal circuit thereof become comparatively small because the wiring leads are fabricated by IC technology. It is therefore possible to render the transmission speeds of signals comparatively high. More specifically, in the case where the control signal $\overline{REF}$ is supplied from the external circuit to the D-RAM as stated before, the operating speed of the D-RAM is limited by the transmission speed of the control signal $\overline{REF}$ of slow transmission. Accordingly, such external control signal is dispensed with, and hence, the operating speed of the D-RAM is allowed to be raised.

In order to more reliably retain the information of the respective memory cells, the D-RAM may be so constructed as to perform an additional refresh operation also in a time interval that is determined by the combination of the state in which the D-RAM is not accessed by the CPU and the state in which the timing signal AC is held at the low level. In order to permit the additional refresh operation, a detector circuit for detecting if the access by the CPU has occurred is located within the D-RAM.

The output signal of the detector circuit is supplied to the automatic refresh circuit as, e.g. an operation control signal. In accordance with this arrangement, when it has been detected by the detector
5 circuit that the D-RAM is not accessed, the automatic refresh circuit is continuously operated.

Part B in Figure 8 of the accompanying drawings shows the waveforms of the refresh operation. The minimum value of the precharging time T_{PR} allotted
10 to the D-RAM by the CPU is stipulated by the timing signal AC. Supposing that the D-RAM has been accessed until a time t_0 , the precharging of the internal circuits thereof is started in response to the fact that the timing signal AC is brought to the high level
15 at the time t_0 . The refresh operation is started at a time t_1 at which a predetermined precharging period T_{p1} has lapsed. The refresh operation is ended at a time t_2 at which a predetermined refresh period T_R has lapsed. The precharging of the internal circuits
20 is started at the time t_2 again. The precharging operation started at the time t_2 should desirably end before a time t_3 at which a re-access to the D-RAM is permitted. Accordingly, the time interval T_{p2} from the time t_2 to the time t_3 is made longer than
25 the precharging time interval which is required by the internal circuits of the D-RAM.

In the case where the D-RAM has not been accessed

at an accessible time t_5 , that is, in the case where the D-RAM has not been accessed in spite of the change of the timing signal AC to the low level, the refresh operation is performed again as indicated by a broken line in part B of Figure 8. In this case, the precharging of the internal circuits has already ended when the timing signal AC falls from the high level to the low level. Accordingly, the automatic refresh circuit is so constructed as to immediately perform the refresh operation of the desired memory cells. In addition, the refresh operation and the precharging operation may be carried out a plurality of times within the time interval T_R . In this case, a plurality of memory cells can be refreshed within the time interval T_R .

15 The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, wherein:-

Figure 1 is a block diagram of a first preferred form of a D-RAM;

20 Figures 2 and 3 are waveform diagrams for explaining the read and write operations of the D-RAM shown in Figure 1;

Figure 4 is a block diagram showing one form of an automatic refresh circuit;

25 Figures 5 and 6 are circuit diagrams each showing other preferred forms of the essential portions of the automatic refresh circuit;

Figure 7 is a waveform diagram for explaining

the automatic refresh operation;

Figure 8 is a waveform diagram for explaining the operation of a D-RAM; and

Figure 9 is a circuit diagram of a second
5 form of a D-RAM.

Referring first to the D-RAM shown in Figure 1, the blocks enclosed with a two-dot chain line are formed on a single semiconductor substrate by known semiconductor production techniques.

10 The D-RAM has an earth terminal which is connected to the earth potential GND of the circuit, a power source terminal which is supplied with a supply voltage V_{DD} such as +5 volts, an output terminal which delivers a read data signal D_{OUT} , an input terminal
15 which is supplied with a write data signal D_{IN} a write control terminal which is supplied with a write enable signal $\overline{WE}$, a control terminal which is supplied with a column address strobe signal CAS, a control terminal which is supplied with a row address strobe
20 signal RAS, and address input terminals which are supplied with address signals A_0 to A_i or A_{i+1} to A_j in multiplexed fashion.

Although the D-RAM shown has an automatic refresh circuit 12 to be described later, it does not
25 have an external control terminal to be exclusively used for controlling the circuit 12.

The supply voltage delivered from a power source unit (not shown) is supplied across the power source terminal and earth terminal of the D-RAM.

Thus, various internal circuits constituting the D-RAM are brought into their respective operating states.

The output terminal, input terminal, control terminals and address terminals of the D-RAM are coupled to a CPU (not shown) through a controller (not shown).

The arrangement of a memory array 1 is the same as a known one, and has a plurality of memory cells arranged in a matrix. Each of the memory cells is formed into a one-MOS transistor/cell structure, whereby each of the memory cells is composed of a switching MOS transistor, and a capacitor for retaining information. The gate of the switching MOS transistor acts as the select terminal of the memory cell, and the drain acts as the data input/output terminal of the memory cell. The select terminals of the memory cells in the matrix are connected to word lines $W_0 - W_k$, while the data input/output terminals are connected to data lines $D_0, \overline{D_0} - D_m, \overline{D_m}$. The memory array 1 also includes dummy cells which determine a reference potential in reading out data from the memory cells.

The word lines $W_0 - W_k$ are respectively assigned row addresses. These word lines are connected to the output terminals of a row decoder and

driver 3.

The data lines D_0 , $\overline{D}_0 - D_m$, $\overline{D}_m$ are connected to a column switch 6 through a sense amplifier 7. One set of adjoining data lines, for example D_0 and $\overline{D}_0$ are paired. The respective pairs of data lines are assigned column addresses. The paired data lines are selected by the column switch 6.

The illustrated internal circuits, such as a row address buffer 2, the row decoder and driver 3, a column address buffer 4, a column decoder and driver 5, the sense amplifier 7, a data input buffer 10 and a data output buffer 11, are constructed of dynamic circuits in order to reduce the power dissipation of the circuits. That is, these internal circuits have circuit elements such as precharging MOS transistors (not shown) which are dynamically driven. Precharge pulses for bringing these internal circuits into their precharged states, and control pulses for bringing them into their operating states are delivered from a signal generator 8.

The signal generator 8 delivers the precharge pulses to be supplied to the internal circuits, in response to the change of the row address strobe signal $\overline{RAS}$ from its low level to its high level, this signal being supplied to the external terminal of the memory chip. The signal generator 8 also delivers the

control pulses in response to the row address strobe signal $\overline{\text{RAS}}$ and the column address strobe signal $\overline{\text{CAS}}$.

Figures 2 and 3 are waveform diagrams showing the operations of the read cycle and write cycle of the D-RAM shown in Figure 1, and the operation of the D-RAM will now be described with reference to Figures 2 and 3.

First, the levels of the respective row address signals $A_0 - A_i$ are set at such levels in order to select the row address of a desired memory cell within the memory array 1. Thereafter, the $\overline{\text{RAS}}$ signal is made the low level. The signal generator circuit 8 (hereinafter referred to as "SG 8") provides a control signal ϕ_{ARO} in response to the fall of the $\overline{\text{RAS}}$ signal. When the signal ϕ_{ARO} has been provided, the row address buffer 2 (hereinafter referred to as "R-ADB") which has been previously held in the precharged state is brought into the operating state. As a result, the row address signals $A_0 - A_i$ are applied to the R-ADB 2 and latched therein. In response to the row address signals $A_0 - A_i$, the R-ADB 2 generates internal address signals $a_0, \overline{a_0} - a_i, \overline{a_i}$ of true and false levels. The reason why the $\overline{\text{RAS}}$ signal is made later than the row address signals $A_0 - A_i$ is in order to ensure a reliable supply of the row address signals

$A_0 - A_i$ to the R-ADB.

Next, the signal ϕ_{AR} delayed by a predetermined period of time with respect to the $\overline{RAS}$ signal is applied to the R-ADB. Upon the generation of the signal ϕ_{AR} , the internal address signals $a_0, \overline{a_0} - a_i, \overline{a_i}$ produced by the R-ADB are transmitted to the row decoder and driver circuit 3 (hereinafter referred to as "R-DCR"). The R-DCR 3 decodes the internal address signals $a_0, \overline{a_0} - a_i, \overline{a_i}$. Amongst the decoded signals of the R-DCR 3, only those which are to be selected remain at the high level, and the others which are not to be selected are brought to the low level.

Subsequently, a signal ϕ_X which is delayed by a predetermined period of time with respect to the signal ϕ_{AR} is delivered from the SG 8. Upon the generation of the signal ϕ_X , the decoded signals formed by the R-DCR 3 are transmitted to the row address lines of the memory array 1 (hereinafter referred to as "M-ARY"). The reason why the signal ϕ_X is delayed with respect to the signal ϕ_{AR} is in order to operate the R-DCR 3 after the operation of the R-ADB 2 has ended. In this way, the row address in the M-ARY 1 is set. That is, one row address line in the M-ARY 1 is selected by one high-level signal amongst the 2^{i+1} output signals of

31

the R-DCR 3.

Next, data signals corresponding to the information of "1" or "0" read out from the respective memory cells, which are connected to the selected single row address line in the M-ARY 1, are amplified by the sense amplifier 7 (hereinafter referred to as "SA 7"). The amplifying operation of the SA 7 is started upon the generation of the signal ϕ_{PA} .

At a correct time illustrated by the waveform E in Figure 2, the respective levels of the column address signals $A_{i+1} - A_j$ are set at such levels as select the column address of the desired memory cell. Thereafter, when the $\overline{CAS}$ signal has been made the low level so as to provide a signal ϕ_{ACO} from the SG 8, the column address signals $A_{i+1} - A_j$ are applied to the column address buffer (hereinafter referred to as "C-ADB") 4 and latched therein. The reason why the $\overline{CAS}$ signal is made later than the column address signals $A_{i+1} - A_j$ is in order to reliably supply the C-ADB with the column address signals as the column address in the memory array.

Subsequently, a signal ϕ_{AC} delayed with respect to the $\overline{CAS}$ signal is delivered from the SG 8, and it is applied to the C-ADB 4. Upon the generation of the signal ϕ_{AC} , the C-ADB 4 transmits internal address signals $a_{i+1}, \overline{a_{i+1}} - a_j, \overline{a_j}$

corresponding to the column address signals, to the column decoder and driver circuit 5 (hereinafter referred to as "C-DCR 5"). The C-DCR 5 generates 2^{j+1} decoded signals by an operation similar to that of the R-DCR 3. Amongst the decoded signals, one which corresponds to the combination of the internal address signals is brought to the high level. Next, a signal ϕ_Y delayed with respect to the signal ϕ_{AC} is applied to the C-DCR 5. Upon the generation of the signal ϕ_Y , the decoded signals are delivered from the C-DCR 5 and transmitted to the multiplexer or column switch (hereinafter, termed "C-SW") 6. In this way, the column address in the M-ARY 1 is set, i.e. one of the bit lines in the M-ARY 1 is selected by the C-SW 6.

One memory address in the M-ARY 1 is set by such setting of the row address and the column address.

Next, the read and write operations for the set address will be described in greater detail.

A read mode is specified by the high level of the $\overline{WE}$ signal. The $\overline{WE}$ signal is made the high level before the $\overline{CAS}$ signal is made the low level. Preparations for the read operation are made by bringing the $\overline{WE}$ signal to the high level. Accordingly, when the $\overline{WE}$ signal has been brought to the high level

in advance, the read operation gets ready before one address of the M-ARY 1 is set by making the $\overline{\text{CAS}}$ signal the low level. As a result, the period of time for starting the read operation can be shortened.

- 5 When a signal ϕ_{Op} which is a CAS-group signal has been provided from the SG 8, an output amplifier (not shown) which is included in the data output buffer circuit 11 (hereinafter referred to as "DOB") is responsively activated. Information read out from
- 10 the set address, namely, information supplied through the C-SW is amplified by the activated output amplifier. The amplified information is delivered through the DOB 11 to the data output (D_{out}) terminal. Thus, the read operation is effected.
- 15 When the $\overline{\text{CAS}}$ signal has become the high level, the read operation ends.

- A write mode is specified by the low level of the $\overline{\text{WE}}$ signal. A signal ϕ_{RW} is brought to the high level by the $\overline{\text{WE}}$ signal of low level and the
- 20 $\overline{\text{CAS}}$ signal of low level. The signal ϕ_{RW} is applied to the data input buffer circuit 10 (hereinafter referred to as "DIB"). The DIB is activated by the signal ϕ_{RW} of high level, and then transmits write data from the input data (D_{in}) terminal to the C-SW.
- 25 The write data is transmitted to the set address of the M-ARY 1 through the C-SW. As a result, the

write operation is performed.

In the write operation, the DOB is inactivated by being supplied with the inverted signal of the signal ϕ_{RW} , namely, the signal $\overline{\phi_{RW}}$ of low level. Thus,
5 the data in the write operation is prevented from being read out.

The respective clocks signals ϕ_X , ϕ_Y are formed on the basis of the address strobe signals ($\overline{RAS}$ signal, $\overline{CAS}$ signal) in the SG8 which receives
10 these address strobe signals as previously stated. The clock signal ϕ_{RW} is formed on the basis of the $\overline{WE}$ signal and the output signal from the SG 8 in the read/write clock pulse generator (R/W-SG) 9.

The D-RAM described above is provided with
15 the automatic refresh circuit 12 (hereinafter referred to as "REF 12") which does not require any increase in the number of external terminals of the D-RAM.

The REF 12 forms clock and address signals necessary for the refresh operation, on the basis
20 of the $\overline{RAS}$ signal amongst the address strobe signals supplied from the external terminals.

A block diagram showing a preferred form of the REF 12 is shown in Figure 4. The operations of the REF 12 will now be described with reference
25 to Figure 4.

The $\overline{RAS}$ signal supplied from the external

35

- 21 -

terminal is applied to a pulse generator circuit PG. The pulse generator PG forms a pulse ϕ_1 which is produced with a delay of the period of time required for precharging the internal circuits of the D-RAM, with respect to the rise timing of the $\overline{\text{RAS}}$ signal to the precharged level (the level of the supply voltage V_{DD}) and which is brought to its reset level in synchronism with the fall of the $\overline{\text{RAS}}$ signal. The form of circuit shown is constructed so that an internal address strobe signal RAS_1 (the inverted signal of the $\overline{\text{RAS}}$ signal) formed in the SG 8 is supplied to the pulse generator PG in order to reset the pulse ϕ_1 .

The pulse ϕ_1 is used as an operation start signal for an oscillator circuit OSC. The oscillator OSC forms a pulse ϕ_2 which sets a refresh period. The period of the pulse ϕ_2 is set so as to have a predetermined ratio of division with respect to the memory access period T which has been or will be described with reference to Figures 7 and 8. The pulse ϕ_2 is transmitted to a clock pulse generator SG' and a refresh address counter COUNT.

When the pulse ϕ_2 has been brought to the high level, the clock pulse generator SG' forms clock pulses required for performing the refresh operation, namely, clock pulses ϕ_X' and ϕ_{PA}' corresponding to the respective clock pulses ϕ_X and

ϕ_{PA} used in the ordinary operation cycles. The clock pulses ϕ_X' and ϕ_{PA}' are respectively supplied to the R-DCR 3 and the SA 7 shown in Figure 1.

The number of the pulses ϕ_2 to be supplied to the counter COUNT corresponds to the number of refresh cycles. The number of the pulses counted by the counter corresponds to a refresh address. Accordingly, the counter COUNT successively increments the refresh address by counting the refresh cycles.

10 The count output signals of the counter COUNT are transmitted to the address input terminals of the R-DCR 3. The counter COUNT is constructed of a counter circuit of the scale of, e.g. 2^{i+1} .

A multiplexer (not shown) for selecting the address signals delivered from the R-ADB 2 or the address signals delivered from the counter COUNT is located on the address input terminal side of the R-DCR 3. The multiplexer for the R-DCR 3 has its operation controlled by the address strobe signal $\overline{RAS}$.

20 $\overline{RAS}$. The counter COUNT has its address signals transmitted to the R-DCR 3 when the address strobe signal $\overline{RAS}$ is at the high level. On the other hand, the address signals of the R-ADB 2 are transmitted to the R-DCR 3 when the address strobe signal $\overline{RAS}$ is

25 at the low level.

Figure 5 shows a circuit diagram of a

31

- 23 -

preferred form of the pulse generator PG as well as the oscillator OSC. A fundamental circuit arrangement constructed of N-channel MOS transistors is shown in order to simplify the explanation. When the circuit arrangement is to be realized as an integrated circuit, various modifications may be made.

The pulse generator PG comprises the following elements. A MOS transistor Q_1 which has the $\overline{RAS}$ signal applied to its gate, and a capacitor C_1 constitute an integrator circuit. The output signal A of the integrator circuit is applied to the gate of a driving MOS transistor Q_5 . A predetermined delay time for the $\overline{RAS}$ signal is set by appropriately setting the time constant of the integrator circuit and the threshold voltage V_L of the driving MOS transistor Q_5 . Connected to the drain of the driving MOS transistor Q_5 is a load MOS transistor Q_2 which is driven by the $\overline{RAS}$ signal. The output signal B of the inverter circuit (Q_5, Q_2) is applied to an inverter circuit which comprises a driving MOS transistor Q_6 and a load MOS transistor Q_3 . The output terminal of this inverter circuit (Q_6, Q_3) delivers the pulse ϕ_1 which rises with the delay of the period of time required for precharging the internal circuits of the D-RAM, relative to the timing of the rise of the $\overline{RAS}$ signal to the precharged

level. In order to synchronize the fall of the pulse ϕ_1 with the $\overline{\text{RAS}}$ signal, there are provided a resetting MOSFET Q_4 which is connected between the capacitor C_1 and earth of the circuit and whose gate is supplied
5 with the RAS_1 signal, and a resetting MOSFET Q_7 which is connected in parallel with the driving MOS transistor Q_6 and whose gate has the RAS_1 signal applied thereto.

As previously described, the RAS_1 signal is that inverted signal of the $\overline{\text{RAS}}$ signal which has been
10 formed in the SG 8.

The oscillator circuit OSC comprises three inverter circuits which are connected in the form of a ring. The pulse ϕ_1 is applied to the gates of load MOS transistors Q_8 to Q_{10} in the respective
15 inverter circuits. Accordingly, the oscillator OSC forms a controlled oscillator circuit which has the start and stop of its oscillating operation controlled by the pulse ϕ_1 . Capacitors C_2 to C_4 for attaining a predetermined oscillation period are
20 coupled to the respective inverter circuits. The oscillator OSC further includes a resetting MOS transistor Q_{14} which has the RAS_1 signal applied to its gate, in order to reset the oscillation output pulse ϕ_2 of the oscillator in synchronism with the
25 $\overline{\text{RAS}}$ signal.

Next, the operation of the circuit shown

in Figure 5 will be described with reference to the waveform diagrams of Figure 7.

First, the $\overline{\text{RAS}}$ signal rises to the high level, whereupon the preceding memory cycle (memory access period) is ended, and the next memory cycle (memory access period) T is started. In response to the rise of the $\overline{\text{RAS}}$ signal, the integration output signal A rises as shown in waveform B (signal A) in Figure 7. When the integration output signal A has reached the logic threshold voltage V_L of the MOS transistor Q_5 , the pulse ϕ_1 rises as shown in waveform C (signal ϕ_1) in Figure 7. Upon the change of the pulse ϕ_1 to the high level, the oscillator OSC is activated. As a result, the pulse ϕ_2 is formed as shown in waveform D (signal ϕ_2) in Figure 7, owing to the rise of the pulse ϕ_1 to the high level.

The rise characteristics and period of the pulses ϕ_2 are determined by the conductance characteristics of the respective MOS transistors and the capacitances of the capacitors constituting the oscillator OSC. For example, the fast rise of the pulse ϕ_2 is permitted by raising the charging rate of the capacitor C_4 . The high level duration of the pulse ϕ_2 is determined by the discharge rate of the capacitor C_2 which is decided by a driving

MOS transistor Q_{11} , the charging rate of the capacitor C_3 which is decided by the load MOS transistor Q_9 , and the threshold voltages of the MOS transistors.

5 The pulse ϕ_2 has low level and high level durations T_1 to T_6 which lie within the memory cycle (memory access period) T .

 The pulse ϕ_2 is held at the low level in the time interval T_1 . Within this time interval T_1 ,
10 namely, within the response delay time of the pulse generator PG and the oscillator OSC, the internal circuits are precharged.

 The pulse ϕ_2 is held at the high level in the time interval T_2 . In this time interval T_2 , the
15 refresh operation is performed. More specifically, the address signals from the counter circuit COUNT shown in Figure 4 are applied to the R-DCR 3 shown in Figure 1. The R-DCR 3 receives the address signals and the signal ϕ_X' delivered from
20 the SG' within the REF circuit, and thereby selects a group of memory cells determined by the address signals. Information from the selected group of memory cells is applied to the sense amplifier SA shown in Figure 1. The sense amplifier SA
25 amplifies the information in response to the signal ϕ_{PA}' delivered from the SG'. The amplified information is written into the group of memory cells again. When the pulse ϕ_2 falls, the counter

(241)

circuit COUNT shown in Figure 3 performs the counting operation in synchronism with the falling edge of the pulse. As a result, the count value of the counter COUNT is updated by +1 (or -1).

5 The pulse ϕ_2 is again brought to the low level in the time interval T_3 . In response thereto, the circuits of the R-DCR 3, the SA 7, operated in the refresh operation are precharged.

10 In the case where the read or write is performed in the memory cycle (memory access period) T , the $\overline{\text{RAS}}$ signal is changed to the low level as indicated by a solid-line curve $\overline{\text{RAS}}$ in Figure 7. It should be noted that the precharging of the internal circuits started in the time interval T_3
15 must be over when the $\overline{\text{RAS}}$ signal changes to the low level. Therefore, the period of the pulses ϕ_2 is set in conformity with the memory cycle.

 When the $\overline{\text{RAS}}$ signal is caused to fall, the pulses ϕ_1 and ϕ_2 are responsively reset to the low
20 level. In consequence, the signals ϕ_X' and ϕ_{PA}' are no longer provided from the REF circuit. The $\overline{\text{WE}}$ signal and the $\overline{\text{CAS}}$ signal, which are required for the write or read operation, are changed subsequently to the fall of the $\overline{\text{RAS}}$ signal. Upon the changes
25 of these signals, the signals necessary for the write operation or the signals necessary for the read operation are provided from the R/W SG 9 and

the SG 8 shown in Figure 1. At this time, the address multiplexer located on the address input terminal side of the R-DCR 3 selects the address signals supplied from the address buffer R-ADB, because the $\overline{\text{RAS}}$ signal is at the low level. The memory cell specified by the address signals $A_0 - A_j$ is selected from within the memory array M-ARY, and information is written into or read out from the memory cell. That is, the write or read operation of information into or from the memory cell, explained with reference to Figure 2 or 3 before, is carried out.

On the other hand, in the case where the D-RAM is not selected in the memory cycle (memory access period) T , the $\overline{\text{RAS}}$ signal is held at the high level as it is, as indicated by a broken line in Figure 7. In this case, the oscillator circuit OSC continues to oscillate. To this end, the pulse ϕ_2 is caused to rise to the high level in the time interval T_4 again. Then, the refresh operation for a group of memory cells specified by the row address in the counter count subjected to +1 (or -1) is carried out similarly to the case of the time interval T_2 .

In the time interval T_5 during which the pulse ϕ_2 is held at the low level again, the precharging operation of the internal circuits of

the D-RAM is performed again similarly to the case of the time interval T_3 . The refresh operation of a group of memory cells having the row address further subjected to +1 (or -1), namely the updated refresh address, is performed in the time interval T_6 . Then, the circuit operation shifts to the next memory cycle.

Thenceforth, similar operations are repeated. Accordingly, in the case where the read or write operation is performed in a certain memory cycle (memory access period), only one refresh operation is carried out, and in the case where the read or write is performed, three refresh operations (of three different row addresses) are carried out.

Figure 6 is a circuit diagram of a modification of the fundamental circuit arrangement shown in Figure 5.

The circuit arrangement shown in Figure 6 comprises a pulse generator PG which is similar to the pulse generator PG shown in Figure 5, that is which consists of MOS transistors Q_1 to Q_7 , and a delay circuit DELAY which is coupled on the output side of the pulse generator PG. An output signal delayed by the delay circuit DELAY is fed back to the pulse generator PG. The output signal of the delay circuit DELAY is fed back to a driving

transistor Q_{16} which is arranged in parallel with a capacitor C_1 in the pulse generator PG. Owing to the feedback connection, the pulse generator PG and the delay circuit DELAY constitute in effect, a
5 controlled oscillator circuit. The period of the pulses ϕ_2' to be delivered from the circuit arrangement shown in Figure 6 is determined by a lag time which is set by an integrator circuit consisting of the load MOS transistor Q_1 and the capacitor C_1 ,
10 and a delay time which is set by the delay circuit DELAY.

Where the circuit shown in Figure 6 is used, the time intervals T_1 , T_3 and T_5 are set by means of the integrator circuit, and the time intervals
15 T_2 , T_4 and T_6 are set by means of the delay circuit.

With this embodiment, the automatic refresh operation can be effected without providing any external terminal therefor. Therefore, by way of example, a D-RAM of 256 kilobits with the
20 automatic refresh function added thereto can be installed on a package of 16 pins.

In addition, in the case of a D-RAM of 64 kilobits, there is one surplus pin after the refresh function has been added to the D-RAM. By
25 utilizing this pin, therefore, another new function can be added.

Furthermore, the refresh operation is effected in accordance with the pulse ϕ_2 formed by the internal circuit. Therefore, the time intervals T_1 , T_2 can be set depending upon the operating speeds of the respective internal circuits, and the memory cycle T can operate more quickly.

The memory cycle (memory access period) depends upon the machine cycle of the central processing unit (CPU) of the computer in which the D-RAM is used. It is accordingly possible to obtain a D-RAM which can satisfactorily cope with enhancing the operating speed of a one-chip CPU such as, for example, a microcomputer. Moreover, since the control signal REF as in the prior art is dispensed with, the memory system control circuit can be simplified, and the D-RAM can be used in substantially the same manner as that of a static RAM.

When it is intended to use the D-RAM as the memory of a large-sized computer of high operating speed, the automatic refresh operation described above cannot, in effect, be satisfactorily performed. In the large-sized computer, the memory access period is set to be short since a high operating speed is required. Accordingly, the time interval, which is allotted to the D-RAM by the CPU in order to precharge the internal circuits of the D-RAM, is shorter than

that which is really required for precharging the internal circuits of the D-RAM. Within such a short time interval, it is difficult to execute the refresh operation.

However, this does not always mean that the
5 above described D-RAM cannot be applied to high-speed uses.

The D-RAM having included in the REF circuit, the circuit for detecting the pulse width of the $\overline{\text{RAS}}$ signal as shown in Figure 5 or Figure 6, that is, the
10 circuit which consists of the integrator circuit comprising the MOSFETs Q_1 , Q_4 and the capacitor C_1 , and the MOSFET Q_5 receiving the output signal of the integrator circuit, can be used as the memory of the large-sized computer of high operating speed.

15 In order to permit such uses, the detectable time interval by the detector circuit is set to be slightly longer than the time interval which is really required for precharging the internal circuits of the D-RAM. The detection time of the
20 detector circuit is set by the integrator circuit and the MOSFET Q_5 receiving the output thereof.

With this measure, in the application to the microcomputer of low operating speed, the signal ϕ_1 is delivered from the PG when the $\overline{\text{RAS}}$ signal is at
25 the precharged level. As a result, the automatic refresh is carried out. In contrast, in the

the application to the large-sized computer of high operating speed, the signal ϕ_1 is not delivered from the PG. Accordingly, the automatic refresh operation fails to proceed. In this case, the D-RAM is usable
5 in similar manner to the conventional D-RAM. That is, in the above described D-RAM, the constituent memory cells are refreshed by, e.g. the so-called $\overline{\text{RAS}}$ only refresh in the same manner as in the conventional D-RAM.

10 Therefore, the above described D-RAM has very wide applications.

A number of modifications will now be described.

By way of example, in Figure 7, the pulse
15 ϕ_2 for the refresh operation may be a pulse which is at the low level during the time intervals T_3 , T_4 and T_5 . Alternatively it may be a pulse which becomes the high level during only the time interval T_2 . Such pulses can be formed, for example, in the way
20 that the change to the high level in the time interval T_4 or in the time intervals T_4 and T_6 is limited by employing the pulse ϕ_2 of the oscillator circuit OSC and by means of a logic gate circuit, a counter circuit as predetermined.

25 Further, in Figure 4, the counter circuit COUNT for the refresh operation may be made a 2^{i+2} -scale

circuit, which provides address signals for the refresh operation in only the first half of one circulation of counting.

In this case, the generation of the pulse ϕ_2 may be inhibited by the most significant bit signal of the counter circuit. This brings forth the advantage that current consumption attributed to the unnecessary execution of the refresh operation in relation to, e.g. the memory cycle can be reduced.

It also allows one to provide a pulse width detector circuit constructed of a timer circuit, so as to switch the refresh periods upon detecting the fact that the memory retention status has been held for a long time. That is, timings may be switched so as to omit the refresh operations of the time intervals T_4 and T_6 in Figure 7. Also in this case, a reduction in power consumption can be achieved, which reduction is attributed to the fact that the refresh operation is executed unnecessarily.

The system structure of the D-RAM can also be modified in a number of ways.

Figure 9 is a block diagram of a modified form of the automatic refresh circuit 12. Although the automatic refresh circuit 12 of this embodiment corresponds approximately to that shown in the embodiment of Figure 4, it does not include the signal

generator SG' as shown in Figure 4.

A pulse generator circuit PG, an oscillator circuit OSC and a counter circuit COUNT are the same as those in Figure 4. The output signal ϕ_2 of the oscillator OSC is supplied to the signal generator 8.

The signal generator 8 has its internal circuits constructed appropriately so that it regards the output signal ϕ_2 of the oscillator OSC as a pseudo row address strobe signal. In addition, the operation of the data output buffer DOB shown in Figure 1 is not required during the refresh operation. Accordingly, the signal generator 8 has a suitable inhibitor circuit in order to inhibit the delivery of the signal ϕ_{Op} even when it is supplied with the pseudo address strobe signal.

The operations of the circuit arrangement in Figure 9 resemble those of the circuit arrangement in Figure 4.

When the row address strobe signal $\overline{RAS}$ supplied to the external terminal of the circuit arrangement has been brought from the low level to the high level, the signal generator 8 generates precharging pulses for putting the internal circuits, shown in Figure 1, into their precharged states. The signal RAS_1 , which is brought to the low level in response to the change of the row address strobe signal $\overline{RAS}$ to the high level, is provided from the

signal generator 8. In response to them, the pulse generator PG delivers the signal ϕ_1 similar to the signal ϕ_1 in Figure 4. The oscillator OSC delivers the refresh pulse ϕ_2 of high level in response to the
5 output signal ϕ_1 of the pulse generator PG.

In response to the refresh pulse ϕ_2 , the signal generator 8 delivers the control pulses ϕ_X , ϕ_{PA} . In this case, the control pulse ϕ_{OP} is not delivered as described above. The refresh operation
10 is executed by the control pulses ϕ_X , ϕ_{PA} .

After a predetermined time interval which is decided by the oscillator OSC, the refresh pulse ϕ_2 is again brought to the low level. In response to this change of the refresh pulse ϕ_2 from the high
15 level to the low level, the signal generator 8 produces the precharging pulses for putting the internal circuits, shown in Figure 1, into their precharged states

If, in spite of the lapse of a predetermined
20 time interval since the start of the precharging operation, the D-RAM is not accessed, that is, the external row address strobe signal $\overline{RAS}$ is not made the low level, the refresh pulse ϕ_2 of high level is delivered from the oscillator OSC again. In response
25 thereto, the refresh operation is restarted.

In the case where the external row address

strobe signal $\overline{RAS}$ has been changed from the high level to the low level, appropriate control pulses are responsively provided from the signals generator 8 as in the embodiment of Figure 4.

- 5 In order to cause the pulse generator PG to respond to only the external row address strobe signal, the signal RAS_1 to be provided from the signal generator 8 is made responsive to the external row address strobe signal, but not to the refresh pulse
- 10 ϕ_2 .

The circuit arrangement of the embodiment shown in Figure 9 does not need the signal generator SG' as shown in Figure 4, which means that it is possible to reduce the number of circuit elements.



(52)

CLAIMS.

1. A dynamic random access memory which has memory cells that need to be periodically refreshed, internal circuits that are brought into their precharged states and thereafter into their operating states, and an external terminal which
5 is supplied with an address strobe signal and which is accessed in response to the address strobe signal being made a first level; said dynamic random access memory including:
 - (a) a pulse generator which generates refresh pulses upon detecting the address strobe signal being made a second
10 level different from the first level; and
 - (b) an address counter which forms refresh address data by counting the refresh pulses output from the pulse generator;whereby a refresh timing of the memory cells specified
15 by said address counter is determined solely by the refresh pulses output from the pulse generator, the generator itself being rendered operative when the address strobe signal is at said second level without the need for an external terminal dedicated exclusively to refresh control.
- 20 2. A dynamic random access memory according to claim 1, further including:
 - (c) a timing pulse generator which generates precharging pulses for bridging said internal circuits into their precharged states, when the address strobe signal is made
25 the second level, and which generates control pulses for bringing said internal circuits into their operating states, when the address strobe signal is made the first level.

(43)



- 39 -

3. A dynamic random access memory according to claim 2, wherein said pulse generator which generates the refresh pulses comprises a first circuit which detects the second level of the address strobe signal, and a second circuit which is started by a detection output of said first circuit and which generates the refresh pulse at that time.
4. A dynamic random access memory according to claim 3, wherein said second circuit comprises a controlled oscillator circuit whose start and stop are controlled by the detection output of said first circuit, whereby the refresh pulses are periodically generated in a time interval during which the address strobe signal is made the second level.
5. A dynamic random access memory according to claim 4, wherein said first circuit includes a delay circuit which is constituted by an integrator circuit, whereby the refresh pulses are generated after end of a precharging operation of said internal circuits which is started when the address strobe signal has been made the second level.
6. A dynamic random access memory according to claim 5, wherein a time interval between one refresh pulse to be delivered from said controlled oscillator circuit and another to be subsequently delivered is made longer than a time interval which is required for precharging said internal circuits.



54

- 40 -

7. A dynamic random access memory according to claim 2, wherein said pulse generator which generates the refresh pulses includes a delay circuit which is constituted by an integrator circuit, whereby the
5 refresh pulses are generated after the end of a precharge operation of said internal circuits which is started when the address strobe signal is made the second level.
8. A dynamic random access memory according to
10 claim 2, wherein said pulse generator which generates the refresh pulses is constituted by a controlled oscillator circuit whose operation is controlled by the address strobe signal.
9. A dynamic random access memory constructed
15 substantially as herein described with reference to and as illustrated in the accompanying drawings.
-