

Furthermore, the BOX dissolution reaction is generally known to be purely time-controlled, and the speed of the reaction is known to be temperature-dependent. As a consequence, the final dissolved thickness depends on the local temperature, which is known to result in additional non-uniformities.

- 5 In metal-oxide-semiconductor (CMOS) integrated technology, high permittivity or high dielectric constant (high-k) materials are typically used for the oxide gate dielectric in order to prevent leakage currents. Interfacial layer scavenging, i.e. depositing an oxygen scavenging layer directly on the oxide gate dielectric, is a known alternative to using even higher-k oxides (*“Ultimate Scaling of High-k Gate Dielectrics: Higher-k or Interfacial Layer Scavenging”* by T. Ando; *Materials*, 2012, Vol. 5, p. 478 – 500).
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An example of interfacial layer scavenging can be found in US 2010/0244206 A1, which discloses a method of forming a high-k metal gate transistor (MOSFET) having interface nitridation to modulate threshold voltage and improve drive current. This document discloses a high-k dielectric gate structure comprising a substrate, a nitridized interfacial layer on the substrate, a high-k dielectric layer on the nitridized interfacial layer, and an oxygen scavenging layer on the high-k dielectric layer. In the method disclosed therein, an anneal is performed after depositing the oxygen scavenging layer on the high-k dielectric layer.

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In view of the aforementioned problems, embodiments of the present invention seek to provide an improved BOX dissolution method, allowing in particular to perform the BOX dissolution annealing step also when the SOI wafer has a thin silicon layer, that is when the silicon layer of the SOI wafer has a thickness below 150 nm or even less, and possibly without the need of an oxygen-tight furnace or of a specifically designed high temperature furnace.

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25 An aspect of the present disclosure relates a method of manufacturing a silicon-on-insulator wafer comprising providing a silicon-on-insulator wafer. The silicon-on-insulator wafer can include a silicon layer, a carrier substrate a buried oxide layer between the silicon layer and the carrier substrate and an oxygen scavenging layer on or over the silicon layer. The method of manufacturing the silicon-on-insulator wafer also comprises annealing the silicon-on-insulator wafer and at least partially dissolving the buried oxide layer.

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There is also disclosed a method for dissolving a buried oxide in a silicon-on-insulator wafer, comprising a step of providing a silicon-on-insulator wafer having a silicon layer

attached to a carrier substrate via a buried oxide layer, and subsequent step of annealing said silicon-on-insulation wafer to at least partially dissolve the buried oxide layer. According to the present invention, the method further comprises a step of providing an oxygen scavenging layer on or over the silicon layer before the annealing step.

- 5 Accordingly, the proposed inventive method is based on depositing an oxygen scavenging layer on top of the silicon layer of a SOI wafer before the BOX dissolution anneal. As mentioned above, interfacial layer scavenging is known in relation to metal-oxide-

Claims

1. A method of manufacturing a silicon-on-insulator wafer, comprising:
providing a silicon-on-insulator wafer including:
a silicon layer,
a carrier substrate,
a buried oxide layer between the silicon layer and the carrier substrate, and
an oxygen scavenging layer on or over the silicon layer; and
annealing the silicon-on-insulator wafer and at least partially dissolving the buried oxide layer.
2. The method of claim 1, wherein the silicon layer has a thickness (h_{Si}) of about 150 nm or less.
3. The method of claim 2, wherein the silicon layer has a thickness (h_{Si}) of about 50 nm or less.
4. The method of claim 3, wherein the silicon layer has a thickness (h_{Si}) of about 25 nm or less.
5. The method of claim 2, wherein the silicon layer is a strained layer.
6. The method of claim 5, wherein the oxygen scavenging layer has a thickness (h_{scav}) adapted for dissolving at least a predetermined thickness of the buried oxide layer to be dissolved.
7. The method of claim 6, wherein the oxygen scavenging layer comprises substoichiometric HfO_x , wherein $x < 2$.
8. The method of claim 7, wherein the oxygen scavenging layer comprises a material chosen from among a lanthanide metal, a rare earth metal, a titanium rich (Ti-rich) titanium nitride (TiN), Group 2 elements, and Group 3 elements.

9. The method of claim 8, further comprising providing a diffusion barrier layer on top of the oxygen scavenging layer and/or between the oxygen scavenging layer and the silicon layer prior to annealing the silicon-on-insulator wafer and at least partially dissolving the buried oxide layer.
10. The method of claim 9, wherein the diffusion barrier layer is provided on top of the oxygen scavenging layer, and wherein the diffusion barrier layer is an oxygen diffusion barrier layer.
11. The method of claim 10, wherein when the diffusion barrier layer is provided directly on top of the oxygen scavenging layer, and wherein the diffusion barrier layer is a layer of a silicon nitride.
12. The method of claim 9, wherein the diffusion barrier layer is provided between the oxygen scavenging layer and the silicon layer, and wherein the diffusion barrier layer comprises a material having a composition preventing diffusion of an oxygen scavenging element of the oxygen scavenging layer into the silicon layer.
13. The method of claim 12, wherein the diffusion barrier layer comprises a layer of stoichiometric HfO_2 .
14. The method of claim 1, wherein annealing the silicon-on-insulator wafer comprises annealing the silicon-on-insulator wafer in a standard furnace that is not oxygen-tight.
15. The method of claim 1, wherein providing the silicon-on-insulator wafer comprises transferring the silicon layer onto the carrier substrate using a layer transfer technique by ion implantation.
16. The method of claim 1, wherein the silicon layer is a strained layer.

17. The method of claim 1, wherein the oxygen scavenging layer has a thickness (h_{scav}) adapted for dissolving at least a predetermined thickness of the buried oxide layer to be dissolved.
18. The method of claim 1, wherein the oxygen scavenging layer comprises substoichiometric HfO_x , wherein $x < 2$.
19. The method of claim 1, wherein the oxygen scavenging layer comprises a material chosen from among a lanthanide metal, a rare earth metal, a titanium rich (Ti-rich) titanium nitride (TiN), Group 2 elements, and Group 3 elements.
20. The method of claim 1, further comprising providing a diffusion barrier layer on top of the oxygen scavenging layer and/or between the oxygen scavenging layer and the silicon layer prior to annealing the silicon-on-insulator wafer and at least partially dissolving the buried oxide layer.