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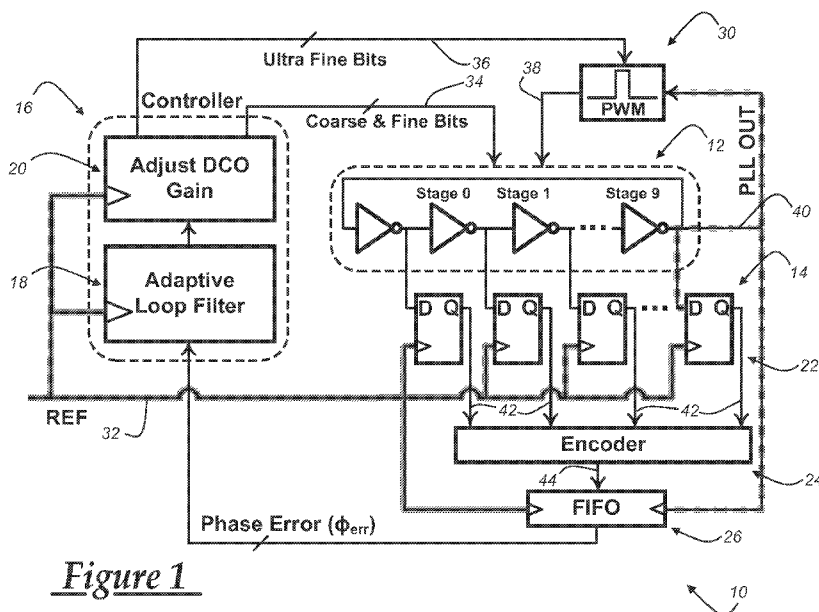
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(54) Title: AUTOMATICALLY PLACED-AND-ROUTED ADPLL WITH PWM-BASED DCO RESOLUTION ENHANCEMENT



(S7) Abstract: An all digital phase-locked loop (PLL) and a method of controlling the PLL is provided. The method includes the steps of receiving a reference signal (f_{REF}) at a controller and a time-to-digital converter (TDC), the controller and TDC being coupled to multiple tunable delay elements; receiving at the multiple tunable delay elements a first signal input via the controller and a pulse-width modulation (PWM) circuit; providing an PLL output (f_{DCO}) to the TDC at least partially based on the first signal input; and generating a phase error output (Φ_{ERR}) based on the reference signal (f_{REF}) and the PLL output (f_{DCO}), wherein the phase error output (Φ_{ERR}) is provided as feedback to the controller to control the PLL output (f_{DCO}).