

SEMICONDUCTOR DEVICE INCLUDING DATA STORAGE PATTERN

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This patent application claims benefit of priority to Korean Patent Application
5 No. 10-2019-0110621, filed on 6 September 2019, in the Korean Intellectual Property
Office, the disclosure of which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] The present inventive concept relates to a semiconductor device, and more
10 particularly, to a semiconductor device including a data storage pattern, and a method of
forming the same.

BACKGROUND

[0003] In order to increase the price competitiveness of products, there is growing
15 demand for improving the degree of integration of a semiconductor device. In order to
improve the degree of integration of a semiconductor device, a semiconductor device
having three-dimensional array of memory cells, instead of two-dimensional array of
memory cells, has been proposed.

SUMMARY

[0004] An aspect of the present inventive concept is to provide a semiconductor device
capable of improving a degree of integration.

[0005] An aspect of the present inventive concept is to provide a method of forming a
semiconductor device capable of improving a degree of integration.

25 [0006] According to an aspect of the present inventive concept, a semiconductor

device includes a lower structure; a stack structure on the lower structure and having an opening; a vertical structure in the opening; a contact structure on the vertical structure; and a conductive line on the contact structure, wherein the stack structure comprises a plurality of gate layers and a plurality of interlayer insulating layers, wherein the
5 vertical structure comprises an insulating core region, a channel semiconductor layer, a plurality of data storage patterns, a first dielectric layer, and a second dielectric layer, wherein the insulating core region extends in a vertical direction, the vertical direction being perpendicular to an upper surface of the lower structure, wherein the channel semiconductor layer covers a side surface and a lower surface of the insulating core
10 region, wherein the plurality of data storage patterns are disposed between the channel semiconductor layer and the plurality of gate layers, and are disposed to be spaced apart from each other in the vertical direction, wherein at least a portion of the first dielectric layer is disposed between the plurality of data storage patterns and the plurality of gate layers, wherein at least a portion of the second dielectric layer is disposed between the
15 plurality of data storage patterns and the channel semiconductor layer, and wherein the insulating core region comprises a plurality of first convex portions having increased widths in regions facing the plurality of gate layers.

[0007] According to an aspect of the present inventive concept, a semiconductor device includes a lower structure; a stack structure including an interlayer insulating
20 layer and a gate layer, sequentially stacked on the lower structure; and a vertical structure passing through the stack structure, wherein the vertical structure comprises an insulating core region passing through the interlayer insulating layer and the gate layer, a channel semiconductor layer covering at least a side surface of the insulating core region, a data storage pattern between the channel semiconductor layer and the gate
25 layer, a first dielectric layer at least interposed between the data storage pattern and the

gate layer, and a second dielectric layer at least interposed between the data storage pattern and the channel semiconductor layer, wherein the data storage pattern has a first side surface facing the gate layer, and a second side surface facing the channel semiconductor layer, and wherein the second side surface of the data storage pattern has
5 a concave portion.

[0008] According to an aspect of the present inventive concept, a semiconductor device includes a lower structure; a stack structure including an interlayer insulating layer and a gate layer, sequentially stacked on the lower structure; and a vertical structure passing through the stack structure, wherein the vertical structure comprises an
10 insulating core region passing through the interlayer insulating layer and the gate layer, a channel semiconductor layer covering at least a side surface of the insulating core region, a data storage pattern between the channel semiconductor layer and the gate layer, a first dielectric layer at least interposed between the data storage pattern and the gate layer, and a second dielectric layer at least interposed between the data storage
15 pattern and the channel semiconductor layer, and wherein the insulating core region has at least two inflection points in regions facing the gate layer.

BRIEF DESCRIPTION OF DRAWINGS

[0009] The above and other aspects, features, and advantages of the present inventive
20 concept will be more clearly understood from the following detailed description, taken in conjunction with the accompanying drawings, in which:

[0010] FIG. 1 is a plan view illustrating a portion of a semiconductor device, according to an example embodiment of the present inventive concept.

[0011] FIG. 2 is a cross-sectional view illustrating an example of a semiconductor
25 device, according to an example embodiment of the present inventive concept.

[0012] FIG. 3 is a partially enlarged view illustrating portion 'A' of FIG. 2.

[0013] FIG. 4 is a partially enlarged view illustrating portion 'B' of FIG. 2.

[0014] FIG. 5 is a partially enlarged view illustrating a modified example of a semiconductor device, according to an example embodiment of the present inventive
5 concept.

[0015] FIG. 6 is a partially enlarged view illustrating a modified example of a semiconductor device, according to an example embodiment of the present inventive concept.

[0016] FIG. 7 is a partially enlarged view illustrating a modified example of a
10 semiconductor device, according to an example embodiment of the present inventive concept.

[0017] FIG. 8A is a cross-sectional view illustrating a modified example of a semiconductor device, according to an example embodiment of the present inventive concept.

15 [0018] FIG. 8B is a partially enlarged view illustrating portion 'A1' of FIG. 8A.

[0019] FIG. 9 is a partially enlarged view illustrating a modified example of a semiconductor device, according to an example embodiment of the present inventive concept.

[0020] FIG. 10 is a cross-sectional view illustrating a modified example of a
20 semiconductor device, according to an example embodiment of the present inventive concept.

[0021] FIG. 11 is a cross-sectional view illustrating a modified example of a semiconductor device, according to an example embodiment of the present inventive concept.

25 [0022] FIG. 12 is a cross-sectional view illustrating a modified example of a

semiconductor device, according to an example embodiment of the present inventive concept.

[0023] FIGS. 13A to 13F are cross-sectional views illustrating an example of a method of forming a semiconductor device, according to an example embodiment of the present
5 inventive concept.

[0024] FIGS. 14A to 14C are cross-sectional views illustrating another example of a method of forming a semiconductor device, according to an example embodiment of the present inventive concept.

DETAILED DESCRIPTION

[0025] Hereinafter, example embodiments of the present inventive concept will be described with reference to the accompanying drawings. In the drawings, like numbers refer to like elements throughout.

[0026] FIG. 1 is a plan view illustrating a portion of a semiconductor device according
15 to an example embodiment of the present inventive concept, FIG. 2 is a cross-sectional view illustrating a region taken along cross-sectional line I-I' of FIG. 1 to illustrate an example of a semiconductor device according to an example embodiment of the present inventive concept, FIG. 3 is a partially enlarged view illustrating portion 'A' of FIG. 2, and FIG. 4 is a partially enlarged view illustrating portion 'B' of FIG. 2.

[0027] Referring to FIGS. 1 to 4, a stack structure 68 may be disposed on a lower
20 structure 3. In an example, the lower structure 3 may include a semiconductor substrate. The stack structure 68 may include a plurality of interlayer insulating layers 22 and a plurality of gate layers 65, alternately stacked.

[0028] A horizontal connection structure 62 may be disposed between the lower
25 structure 3 and the stack structure 68. The horizontal connection structure 62 may

include a lower horizontal connection pattern 59, and an upper horizontal connection pattern 17 on the lower horizontal connection pattern 59. The lower horizontal connection pattern 59 and the upper horizontal connection pattern 17 may be formed of polysilicon having N-type conductivity.

5 [0029] An opening 30 passing through the stack structure 68 may be disposed. A vertical structure 50 may be disposed in the opening 30. The vertical structure 50 may pass through the stack structure 68, may extend in a downward direction (e.g., toward the upper surface 3s of the lower structure 3), may pass through the horizontal connection structure 62, and may extend into the lower structure 3. When viewed in
10 plan view, the vertical structure 50 may have a circular shape, an elliptical shape, an oval shape, etc.

[0030] A first upper insulating layer 53 and a second upper insulating layer 75 sequentially stacked on the stack structure 68 and the vertical structure 50 may be arranged. For example, the first upper insulating layer 53 may be formed on an upper
15 surface of the uppermost interlayer insulating layers 22U of the interlayer insulating layers 22, and the second upper insulating layer 75 may be formed on an upper surface of the first upper insulating layer 53.

[0031] Separation structures 72 passing through the first upper insulating layer 53 and the stack structure 68 may be disposed. Each of the separation structures 72 may include
20 a separation spacer 72a and a separation pattern 72b. The separation spacer 72a may be disposed on a side surface of the separation pattern 72b, contacting the side surface of the separation pattern 72b. In an example, the separation spacer 72a may be formed of an insulating material, and the separation pattern 72b may be formed of a conductive material. In another example, the separation structures 72 may be formed of an
25 insulating material. For example, the separation structures 72 may be formed of a

silicon oxide.

[0032] The separation structures 72 may pass through the first upper insulating layer 53, may extend in the downward direction (e.g., toward the upper surface 3s of the lower structure 3), and may pass through the horizontal connection structure 62. The
5 separation structures 72 may separate the stack structure 68 in a first horizontal direction X. The separation structures 72 may have a linear shape extending lengthwise in a second horizontal direction Y, perpendicular to the first horizontal direction X. The first and second horizontal directions X and Y may be parallel to an upper surface 3s of the lower structure 3.

10 [0033] A conductive line 81 may be disposed on the second upper insulating layer 75. A contact plug 78 may be disposed between the conductive line 81 and the vertical structure 50.

[0034] The stack structure 68 may include the interlayer insulating layers 22 and the gate layers 65, alternately and repeatedly stacked.

15 [0035] In an example, each of the plurality of gate layers 65 may include a first layer 66a and a second layer 66b. The first layer 66a may extend between the first layer 66a and the vertical structure 50 while covering lower and upper surfaces of the second layer 66b.

[0036] In an example, the second layer 66b may include a conductive material (e.g.,
20 doped polysilicon, TiN, TaN, WN, TiSi, TaSi, CoSi, WSi, Ti, Ta, W, or the like), and the first layer 66a may comprise a dielectric material. The dielectric material of the first layer 66a may be a high-k dielectric such as AlO, or the like. In another example, the first layer 66a may be replaced with a conductive material, different from the conductive material of the second layer 66b (e.g. TiN, WN, or the like).

25 [0037] The plurality of gate layers 65 may include one or a plurality of lower gate

layers 65L, a plurality of intermediate gate layers 65M on the one or plurality of lower gate layers 65L, and one or a plurality of upper gate layers 65U on the plurality of intermediate gate layers 65M.

[0038] At least one lower gate layer 65L, among the one or the plurality of lower gate layers 65L, may include a ground select gate electrode, and at least one upper gate layer 65U, among the one or the plurality of upper gate layers 65U, may include a string select gate electrode. The plurality of intermediate gate layers 65M may include word lines. For example, second layers 66b of the plurality of intermediate gate layers 65M may be the word lines.

[0039] The interlayer insulating layers 22 may include a lowermost interlayer insulating layer 22L, an uppermost interlayer insulating layer 22U, and intermediate interlayer insulating layers 22M between the lowermost interlayer insulating layer 22L and the uppermost interlayer insulating layer 22U. Among the interlayer insulating layers 22, the uppermost interlayer insulating layer 22U may have a thickness greater than that of each of the remaining interlayer insulating layers 22. The interlayer insulating layers 22 may be formed of silicon oxide.

[0040] An insulating pattern 27 extending from an upper surface of the stack structure 68 in the downward direction (e.g., toward an upper surface 3s of the lower structure 3) and passing through the one or more upper gate layers 65U may be disposed. The insulating pattern 27 may be formed of silicon oxide. The vertical structure 50 may be spaced apart from the insulating pattern 27. For example, the insulating pattern 27 may be disposed between and spaced apart from adjacent ones of the vertical structures 50. A dummy structure 50d contacting the insulating pattern 27 and passing through the stack structure 68 may be disposed (FIG. 1). A cross-sectional structure of the dummy structure 50d of FIG. 1 may be the same as a cross-sectional structure of the vertical

structure 50. In some embodiments, the dummy structures 50d may be formed in the same processes and may include the same materials as the vertical structures 50; however, the dummy structures 50d may not be effective to function for operations.

[0041] Reinforcing patterns 36 may be arranged adjacent to the vertical structure 50.

5 The reinforcing patterns 36 may be formed of an insulating material such as silicon oxide, or the like.

[0042] In an example, the reinforcing patterns 36 may be adjacent to a side surface of the vertical structure 50, and may be spaced apart from each other in a vertical direction Z. The vertical direction Z may be a direction perpendicular to the upper surface 3s of the lower structure 3. The reinforcing patterns 36 may be disposed between the interlayer insulating layers 22 and the vertical structure 50. The reinforcing patterns 36 may include a lower reinforcing pattern 36L interposed between the lowermost interlayer insulating layer 22L and the vertical structure 50 and extending between a portion of the horizontal connection structure 62 and the vertical structure 50. For example, the lower reinforcing pattern 36L may be disposed between the upper horizontal connection pattern 17 and the vertical structure 50. In addition, the reinforcing patterns 36 may include an upper reinforcing pattern 36U interposed between the uppermost interlayer insulating layer 22U and the vertical structure 50, and an intermediate reinforcing patterns 36M interposed between the intermediate interlayer insulating layers 22M and the vertical structure 50.

[0043] Each of the intermediate reinforcing patterns 36M may be in contact with a corresponding one of the intermediate interlayer insulating layers 22M. Each of the intermediate reinforcing patterns 36M may have a vertical thickness greater than that of each of the intermediate interlayer insulating layers 22M. In this case, the vertical thickness refers to a thickness in the vertical direction (Z direction). Each of the

intermediate reinforcing patterns 36M may be concave in a central portion of the intermediate reinforcing patterns 36M, facing the vertical structure 50.

[0044] A substrate insulating layer 37 interposed between the vertical structure 50 and the lower structure 3 may be disposed. The substrate insulating layer 37 may be at a lower vertical level than that of the upper surface 3s of the lower structure 3. The substrate insulating layer 37 may be formed of silicon oxide.

[0045] In an example, the vertical structure 50 may include an insulating core region 46, a channel semiconductor layer 44, a plurality of data storage patterns 40, a first dielectric layer 38, a second dielectric layer 42, and a pad pattern 48.

[0046] The insulating core region 46 may extend in the vertical direction Z. The insulating core region 46 may include an insulating material. For example, the insulating core region 46 may be filled with an insulating material such as silicon oxide, or the like, or may be formed of an insulating material having a void therein.

[0047] The pad pattern 48 may be disposed on the insulating core region 46, and may contact a top surface of the insulating core region 46. The pad pattern 48 may be formed of polysilicon having N-type conductivity.

[0048] At least a portion of the channel semiconductor layer 44 may cover a side surface and a lower surface of the insulating core region 46, contacting the side surface and the lower surface of the insulating core region 46. The channel semiconductor layer 44 may be in contact with the pad pattern 48. For example, the channel semiconductor layer 44 may contact a side surface of the pad pattern 48. Therefore, the channel semiconductor layer 44 may be electrically connected to the pad pattern 48. The channel semiconductor layer 44 may be formed of polysilicon.

[0049] The plurality of data storage patterns 40 may be spaced apart from each other in the vertical direction Z while being disposed between the plurality of gate layers 65 and

the channel semiconductor layer 44. The plurality of data storage patterns 40 may face the plurality of gate layers 65 in a one-to-one manner.

[0050] The plurality of data storage patterns 40 may be formed of a material capable of storing data. For example, when a semiconductor device according to an example
5 embodiment of the present inventive concept is a memory device such as a NAND flash, the plurality of data storage patterns 40 may be formed of a material capable of charge trapping, for example, silicon nitride.

[0051] In example embodiments of the present inventive concept, the material of the plurality of data storage patterns 40 is not limited to silicon nitride, and may be replaced
10 with another material capable of storing data.

[0052] At least a portion of the first dielectric layer 38 may be disposed between the plurality of data storage patterns 40 and the plurality of gate layers 65. The first dielectric layer 38 may extend from a portion interposed between the plurality of data storage patterns 40 and the plurality of gate layers 65, to cover the reinforcing patterns
15 36. For example, a portion of the first dielectric layer 38 may be disposed between the reinforcing patterns 36 and the second dielectric layer 42, contacting both the reinforcing patterns 36 and the second dielectric layer 42.

[0053] At least a portion of the second dielectric layer 42 may be disposed between the plurality of data storage patterns 40 and the channel semiconductor layer 44, contacting
20 both the plurality of data storage patterns 40 and the channel semiconductor layer 44. The second dielectric layer 42 may extend from a portion interposed between the plurality of data storage patterns 40 and the channel semiconductor layer 44, to cover the first dielectric layer 38.

[0054] Between the channel semiconductor layer 44 and the plurality of gate layers 65,
25 the plurality of data storage patterns 40 may be disposed between the first dielectric

layer 38 and the second dielectric layer 42. The first dielectric layer 38 may cover a lower surface of the channel semiconductor layer 44, and may cover an external side surface of the channel semiconductor layer 44. The second dielectric layer 42 may be disposed between the channel semiconductor layer 44 and the first dielectric layer 38.

5 [0055] The horizontal connection structure 62 may include one or a plurality of horizontal connection patterns. For example, the horizontal connection structure 62 may include the lower horizontal connection pattern 59, and the upper horizontal connection pattern 17 on the lower horizontal connection pattern 59. The lower horizontal connection pattern 59 and the upper horizontal connection pattern 17 may be formed of
10 polysilicon. For example, the lower horizontal connection pattern 59 and the upper horizontal connection pattern 17 may be formed of polysilicon having N-type conductivity. The upper horizontal connection pattern 17 may be spaced apart from the channel semiconductor layer 44. The lower horizontal connection pattern 59 may pass through the first dielectric layer 38 and the second dielectric layer 42, and may contact
15 the channel semiconductor layer 44. The lower horizontal connection pattern 59 may further include a first extension portion 59E1 extending between the lower structure 3 and the channel semiconductor layer 44, and a second extension portion 59E2 extending between the upper horizontal connection pattern 17 and the channel semiconductor layer 44. In some embodiments, the first extension portion 59E1 may contact upper
20 surfaces of the substrate insulating layer 37, the first dielectric layer 38, and the second dielectric layer 42, and the second extension portion 59E2 may contact lower surfaces of the lower reinforcing pattern 36L, the first dielectric layer 38, and the second dielectric layer 42.

[0056] A vertical thickness of each of the plurality of data storage patterns 40 may be
25 smaller than a vertical thickness of each of the plurality of gate layers 65.

[0057] Each of the plurality of data storage patterns 40 may have a lower surface 40L and an upper surface 40U. In each of the plurality of data storage patterns 40, at least one of the lower surface 40L and the upper surface 40U may have a concave shape. For example, in some embodiments, the lower surface 40L and the upper surface 40U each
5 may have a concave shape.

[0058] Each of the plurality of data storage patterns 40 may include a first side surface 40S1 facing the plurality of gate layers 65, and a second side surface 40S2 facing the channel semiconductor layer 44. Each of the plurality of data storage patterns 40 may include a first portion 40p1 adjacent to the first side surface 40S1, a second portion
10 40p2 adjacent to the second side surface 40S2, and a minimum vertical thickness portion 40p3 between the first portion 40p1 and the second portion 40p2. A thickness of the minimum vertical thickness portion 40p3 may be less than a maximum vertical thickness of the first portion 40p1 and a maximum vertical thickness of the second portion 40p2.

[0059] In each of the plurality of data storage patterns 40, a distance between the minimum vertical thickness portion 40p3 and the first side surface 40S1 may be less than a distance between the minimum vertical thickness portion 40p3 and the second side surface 40S2. For example, the minimum vertical thickness portion 40p3 may be nearer to the first side surface 40S1 than to the second side surface 40S2.

[0060] In each of the plurality of data storage patterns 40, the second side surface 40S2 may have a concave portion 40R. The second side surface 40S2 may have curved shapes above and below the concave portion 40R.

[0061] In an example, a distance between an upper end and a lower end of the first side surface 40S1 may be less than a distance between an upper end and a lower end of the
25 second side surface 40S2.

[0062] The insulating core region 46 may include a plurality of first convex portions 46a1 having increased widths in regions facing the plurality of gate layers 65. The insulating core region 46 may include a plurality of second convex portions 46a2 having increased widths in regions facing the plurality of interlayer insulating layers 22, and
5 concave portions 46b1 and 46b2 having decreased widths between the first convex portions 46a1 and the second convex portions 46a2. Each of the concave portions 46b1 and 46b2 may have a width less than that of each of the first and second convex portions 46a1 and 46a2.

[0063] Hereinafter, for convenience of description, the description will be made based
10 on any one of the first convex portions 46a1 facing any one of the gate layers 65.

[0064] A portion of the insulating core region 46 may include any one of the first convex portions 46a1, a first concave portion 46b1 disposed below the first convex portion 46a1 and having a width less than that of the first convex portion 46a1, and a second concave portion 46b2 disposed on the first convex portion 46a1 and having a
15 width less than that of the first convex portion 46a1. A portion of the insulating core region 46 may further include the second convex portion 46a2 disposed below the first concave portion 46b1 and having a width greater than that of the first concave portion 46b1. A portion having a minimum horizontal width in the first concave portion 46b1, and a portion having a minimum horizontal width in the second concave portion 46b2
20 may face any one of the gate layers 65.

[0065] A distance between the portion having the minimum horizontal width in the first concave portion 46b1 and the portion having the minimum horizontal width in the second concave portion 46b2 may be greater than the maximum vertical width of any one of the data storage patterns 40.

25 [0066] The distance between the portion having the minimum horizontal width in the

first concave portion 46b1 and the portion having the minimum horizontal width in the second concave portion 46b2 may be less than a vertical thickness of any one of the gate layers 65. For example, both of the first concave portion 46b1 and the second concave portion 46b2 may be at a higher vertical level than a lower surface of an adjacent gate layer 65 and at a lower vertical level than an upper surface of the adjacent gate layer 65.

[0067] A distance between a portion having a maximum horizontal width in the second convex portion 46a2 and the portion having the minimum horizontal width in the first concave portion 46b1 may be greater than a distance between the portion having the minimum horizontal width in the first concave portion 46b1 and a portion having a maximum horizontal width in the first convex portion 46a1.

[0068] A distance between a first inflection point 46i1 between a side surface of the first concave portion 46b1 and a side surface of the first convex portion 46a1 and a second inflection points 46i2 between a side surface of the first convex portion 46a1 and a side surface of the second concave portion 46b2 may be less than the vertical thickness of any one of the gate layers 65. The first inflection point 46i1 may be the point at which the concavity (or convexity) changes between the first convex portion 46a1 and the first concave portion 46b1, and the second inflection point 46i2 may be the point at which the concavity (or convexity) changes between the first convex portion 46a1 and the second concave portion 46b2.

[0069] The distance between the first inflection point 46i1 between the side surface of the first concave portion 46b1 and the side surface of the first convex portion 46a1 and the second inflection points 46i2 between the side surface of the first convex portion 46a1 and the side surface of the second concave portion 46b2 may be less than the maximum vertical width of any one of the data storage patterns 40.

[0070] The insulating core region 46 may further include a lower convex portion 46c

(of FIG. 4) facing the lower horizontal connection pattern 59, a first lower concave portion 46d1 (of FIG. 4) disposed below the lower convex portion 46c and having a smaller width than that of the lower convex portion 46c, and a second lower concave portion 46d2 (of FIG. 4) disposed on the lower convex portion 46c and having a smaller width than that of the lower convex portion 46c.

[0071] In an example, the data storage patterns 40 may be spaced apart from each other in the vertical direction Z. Therefore, interference between the data storage patterns 40 adjacent to each other in the vertical direction Z may be prevented, and a phenomenon in which a charge trapped in the data storage patterns 40 by the operation of a NAND flash memory device moves to a region other than the data storage patterns 40 may be prevented. Therefore, in a semiconductor device such as a NAND flash memory device, data retention characteristics may be improved.

[0072] Next, modified examples of the plurality of data storage patterns 40 described above will be described with reference to FIGS. 5 and 6, respectively. FIGS. 5 and 6 are partially enlarged cross-sectional views, corresponding to the partially enlarged cross-sectional view of FIG. 3, to describe modified examples of the plurality of data storage patterns 40. In this case, a data storage pattern of any one of the plurality of data storage patterns 40 will be mainly described.

[0073] In a modified example, referring to FIG. 5, at least a portion of a plurality of data storage patterns 40 may further include a void 40v between a first side surface 40S1 and a second side surface 40S2. A distance between the void 40v and the first side surface 40S1 may be greater than a distance between the void 40v and the second side surface 40S2. For example, the void 40v may be closer to the second side surface 40S2 than to the first side surface 40S1. In some embodiments, the void 40v may include air. The term “air” as discussed herein, may refer to atmospheric air, or other gases that may

be present during the manufacturing process.

[0074] In a modified example, referring to FIG. 6, any one of data storage patterns 40' may have a concave upper surface 40U' and a concave lower surface 40L', in a similar manner to those described above. The data storage pattern 40' may have a first side surface 40S1' facing any one of gate layers 65, and a second side surface 40S2' facing a channel semiconductor layer 44.

[0075] In an example, a distance between an upper end and a lower end of the first side surface 40S1' may be greater than a distance between an upper end and a lower end of the second side surface 40S2'.

[0076] The data storage pattern 40' may include a first portion 40p1' adjacent to the first side surface 40S1', a second portion 40p2' adjacent to the second side surface 40S2', and a minimum vertical thickness portion 40p3' between the first portion 40p1' and the second portion 40p2'. The minimum vertical thickness portion 40p3' may have a thickness less than a maximum vertical thickness of the first portion 40p1' and a maximum vertical thickness of the second portion 40p2'.

[0077] A distance between the minimum vertical thickness portion 40p3' and the first side surface 40S1' may be greater than a distance between the minimum vertical thickness portion 40p3' and the second side surface 40S2'. For example, the minimum vertical thickness portion 40p3' may be nearer to the second side surface 40S2' than to the first side surface 40S1'.

[0078] The data storage pattern 40' may further include a void 40v' between the first side surface 40S1' and the second side surface 40S2'. A distance between the void 40v' and the first side surface 40S1' may be less than a distance between the void 40v' and the second side surface 40S2'. For example, the void 40v' may be closer to the first side surface 40S1' than to the second side surface 40S2'.

[0079] Next, a modified example of the insulating core region 46 described above will be described with reference to FIG. 7. FIG. 7 is a partially enlarged cross-sectional view, corresponding to the partially enlarged cross-sectional view of FIG. 4, to illustrate a modified example of the insulating core region 46 described above.

5 [0080] In a modified example, referring to FIG. 7, a portion of an insulating core region 46' facing a horizontal connection structure 62 may have a substantially constant width. Therefore, a channel semiconductor layer 44' between the horizontal connection structure 62 and a side surface of the insulating core region 46' may have a straight linear shape. In such embodiments, the side surface of the lower horizontal connection
10 pattern 59 adjacent to and contacting the channel semiconductor layer 44' may be linear and substantially perpendicular to the upper surface 3s of the lower structure 3.

[0081] Next, a modified example of a semiconductor device according to an example embodiment of the present inventive concept will be described with reference to FIGS. 8A and 8B. FIG. 8A is a cross-sectional view illustrating a modified example of a
15 semiconductor device according to an example embodiment of the present inventive concept, and FIG. 8B is a partially enlarged view illustrating portion 'A1' of FIG. 8A. In describing a modified example of a semiconductor device according to an example embodiment of the present inventive concept with reference to FIGS. 8A and 8B, the modified components of the components described with reference to FIGS. 1 to 4 will
20 be mainly described, and non-modified components may be omitted or cited directly.

[0082] In a modified example, referring to FIGS. 8A and 8B, a vertical structure 50a may sequentially pass through the stack structure 68 and the horizontal connection structure 62, described above, and may extend into the lower structure 3. The vertical structure 50a may include the first dielectric layer 38, the data storage patterns 40, the
25 second dielectric layer 42, and the channel semiconductor layer 44, and the pad pattern

48, in a substantially same manner to those described with reference to FIGS. 2 to 4. The vertical structure 50a may include an insulating core region 146 having a shape different from that of the insulating core region 46 of FIGS. 2 to 4. For example, the insulating core region 146 of the vertical structure 50a may have convex portions 146a
5 in regions facing the data storage patterns 40, and may not have convex portions in regions facing the interlayer insulating layers 22. The insulating core region 146 may have a substantially constant width in regions facing the interlayer insulating layers 22. For example, a side surface of the insulating core region 146 adjacent to the interlayer insulating layers 22 may be linear and substantially perpendicular to the upper surface
10 3s of the lower structure 3.

[0083] One of the convex portions 146a of the insulating core region 146 may be formed between a first portion 146b1 and a second portion 146b2. A vertical thickness of the convex portion 146a, that is, a distance between the first portion 146b1 and the second portion 146b2 may be less than a thickness of any one of the gate layers 65. For
15 example, the first portion 146b1 may be at a higher vertical level than a lower surface of an adjacent gate layer 65 and the second portion 146b2 may be at a lower vertical level than an upper surface of the adjacent gate layer 65.

[0084] The data storage patterns 40 may overlap the interlayer insulating layers 22 in the vertical direction. The reinforcing patterns described with reference to FIGS. 2 to 4
20 (e.g., the reinforcing patterns 36 of FIGS. 2 to 4) may be modified to be formed on surfaces of the interlayer insulating layers 22 facing the data storage patterns 40. Reinforcing patterns 136, thus modified, may be formed on an upper surface and a lower surface of the interlayer insulating layers 22 facing the data storage patterns 40.

[0085] Next, a modified example of the insulating core region 146 and the reinforcing
25 patterns 136 described above with reference to FIGS. 8A and 8B will be described with

reference to FIG. 9. FIG. 9 is a partially enlarged cross-sectional view, corresponding to the partially enlarged cross-sectional view of FIG. 8B, to describe modified examples of the insulating core region 146 and the reinforcing patterns 136 described above with reference to FIGS. 8A and 8B.

5 [0086] In a modified example, referring to FIG. 9, a reinforcing pattern 236, having a round shape, may cover a side surface of any one of the interlayer insulating layer 22, and may extend to an upper surface and a lower surface of the interlayer insulating layer 22. An insulating core region 246 may include a convex portion 246a facing the gate layer 65 and a concave portion 246b facing the interlayer insulating layer 22.

10 [0087] Next, a modified example of a semiconductor device according to an example embodiment of the present inventive concept will be described with reference to FIG. 10. FIG. 10 is a cross-sectional view illustrating a modified example of a semiconductor device according to an example embodiment of the present inventive concept. In this case, modified portions in the semiconductor device according to the example
15 embodiment, described above with reference to FIGS. 2 to 4, will be mainly described.

[0088] Referring to FIG. 10, the lower structure 3 and the horizontal connection structure 62 may be provided in a substantially same manner to those described with reference to FIGS. 2 to 4. The stack structure of FIG. 2 (e.g., the stack structure 68 of FIG. 2) may be modified into a stack structure 68' including a lower stack group 68a,
20 and an upper stack group 68b on the lower stack group 68a. The lower stack group 68a may include lower interlayer insulating layers 22a and lower gate layers 65a, alternately and repeatedly stacked. The upper stack group 68b may include upper interlayer insulating layers 22b and upper gate layers 65b, alternately and repeatedly stacked. The lower and upper interlayer insulating layers 22a and 22b may be formed of the same
25 material, for example, silicon oxide. The lower and upper gate layers 65a and 65b may

be formed of the same material and structure. For example, each of the lower and upper gate layers 65a and 65b may include a first layer 66a and a second layer 66b. The first and second layers 66a and 66b may be substantially the same as those described with reference to FIGS. 2 to 4.

5 [0089] A vertical structure 50c may be disposed to sequentially pass through the stack structure 68 and the horizontal connection structure 62, and may extend into the lower structure 3.

[0090] The vertical structure 50c may include a lower portion 50c_L, and an upper portion 50c_U on the lower portion 50c_L.

10 [0091] In the vertical structure 50c, a width of a lower region of the upper portion 50c_U, adjacent to the lower portion 50c_L, may be less than a width of an upper region of the lower portion 50c_L, adjacent to the upper portion 50c_U.

[0092] The vertical structure 50c may include substantially the same components as those described above with reference to FIGS. 2 to 4 (e.g., the components described
15 above in connection with the vertical structure 50 of FIGS. 2 to 4). For example, the vertical structure 50c may include the first dielectric layer 38, the data storage patterns 40, the second dielectric layer 42, the channel semiconductor layer 44, the insulating core region 46, and the pad pattern 48, described above with reference to FIGS. 2 to 4.

[0093] A first upper insulating layer 53 and a second upper insulating layer 75,
20 sequentially stacked on the stack structure 68', may be arranged. A separation structure 172 passing through the first upper insulating layer 53, the stack structure 68', and the horizontal connection structure 62 may be disposed. The separation structure 172 may be comprised of upper and lower portions, and side surfaces of the upper and lower portions of the separation structure 172 may have an angle with respect to the upper
25 surface 3s of the lower structure 3. The separation structure 172 may be formed of an

insulating material such as silicon oxide, or the like.

[0094] Next, referring to FIG. 11, a modified example of the semiconductor device according to an example embodiment will be described. FIG. 11 is a cross-sectional view illustrating a modified example of a semiconductor device according to an example embodiment of the present inventive concept.

[0095] Referring to FIG. 11, a stack structure 568 may be disposed on a lower structure 503. The lower structure 503 may include a semiconductor substrate. The stack structure 568 may include interlayer insulating layers 522 and gate layers 565, alternately and repeatedly stacked.

[0096] The interlayer insulating layers 522 may include a first lower interlayer insulating layer 522L1, a second lower interlayer insulating layer 522L2 on the first lower interlayer insulating layer 522L1, intermediate interlayer insulating layers 522M on the second lower interlayer insulating layer 522L2, and an upper interlayer insulating layer 522U on the intermediate interlayer insulating layers 522M.

[0097] Each of the gate layers 565 may include a first layer 566a and a second layer 566b. The first layer 566a and the second layer 566b may correspond to the first layer 66a and the second layer 66b, respectively, as described with reference to FIGS. 2 to 4. Therefore, the gate layers 565 may be formed of substantially the same material and have the same structure as the gate layers described with reference to FIGS. 2 to 4 (e.g., the gate layers 65 of FIGS. 2 to 4).

[0098] The gate layers 565 may include a lower gate layer 565L between the first lower interlayer insulating layer 522L1 and the second lower interlayer insulating layer 522L2, intermediate gate layers 565M on the lower gate layer 565L, and one or a plurality of upper gate layers 565U on the intermediate gate layers 565M.

[0099] An insulating pattern 527 passing through the upper interlayer insulating layer

522U, extending in the downward direction (e.g., toward an upper surface of the lower structure 503), and passing through the one or the plurality of upper gate layers 565U may be disposed.

5 [00100] An opening 530 passing through the stack structure 568 and exposing the lower structure 503 may be disposed. A vertical structure 550 may be disposed in the opening 530. The vertical structure 550 may pass through the stack structure 568, and may extend into the lower structure 503.

[00101] The vertical structure 550 may include a lower semiconductor pattern 531, an insulating core region 546, a pad pattern 548, a channel semiconductor layer 544, a first dielectric layer 538, a second dielectric layer 542, and data storage patterns 540.

[00102] The lower semiconductor pattern 531 may be in contact with the lower structure 503. The lower semiconductor pattern 531 may face the lower gate layer 565L, and may be disposed on a lower level than the intermediate gate layers 565M. The insulating core region 546 may partially fill the opening 530 on the lower semiconductor pattern 531. The pad pattern 548 may be disposed on the insulating core region 546. The channel semiconductor layer 544 may cover a lower surface and a side surface of the insulating core region 546, and may be connected to the pad pattern 548. The channel semiconductor layer 544 may be connected to the lower semiconductor pattern 531.

20 [00103] The first dielectric layer 538 may be disposed between the channel semiconductor layer 544 and the stack structure 568 on the lower semiconductor pattern 531. The second dielectric layer 542 may be disposed between the channel semiconductor layer 544 and the first dielectric layer 538 on the lower semiconductor pattern 531. The data storage patterns 540 may face the intermediate and upper gate layers 565M and 565U on the lower semiconductor pattern 531, and may be disposed

between the first dielectric layer 538 and the second dielectric layer 542.

[00104] A cross-sectional structure of the vertical structure 550, adjacent to the intermediate and upper gate layers 565M and 565U and the intermediate and upper interlayer insulating layers 522M and 522U, may be substantially the same as the cross-sectional structure of the vertical structure 50 of, for example, FIG. 2, adjacent to the gate layers 65 of, for example, FIG. 2 and the intermediate and upper interlayer insulating layers 22M and 22U of, for example, FIG. 2. Therefore, the cross-sectional structure of the vertical structure 550 may be substantially the same as the cross-sectional structure of the vertical structure 50, described with reference to FIG. 2 and FIG. 3, in which portion 'A' of FIG. 2 is enlarged.

[00105] Reinforcing patterns 536 adjacent to the vertical structure 550 may be disposed. The reinforcing patterns 536 may be formed of an insulating material such as silicon oxide, or the like. In an example, the reinforcing patterns 536 may include a lower reinforcing pattern 536L interposed between the second lower interlayer insulating layer 522L2 and the vertical structure 550 and contacting a portion of an upper surface of the lower semiconductor pattern 531, an upper reinforcing pattern 536U interposed between the upper interlayer insulating layer 522U and the vertical structure 550, and intermediate reinforcing patterns 536M interposed between the intermediate interlayer insulating layers 522M and the vertical structure 550.

[00106] A first upper insulating layer 553 and a second upper insulating layer 575 may be sequentially arranged on the stack structure 568. Separation structures 572 passing through the first upper insulating layer 553 and the stack structure 568 may be disposed. Each of the separation structures 572 may include a separation spacer 572a and a separation pattern 572b. The separation spacer 572a may be disposed on a side surface of the separation pattern 572b. In an example, the separation spacer 572a may

be formed of an insulating material, and the separation pattern 572b may be formed of a conductive material. In another example, the separation structures 572 may be formed of an insulating material.

[00107] Conductive lines 581 may be disposed on the second upper insulating layer 575. A contact plug 578 may be disposed between the conductive line 581 and the vertical structure 550.

[00108] Next, a modified example of the lower structure 3 described above will be described with reference to FIG. 12. FIG. 12 is a cross-sectional view illustrating a modified example of a semiconductor device according to an example embodiment of the present inventive concept.

[00109] In a modified example, referring to FIG. 12, the lower structure (e.g., the lower structure 3 of FIG. 2) described above in FIG. 2 may be replaced by a lower structure 3' including a lower substrate 5, a peripheral circuit region 7 on the lower substrate 5, and an upper substrate 9 on the peripheral circuit region 7. The lower substrate 5 may be a semiconductor substrate. The peripheral circuit region 7 may include a peripheral circuit wiring 7a, and a peripheral insulating layer 7b covering the peripheral circuit wiring 7a. The upper substrate 9 may be a conductive substrate. For example, the upper substrate 9 may include polysilicon and / or a metal material, having N-type conductivity.

[00110] Next, an example of a method of forming a semiconductor device according to an example embodiment of the present inventive concept will be described with reference to FIGS. 13A to 13F. FIGS. 13A to 13F are cross-sectional views illustrating regions taken along cross-sectional line I-I' of FIG. 1 to illustrate an example of a method of forming a semiconductor device according to an example embodiment of the present inventive concept.

[00111] Referring to FIGS. 1 and 13A, a lower horizontal mold layer 15 and an upper horizontal connection pattern 17 may be sequentially formed on a lower structure 3. The lower horizontal mold layer 15 may include a first lower horizontal mold layer 15a, a second lower horizontal mold layer 15b, and a third lower horizontal mold layer 15c, sequentially stacked.

[00112] In an example, the first and third lower horizontal mold layers 15a and 15c may be formed of a first material (e.g., silicon oxide), and the second lower horizontal mold layer 15b may be formed of a second material (e.g., silicon nitride or polysilicon) different than those of the first and third lower horizontal mold layers 15a and 15c.

[00113] The upper horizontal connection pattern 17 may be formed of polysilicon. For example, the upper horizontal connection pattern 17 may be formed of polysilicon having N-type conductivity.

[00114] A mold structure 20 may be formed on the upper horizontal connection pattern 17.

[00115] The mold structure 20 may include a plurality of interlayer insulating layers 22 and a plurality of sacrificial gate layers 24, alternately and repeatedly stacked. The plurality of interlayer insulating layers 22 may include a lowermost interlayer insulating layer 22L, a plurality of intermediate interlayer insulating layers 22M on the lowermost interlayer insulating layer 22L, and an uppermost interlayer insulating layer 22U on the plurality of intermediate interlayer insulating layers 22M. The plurality of sacrificial gate layers 24 may be formed between the lowermost interlayer insulating layer 22L and the uppermost interlayer insulating layer 22U.

[00116] The plurality of interlayer insulating layers 22 may be formed of silicon oxide, and the plurality of sacrificial gate layers 24 may be formed of a material having etch selectivity with the plurality of interlayer insulating layers 22, for example, silicon

nitride.

[00117] An insulating pattern 27 passing through the uppermost interlayer insulating layer 22U, extending in a downward direction (e.g., toward the upper surface 3s of the lower structure 3), and passing through one or a plurality of upper sacrificial gate layers of the sacrificial gate layers 24 may be formed. The insulating pattern 27 may be formed of silicon oxide.

[00118] An opening 30 passing through the mold structure 20, extending in a downward direction (e.g., toward the upper surface 3s of the lower structure 3), sequentially passing through the upper horizontal connection pattern 17 and the lower horizontal mold layer 15, and extending into the lower structure 3 may be formed. The opening 30 may be formed in plural (e.g., a plurality of openings 30). In some embodiments, when viewed in plan view, each of the openings 30 may have a circular shape, an elliptical shape, an oval shape, etc.

[00119] Referring to FIGS. 1 and 13B, the interlayer insulating layers 22 may be etched, and preliminary reinforcing layers 33 may be formed on side surfaces of the interlayer insulating layers 22. The preliminary reinforcing layers 33 may be formed of polysilicon.

[00120] When the first and third lower horizontal mold layers 15a and 15c and the interlayer insulating layers 22 are formed of the same material, the first and third lower horizontal mold layers 15a and 15c may be etched along with etching of the interlayer insulating layers 22, a first lower preliminary reinforcing layer 33L1 may be formed on a side surface of the first lower horizontal mold layer 15a, and a second lower preliminary reinforcing layer 33L2 may be formed on a side surface of the third lower horizontal mold layer 15c.

[00121] Referring to FIGS. 1 and 13C, the sacrificial gate layers 24 may be

selectively etched to form recess regions 34.

[00122] In an example, when the second lower horizontal mold layer 15b and the sacrificial gate layers 24 are formed of the same material, for example silicon nitride, the second lower horizontal mold layer 15b may be etched, together with the sacrificial gate layers 24, to form a lowermost recess region 34L.

[00123] In another example, when the second lower horizontal mold layer 15b is formed of a material different from the sacrificial gate layers 24, for example polysilicon, the second lower horizontal mold layer 15b may not be substantially etched during the selective etching of the sacrificial gate layers 24.

[00124] Hereinafter, for convenience of description, an example in which the second lower horizontal mold layer 15b is formed of the same material as the sacrificial gate layers 24 will be mainly described.

[00125] Referring to FIGS. 1 and 13D, an oxidation process may be performed to form reinforcing patterns 36 and a substrate insulating layer 37. The oxidation process may be a process of oxidizing silicon to form silicon oxide.

[00126] The oxidation process may be a process of oxidizing the preliminary reinforcing layers (e.g., the preliminary reinforcing layers 33 of FIG. 13C), the first and second lower preliminary reinforcing layers (e.g., the first and second lower preliminary reinforcing layers 33L1 and 33L2 of FIG. 13C), the upper horizontal connection pattern 17, and the lower structure 3, to form silicon oxide.

[00127] The reinforcing patterns 36 may include an upper reinforcing pattern 36U, intermediate reinforcing patterns 36M, and a lower reinforcing pattern 36L. The upper reinforcing pattern 36U may be formed by oxidizing the preliminary reinforcing layer (e.g., the preliminary reinforcing layer 33 of FIG. 13C) on side surfaces of the uppermost interlayer insulating layer 22U. The intermediate reinforcing patterns 36M

may be formed by oxidizing the preliminary reinforcing layers (e.g., the preliminary reinforcing layers 33 of FIG. 13C) on side surfaces of the intermediate interlayer insulating layers 22M. The lower reinforcing pattern 36L may be formed by oxidizing the preliminary reinforcing layer (e.g., the preliminary reinforcing layer 33 of FIG. 13C),
5 the upper horizontal connection pattern 17, and the second lower preliminary reinforcing layer (e.g., the second lower preliminary reinforcing layer 33L2 of FIG. 13C) on side surfaces of the lowermost interlayer insulating layer 22L. The substrate insulating layer 37 may be formed by oxidizing a surface of the lower structure 3 exposed by the opening 30 and the first lower preliminary reinforcing layer (e.g., the
10 first lower preliminary reinforcing layer 33L1 of FIG. 13C).

[00128] Therefore, the reinforcing patterns 36 and the substrate insulating layer 37, as described with reference to FIGS. 2 to 4, may be formed.

[00129] In another example, the reinforcing patterns 36 may be formed by replacing the reinforcing patterns (e.g., the reinforcing patterns 136 of FIGS. 8A and 8B) of FIGS.
15 8A and 8B. For example, after forming the openings (e.g., the openings 30 of FIG. 13A) as in FIG. 13A, the sacrificial gate layers (e.g., the sacrificial gate layers 24 of FIG. 13C) may be etched and recessed, and the reinforcing patterns (e.g., the reinforcing patterns 136 of FIGS. 8A and 8B) as in FIGS. 8A and 8B may be formed on surfaces of the interlayer insulating layers 22 exposed during etching the sacrificial gate layers (e.g.,
20 the sacrificial gate layers 24 of FIG. 13C). The reinforcing patterns 136 of FIGS. 8A and 8B may be formed by an insulating by-product generated by etching the sacrificial gate layers (e.g., the sacrificial gate layers 24 of FIG. 13C).

[00130] In another example, the reinforcing patterns 36 may be formed by being replaced with the reinforcing patterns (e.g., the reinforcing patterns 236 of FIG. 9). For
25 example, after forming the openings (e.g., the openings 30 of FIG. 13A) as in FIG. 13A,

the sacrificial gate layers (e.g., the sacrificial gate layers 24 of FIG. 13C) may be etched and recessed, and an oxide layer having a low step coverage covering the side surfaces of the interlayer insulating layers 22 exposed during etching the sacrificial gate layers (e.g., the sacrificial gate layers 24 of FIG. 13C) may be deposited to form reinforcing patterns (e.g., the reinforcing patterns 236 of FIG. 9) as described in FIG. 9.

[00131] Referring to FIGS. 1 and 13E, a vertical structure 50 may be formed in the opening 30 in which the reinforcing patterns 36 and the substrate insulating layer 37 are formed. The formation of the vertical structure 50 may include forming a first dielectric layer 38 conformally covering an internal wall of the opening 30, forming a plurality of data storage patterns 40 defined in the recess regions 34 on the first dielectric layer 38, conformally forming a second dielectric layer 42, conformally forming a channel semiconductor layer 44, forming an insulating core region 46 on the channel semiconductor layer 44 that partially fills the opening 30, and forming a pad pattern 48 on the insulating core region 46.

[00132] The formation of the plurality of data storage patterns 40 may include forming a data storage layer on the first dielectric layer 38 that covers the inner wall of the opening 30 and fills the recess regions 34, and partially etching the data storage layer to remain the data storage layer in the recess regions 34.

[00133] Referring to FIGS. 1 and 13F, a first upper insulating layer 53 may be formed on the mold structure (e.g., the mold structure 20 of FIG. 13E). A lower horizontal connection pattern 59 may be connected to the channel semiconductor layer 44, while replacing the lower horizontal mold layer (e.g., the lower horizontal mold layer 15 of FIG. 13E) with the lower horizontal connection pattern 59. For example, a preliminary trench passing through the first upper insulating layer 53, the mold structure (e.g., the mold structure 20 of FIG. 13E), the upper horizontal connection pattern 17,

and the third lower horizontal mold layer (e.g., the third lower horizontal mold layer 15c of FIG. 13E), and exposing the second lower horizontal mold layer (e.g., the second lower horizontal mold layer 15b of FIG. 13e) may be formed, a sacrificial spacer may be formed on a side wall of the preliminary trench, and the second lower horizontal mold layer (e.g., the second lower horizontal mold layer 15b of FIG. 13E) may be removed. Then, the first lower horizontal mold layer (e.g., first lower horizontal mold layer 15a of FIG. 13E), the third lower horizontal mold layer (e.g., the third lower horizontal mold layer 15c of FIG. 13E), the first dielectric layer 38 disposed between the lower horizontal mold layer (e.g., lower horizontal mold layer 15 of FIG. 13E) and the channel semiconductor layer 44, the data storage pattern of any one of the data storage patterns 40, and the second dielectric layer 42 may be sequentially etched, and a portion of the lower reinforcing pattern 36L and a portion of the substrate insulating layer 37 may be etched, a space between the lower structure 3 and the upper horizontal connection pattern 17 may be filled, the lower horizontal connection pattern 59 contacting the channel semiconductor layer 44 may be formed, and the sacrificial spacer may be removed. The preliminary trench may be formed as a trench 56 exposing the lower structure 3.

[00134] In an example, the lower horizontal connection pattern 59 and the upper horizontal connection pattern 17 may constitute a horizontal connection structure 62.

[00135] The sacrificial gate layers (e.g., the sacrificial gate layers 24 of FIG. 13E) may be exposed by the trench 56. The sacrificial gate layers (e.g., the sacrificial gate layers 24 of FIG. 13E) exposed by the trench 56 may be replaced with gate layers 65. The formation of the gate layers 65 may include removing the sacrificial gate layers (e.g., the sacrificial gate layers 24 of FIG. 13E) exposed by the trench 56 to form void spaces, forming a first layer 66a conformally covering internal walls of the void spaces,

and forming a second layer 66b filling the void spaces on the first layer 66a. Therefore, each of the gate layers 65 may include the first and second layers 66a and 66b. In an example, the first layer 66a may be formed of an insulating material, and the second layer 66b may be formed of a conductive material. In another example, the first and
5 second layers 66a and 66b may be formed of different conductive materials.

[00136] The gate layers 65 and the interlayer insulating layers 22 may constitute a stack structure 68.

[00137] Subsequently, a separation structure 72 filling the trench 56 may be formed. The separation structure 72 may include a separation spacer 72a on a side wall of the
10 trench 56, and a separation pattern 72b filling the trench 56.

[00138] Referring back to FIGS. 1 to 4, a second upper insulating layer 75 may be formed on the separation structure 72 and the first upper insulating layer 53. A contact plug 78 covering the first and second upper insulating layers 53 and 75 may be formed. A conductive line 81 may be formed on the contact plug 78. The conductive line 81
15 may be a bit line. The conductive line 81 may be electrically connected to the pad pattern 48 of the vertical structure 50 through the contact plug 78.

[00139] Next, a method of forming the semiconductor device described with reference to FIG. 11 will be described with reference to FIGS. 14A to 14C. FIGS. 14A to 14C are cross-sectional views illustrating a method of forming the semiconductor
20 device described with reference to FIG. 11.

[00140] Referring to FIG. 14A, a mold structure 520 may be formed on a lower structure 503. The mold structure 520 may include interlayer insulating layers 522 and sacrificial gate layers 524, alternately and repeatedly stacked. The interlayer insulating layers 522 may be formed of silicon oxide, and the sacrificial gate layers 524 may be
25 formed of a material having etch selectivity with the interlayer insulating layers 522, for

example, silicon nitride.

[00141] The interlayer insulating layers 522 may include a first lower interlayer insulating layer 522L1, a second lower interlayer insulating layer 522L2 on the first lower interlayer insulating layer 522L1, and intermediate interlayer insulating layers 522M on the second lower interlayer insulating layer 522L2, and an upper interlayer insulating layer 522U on the intermediate interlayer insulating layers 522M. The sacrificial gate layers 524 may include a lower sacrificial gate layer 524L between the first lower interlayer insulating layer 522L1 and the second lower interlayer insulating layer 522L2, intermediate sacrificial gate layers 524M on the lower sacrificial gate layer 524L, and one or a plurality of upper sacrificial gate layers 524U on the intermediate sacrificial gate layers 524M.

[00142] An insulating pattern 527 passing through the upper interlayer insulating layer 522U, extending in a downward direction (e.g., toward an upper surface of the lower structure 503), and passing through the one or the plurality of upper sacrificial gate layers 524U may be formed.

[00143] An opening 530 passing through the mold structure 520 and exposing the lower structure 503 may be formed.

[00144] An epitaxial growth process may be performed to form a lower semiconductor pattern 531 epitaxially grown from the lower structure 503. When the lower structure 503 is formed as a silicon substrate, the lower semiconductor pattern 531 may be formed of silicon by an epitaxial growth process. An upper surface of the lower semiconductor patterns 531 may be at a lower vertical level than the intermediate sacrificial gate layers 524M.

[00145] Referring to FIG. 14B, on the lower semiconductor pattern 531, the interlayer insulating layers 522 exposed by the opening 530 may be etched, and

preliminary reinforcing layers 533 may be formed on the side surfaces of the interlayer insulating layers 522. The preliminary reinforcing layers 533 may be formed of polysilicon.

[00146] The preliminary reinforcing layers 533 may include a preliminary reinforcing layer 533 contacting the second lower interlayer insulating layer 522L2 exposed by the opening 530 on the lower semiconductor pattern 531, a preliminary reinforcing layer 533 contacting the upper interlayer insulating layer 522U exposed by the opening 530, and preliminary reinforcing layers 533 contacting the intermediate interlayer insulating layers 522M exposed by the opening 530.

[00147] Referring to FIG. 14C, an oxidation process may be performed to oxidize surfaces of the preliminary reinforcing layers 533 and the lower semiconductor pattern 531, to form reinforcing patterns 536.

[00148] The reinforcing patterns 536 may include a lower reinforcing pattern 536L formed by oxidizing a preliminary reinforcing layer 533 contacting the second lower interlayer insulating layer 522L2 and an upper surface of the lower semiconductor pattern 531, an upper reinforcing pattern 536U formed by oxidizing a preliminary reinforcing layer 533 contacting the upper interlayer insulating layer 522U, and intermediate reinforcing patterns 536M formed by oxidizing preliminary reinforcing layers 533 contacting the intermediate interlayer insulating layers 522M.

[00149] Subsequently, a first dielectric layer 538 may be conformally formed. Data storage patterns 540 may be formed on the first dielectric layer 538. The data storage patterns 540 may be formed between the reinforcing patterns 536 (e.g., between reinforcing pattern 536 that are adjacent in the Z direction). The formation of the data storage patterns 540 may include forming a data storage layer on the first dielectric layer 538, and partially etching the data storage layer to allow the data storage layer to

remain between the reinforcing patterns 536.

[00150] Referring back to FIG. 11, a second dielectric layer 542 may be conformally formed on the data storage patterns 540, and lower portions of the first and second dielectric layers 538 and 542 may be etched to expose at least a portion of an upper surface of the lower semiconductor pattern 531. A channel semiconductor layer 544 covering the second dielectric layer 542 and the lower semiconductor pattern 531 may be conformally formed, an insulating core region 546 partially filling the opening 530 may be formed on the channel semiconductor layer 544, and a pad pattern 548 may be formed on the insulating core region 546. Therefore, a vertical structure 550 including the lower semiconductor pattern 531, the first dielectric layer 538, the data storage patterns 540, the second dielectric layer 542, the channel semiconductor layer 544, the insulating core region 546, and the pad pattern 548 may be formed in the opening 530.

[00151] A first upper insulating layer 553 may be formed on the mold structure (e.g., the mold structure 520 of FIG. 14C). A trench passing through the first upper insulating layer 553 and the mold structure (e.g., the mold structure 520 of FIG. 14C) may be formed, the sacrificial gate layers (e.g., the sacrificial gate layers 524 of FIG. 14C) exposed by the trench may be removed to form void spaces, gate layers 565 filling the void spaces may be formed, and a separation structure 572 filling the trench may be formed.

[00152] A second upper insulating layer 575 may be formed on the separation structure 572 and the first upper insulating layer 553. A contact plug 578 passing through the first and second upper insulating layers 553 and 575 and being electrically connected to the pad pattern 548 of the vertical structure 550 may be formed. A conductive line 581 may be formed on the contact plug 578.

[00153] According to embodiments of the present inventive concept, a

semiconductor device capable of improving a degree of integration, and a method of forming the same may be provided. The semiconductor device according to the example embodiment may include a data storage pattern isolated in a vertical direction. Since the data storage pattern is isolated in the vertical direction, the retention characteristics of charge trapped in the data storage pattern may be improved.

[00154] While example embodiments have been illustrated and described above, it will be apparent to those skilled in the art that modifications and variations could be made without departing from the scope of the present inventive concept as defined by the appended claims.

CLAIMS

What is claimed is:

1. A semiconductor device comprising:
 - a lower structure;
 - a stack structure on the lower structure and having an opening;
 - a vertical structure in the opening;
 - a contact structure on the vertical structure; and
 - a conductive line on the contact structure,wherein the stack structure includes a plurality of gate layers and a plurality of interlayer insulating layers,
 - wherein the vertical structure includes an insulating core region, a channel semiconductor layer, a plurality of data storage patterns, a first dielectric layer, and a second dielectric layer,
 - wherein the insulating core region extends in a vertical direction, the vertical direction being perpendicular to an upper surface of the lower structure,
 - wherein the channel semiconductor layer covers a side surface and a lower surface of the insulating core region,
 - wherein the plurality of data storage patterns are between the channel semiconductor layer and the plurality of gate layers, and are spaced apart from each other in the vertical direction,
 - wherein at least a portion of the first dielectric layer is disposed between the plurality of data storage patterns and the plurality of gate layers,
 - wherein at least a portion of the second dielectric layer is disposed between the plurality of data storage patterns and the channel semiconductor layer, and

wherein the insulating core region includes a plurality of first convex portions having increased widths in regions facing the plurality of gate layers.

2. The semiconductor device according to claim 1, wherein the insulating core region further includes a plurality of second convex portions having increased widths in regions facing the plurality of interlayer insulating layers, and concave portions having decreased widths between the plurality of first convex portions and the plurality of second convex portions.

3. The semiconductor device according to claim 1 or claim 2, wherein each of the plurality of data storage patterns includes a first side surface facing a corresponding one of the plurality of gate layers, and a second side surface facing the channel semiconductor layer,

wherein each of the plurality of data storage patterns includes a first portion adjacent to the first side surface, a second portion adjacent to the second side surface, and a minimum vertical thickness portion between the first portion and the second portion, and

wherein a thickness of the minimum vertical thickness portion is less than a maximum vertical thickness of the first portion and a maximum vertical thickness of the second portion.

4. The semiconductor device according to claim 3, wherein a distance between the minimum vertical thickness portion and the first side surface is less than a distance between the minimum vertical thickness portion and the second side surface.

5. The semiconductor device according to claim 3, wherein a distance between the minimum vertical thickness portion and the first side surface is greater than a distance between the minimum vertical thickness portion and the second side surface.

6. The semiconductor device according to claim 1 or claim 2, wherein each of the plurality of data storage patterns includes a first side surface facing a corresponding one of the plurality of gate layers, and a second side surface facing the channel semiconductor layer,

wherein at least a portion of the plurality of data storage patterns further include a void between the first side surface and the second side surface, and

wherein a distance between the void and the first side surface is greater than a distance between the void and the second side surface.

7. The semiconductor device according to claim 1 or claim 2, wherein each of the plurality of data storage patterns includes a first side surface facing a corresponding one of the plurality of gate layers, and a second side surface facing the channel semiconductor layer,

wherein at least a portion of the plurality of data storage patterns further include a void between the first side surface and the second side surface, and

wherein a distance between the void and the first side surface is less than a distance between the void and the second side surface.

8. The semiconductor device according to claim 1 or claim 2, wherein each of the plurality of data storage patterns includes a first side surface facing a corresponding one of the plurality of gate layers, and a second side

surface facing the channel semiconductor layer, and

wherein at least a portion of the second side surface is a concave shape.

9. The semiconductor device according to any one of claims 1 to 8, wherein at least one of an upper surface and a lower surface in each of the plurality of data storage patterns is a concave shape.

10. The semiconductor device according to any one of claims 1 to 9, further comprising:

a horizontal connection structure between the lower structure and the stack structure,

wherein the horizontal connection structure includes a lower horizontal connection pattern, and an upper horizontal connection pattern on the lower horizontal connection pattern,

wherein the vertical structure passes through the stack structure, extends in a downward direction to pass through the horizontal connection structure, and extends into the lower structure,

wherein the upper horizontal connection pattern is spaced apart from the channel semiconductor layer of the vertical structure, and

wherein the lower horizontal connection pattern is in contact with the channel semiconductor layer of the vertical structure.

11. The semiconductor device according to claim 10, wherein the insulating core region further includes a lower convex portion facing the lower horizontal connection pattern.

12. The semiconductor device according to any one of claims 1 to 11, wherein the insulating core region further includes concave portions having decreased widths in regions facing the interlayer insulating layers.

13. The semiconductor device according to any one of claims 1 to 11, wherein the insulating core region has constant widths in regions facing the interlayer insulating layers.

14. A semiconductor device comprising:
a lower structure;
a stack structure including an interlayer insulating layer and a gate layer sequentially stacked on the lower structure; and
a vertical structure passing through the stack structure,

wherein the vertical structure includes an insulating core region passing through the interlayer insulating layer and the gate layer, a channel semiconductor layer covering at least a side surface of the insulating core region, a data storage pattern between the channel semiconductor layer and the gate layer, a first dielectric layer at least interposed between the data storage pattern and the gate layer, and a second dielectric layer at least interposed between the data storage pattern and the channel semiconductor layer,

wherein the data storage pattern has a first side surface facing the gate layer and a second side surface facing the channel semiconductor layer, and

wherein the second side surface of the data storage pattern has a concave portion.

15. The semiconductor device according to claim 14, wherein the second side surface of the data storage pattern has curved shapes on and below the concave portion.

16. The semiconductor device according to claim 14 or claim 15, wherein the insulating core region includes a first concave portion, a first convex portion having a width greater than the first concave portion and disposed on the first concave portion, and a second concave portion having a width less than the first convex portion and disposed on the first convex portion,

wherein the first convex portion faces the data storage pattern, and

wherein a portion having a minimum horizontal width in the first concave portion and a portion having a minimum horizontal width in the second concave portion face the gate layer.

17. The semiconductor device according to claim 16, wherein a distance between the portion having the minimum horizontal width in the first concave portion and the portion having the minimum horizontal width in the second concave portion is less than a thickness of the gate layer in a vertical direction, and greater than a maximum thickness of the data storage pattern in a vertical direction.

18. The semiconductor device according to claim 16 or claim 17, wherein the insulating core region further includes a second convex portion having a width greater than that of the first concave portion and disposed below the first concave portion, and

wherein the second convex portion faces the interlayer insulating layer.

19. The semiconductor device according to claim 18, wherein a distance between a portion having a maximum horizontal width in the second convex portion and the portion having the minimum horizontal width in the first concave portion is greater than a distance between the portion having the minimum horizontal width in the first concave portion and a portion having a maximum horizontal width in the first convex portion.

20. A semiconductor device comprising:

a lower structure;

a stack structure including an interlayer insulating layer and a gate layer sequentially stacked on the lower structure; and

a vertical structure passing through the stack structure,

wherein the vertical structure includes an insulating core region passing through the interlayer insulating layer and the gate layer, a channel semiconductor layer covering at least a side surface of the insulating core region, a data storage pattern between the channel semiconductor layer and the gate layer, a first dielectric layer at least interposed between the data storage pattern and the gate layer, and a second dielectric layer at least interposed between the data storage pattern and the channel semiconductor layer, and

wherein the insulating core region has at least two inflection points in a portion facing the gate layer.