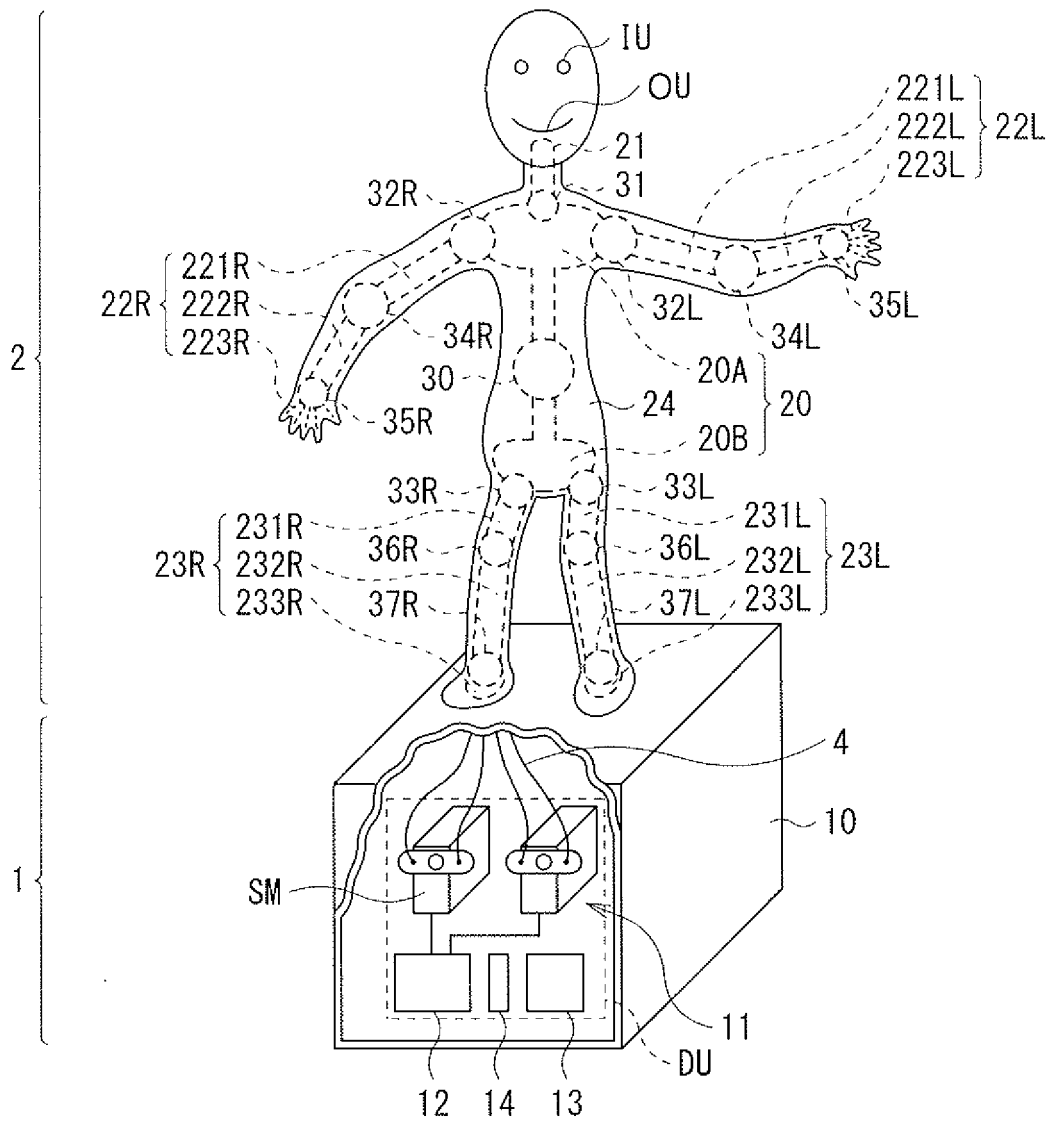
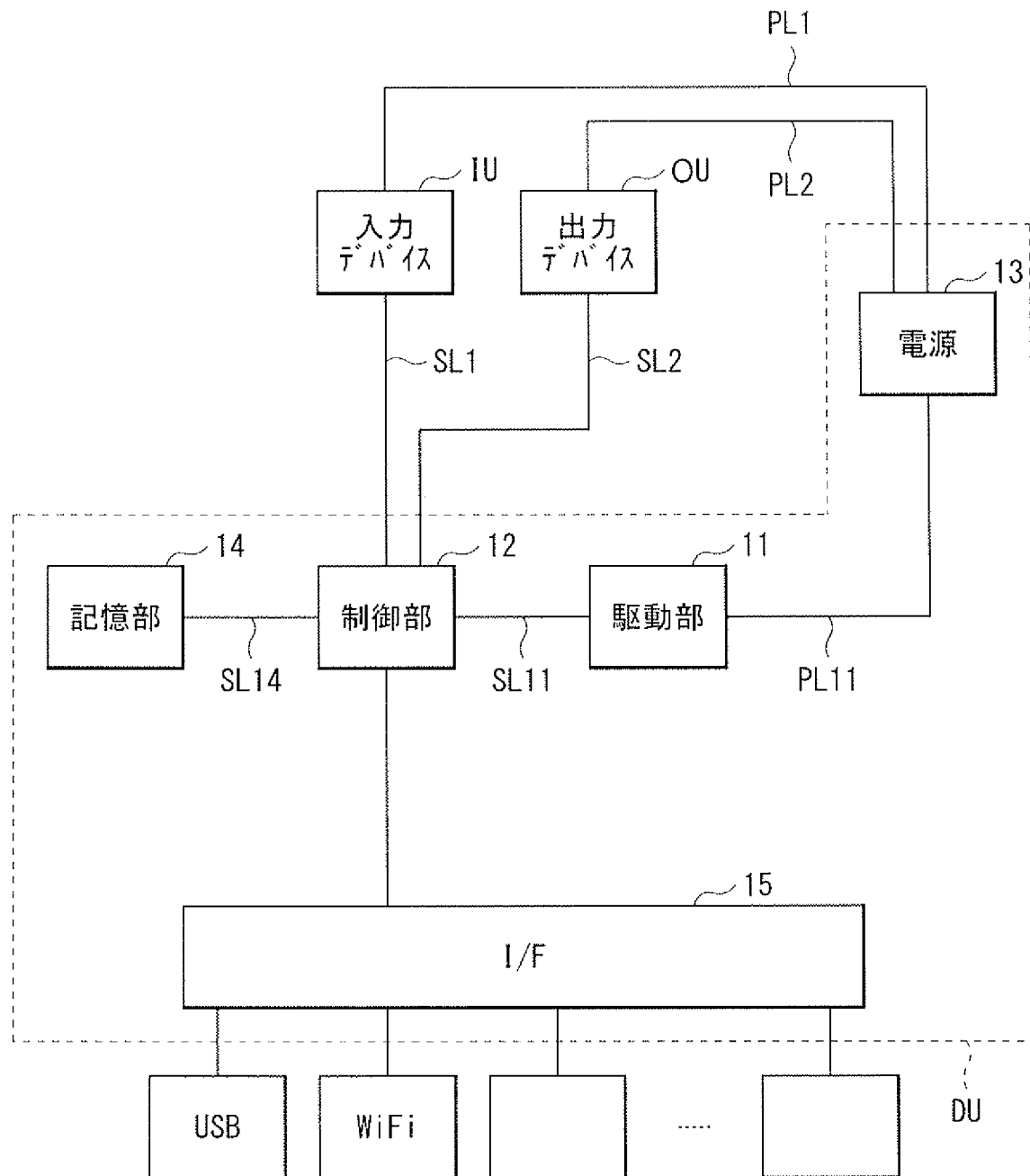


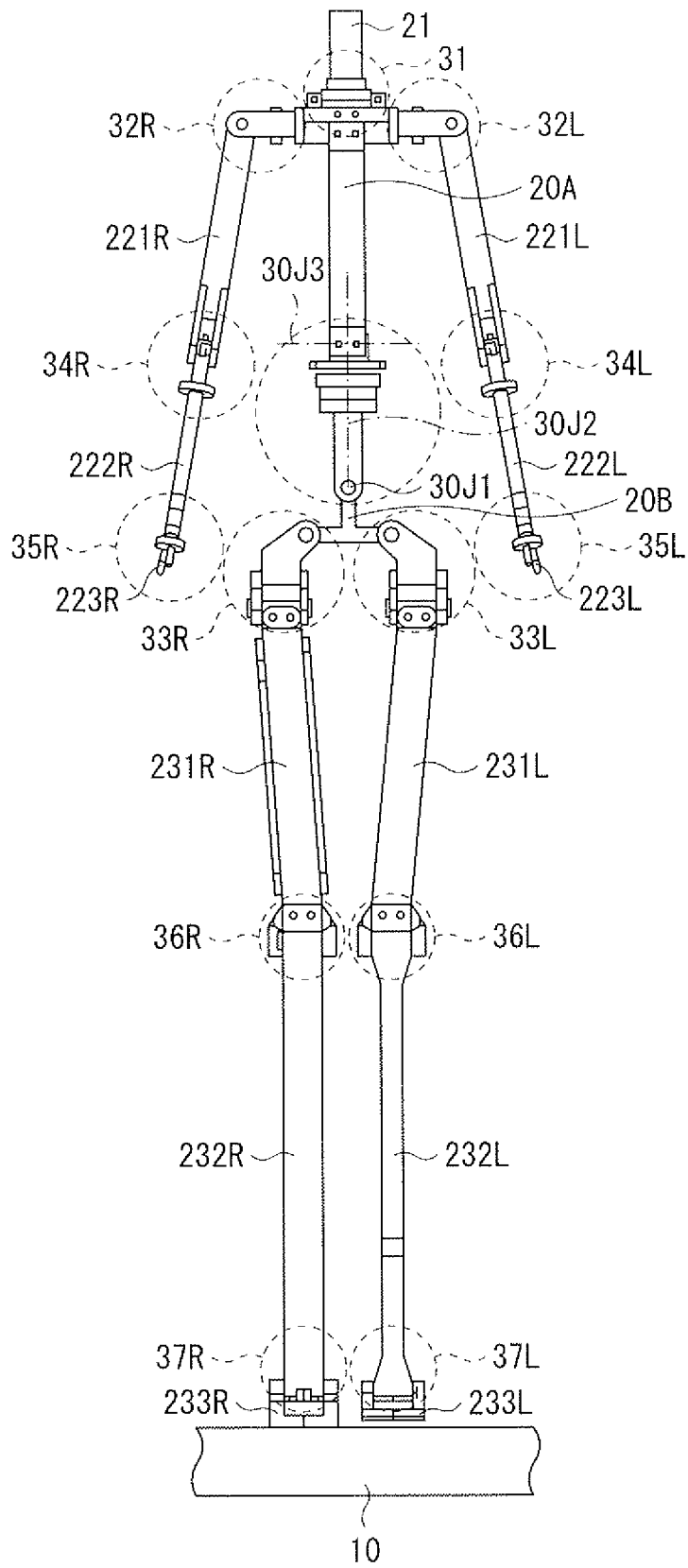
[図1A]



[図1B]



[図1C]

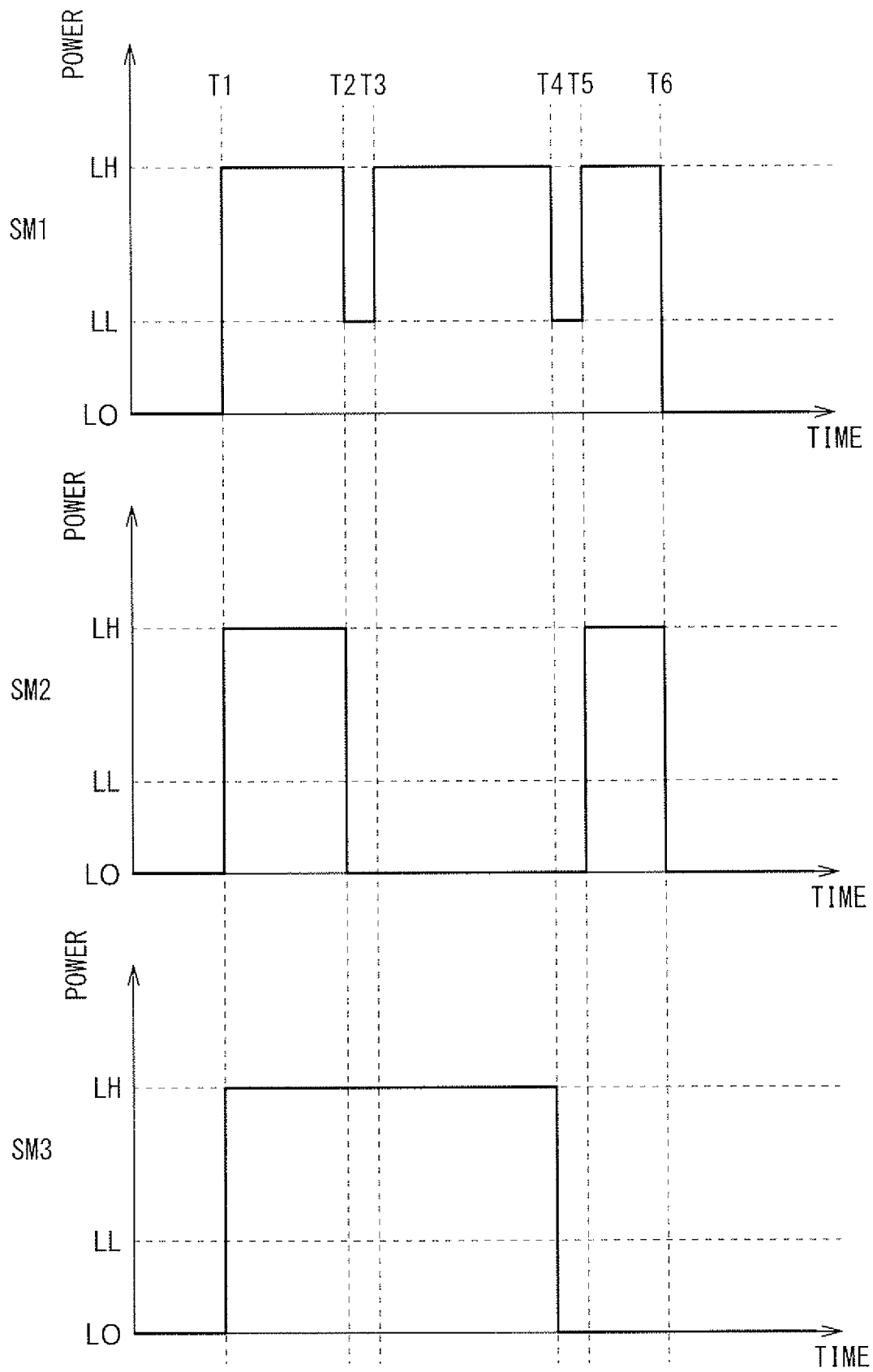


[図1D]

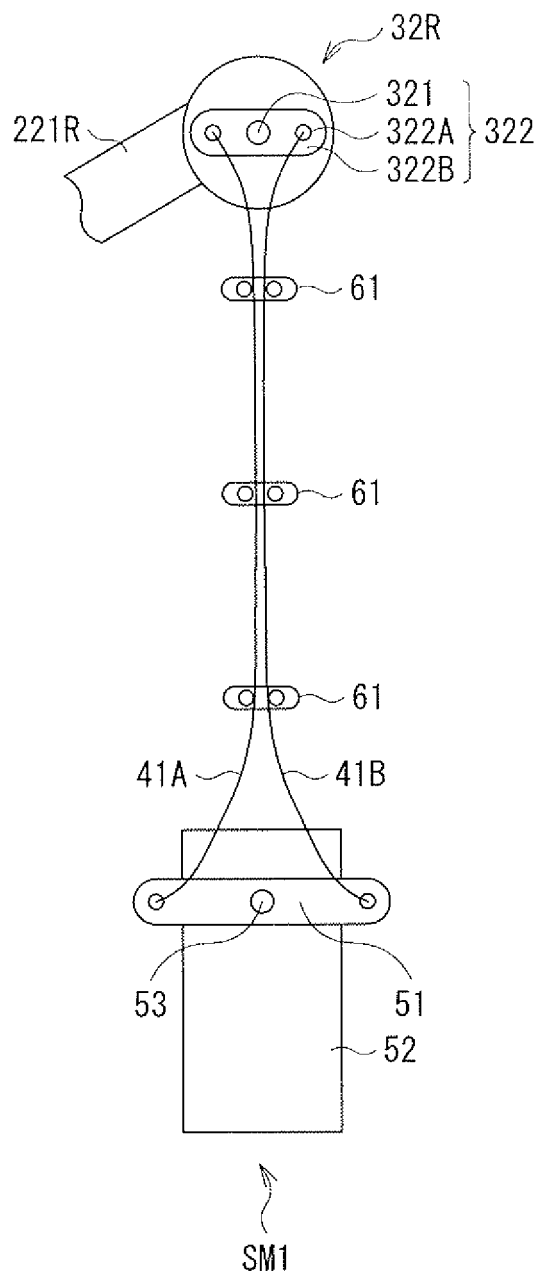




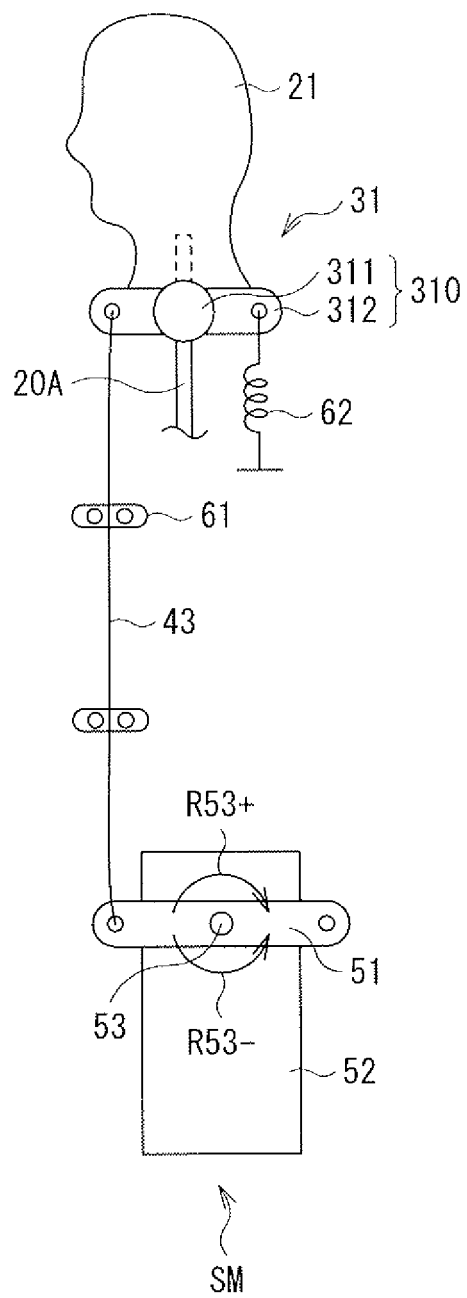
[図2B]



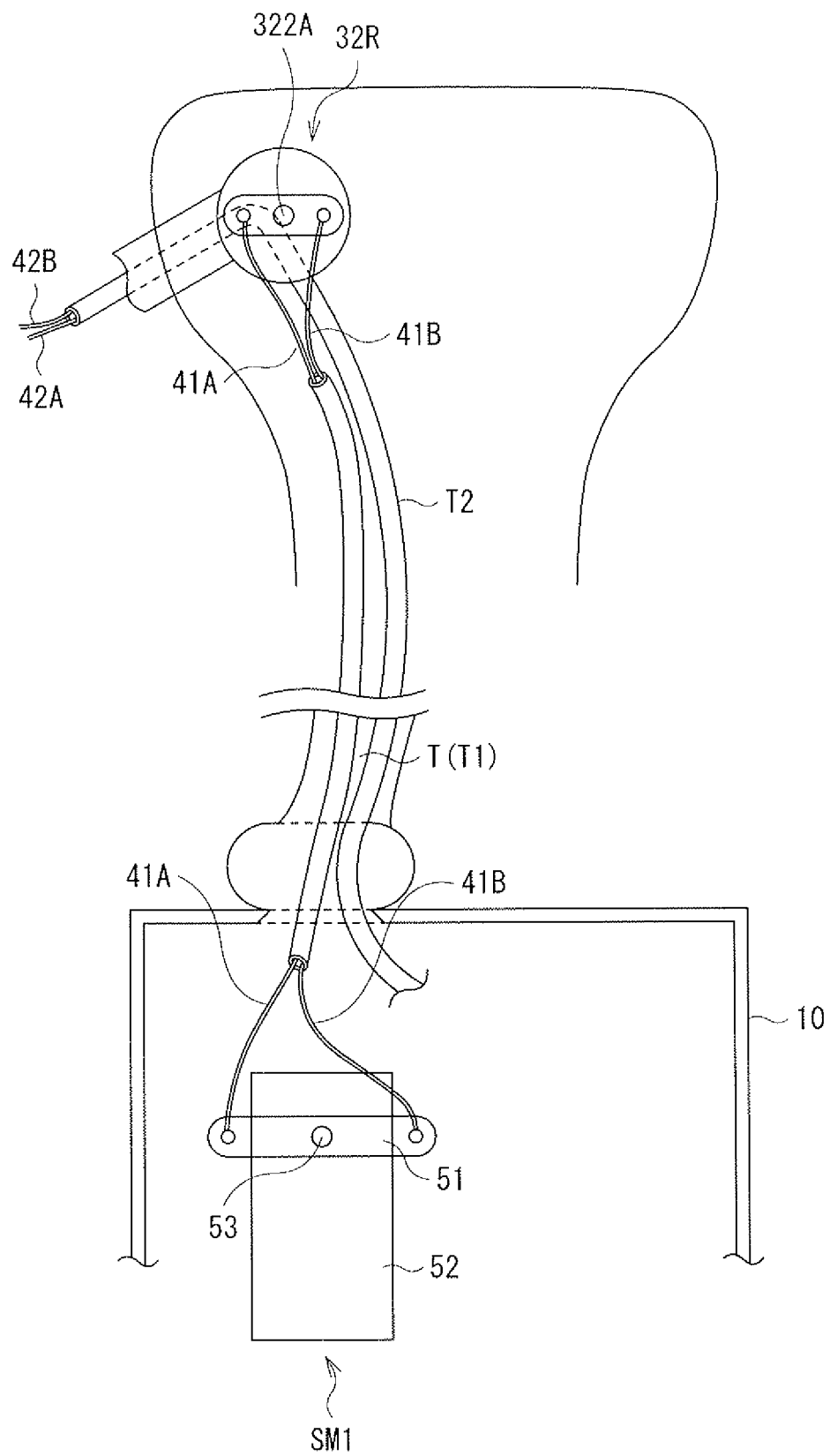
[図3A]



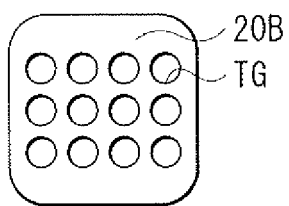
[図3B]



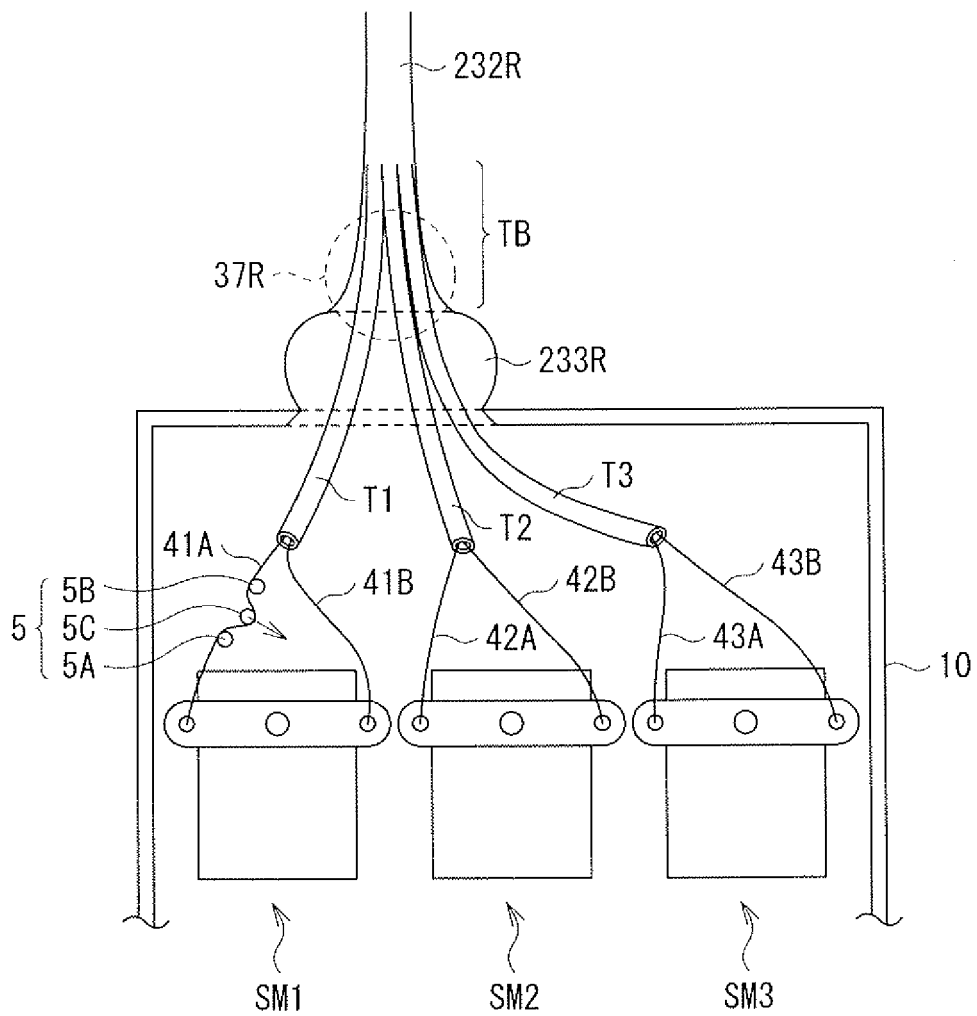
[図4A]



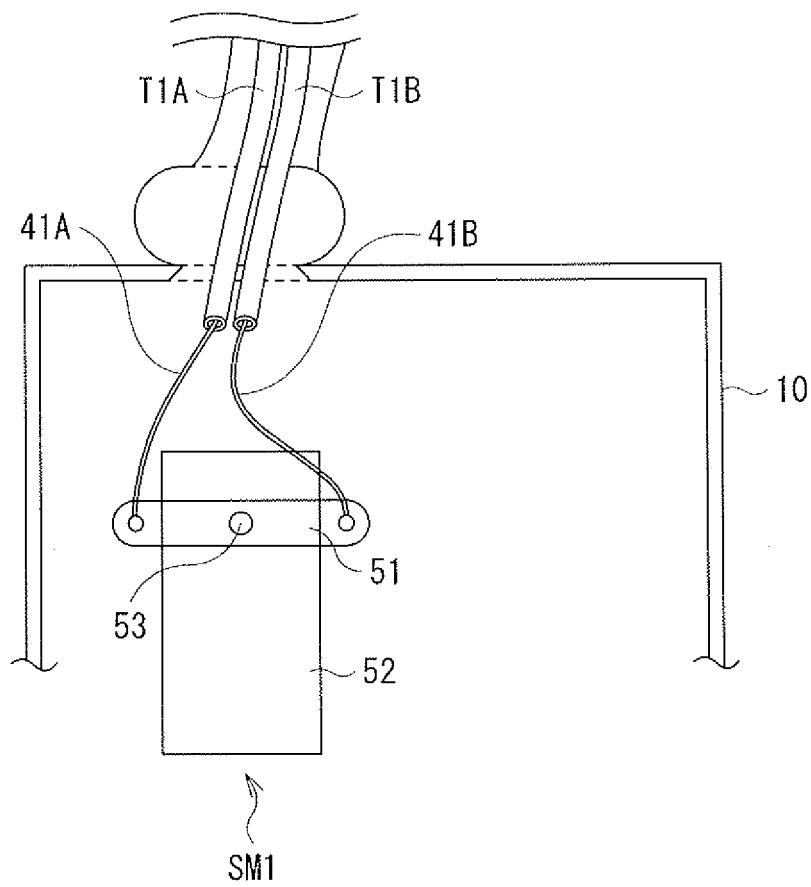
[図4B]



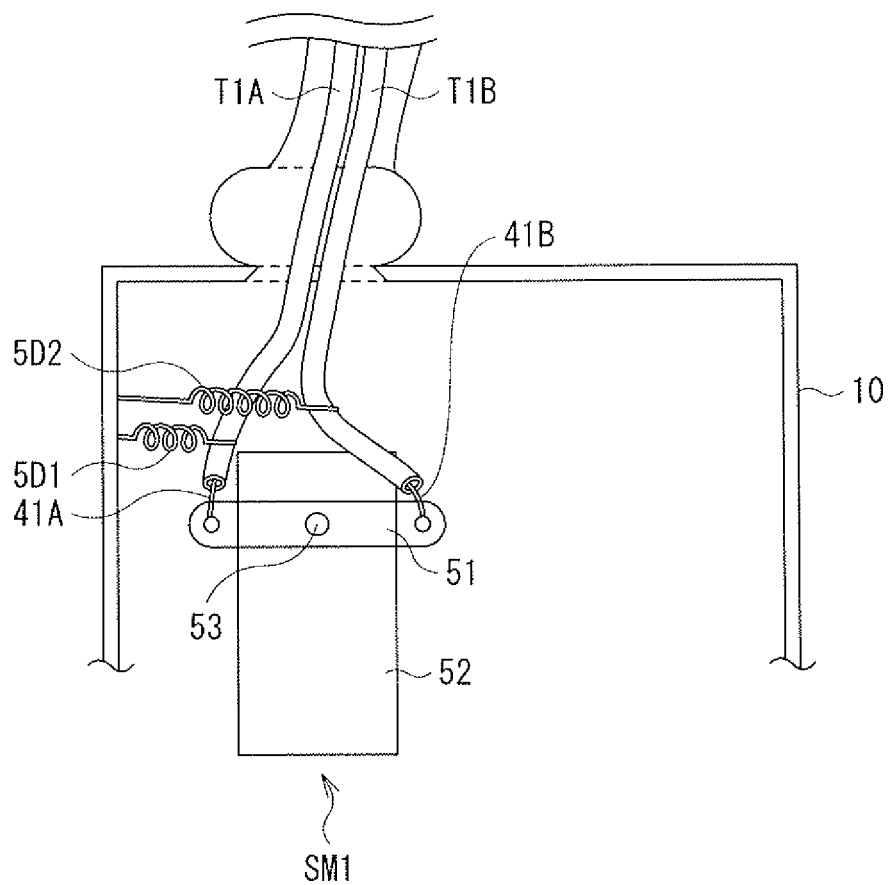
[図4C]



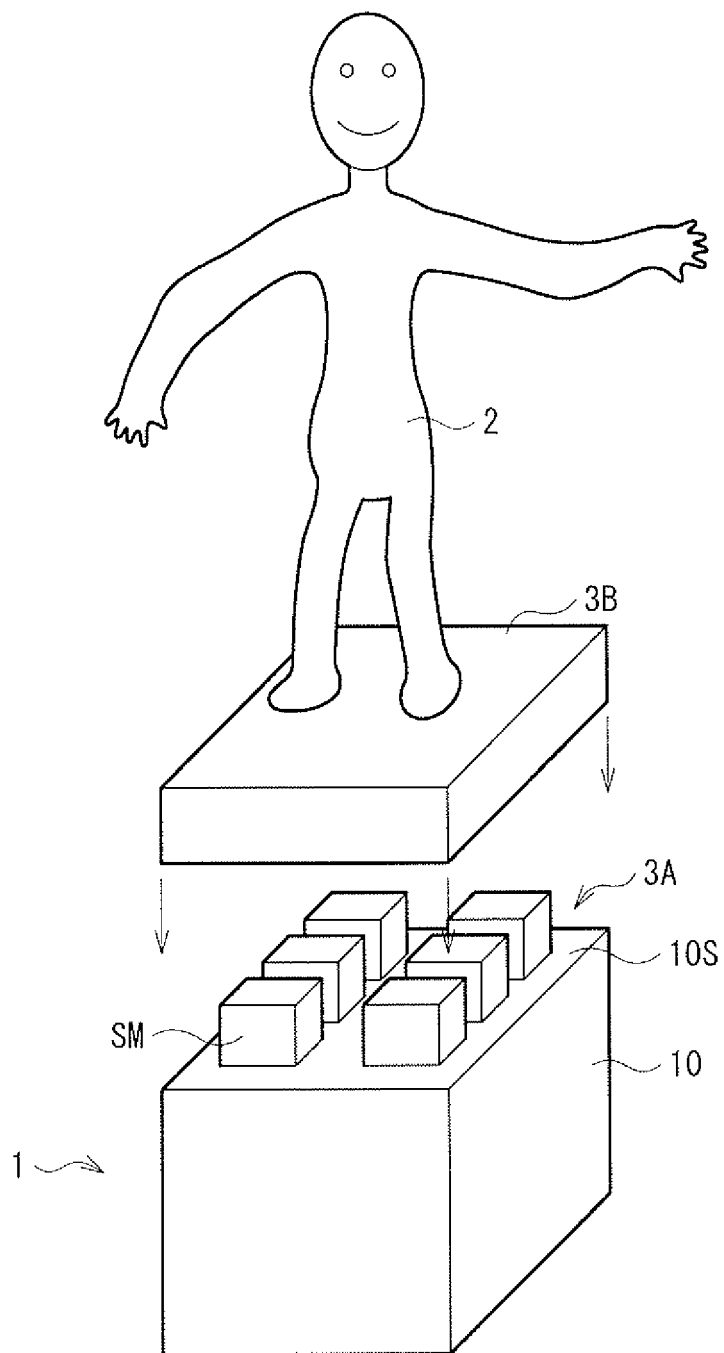
[図5A]



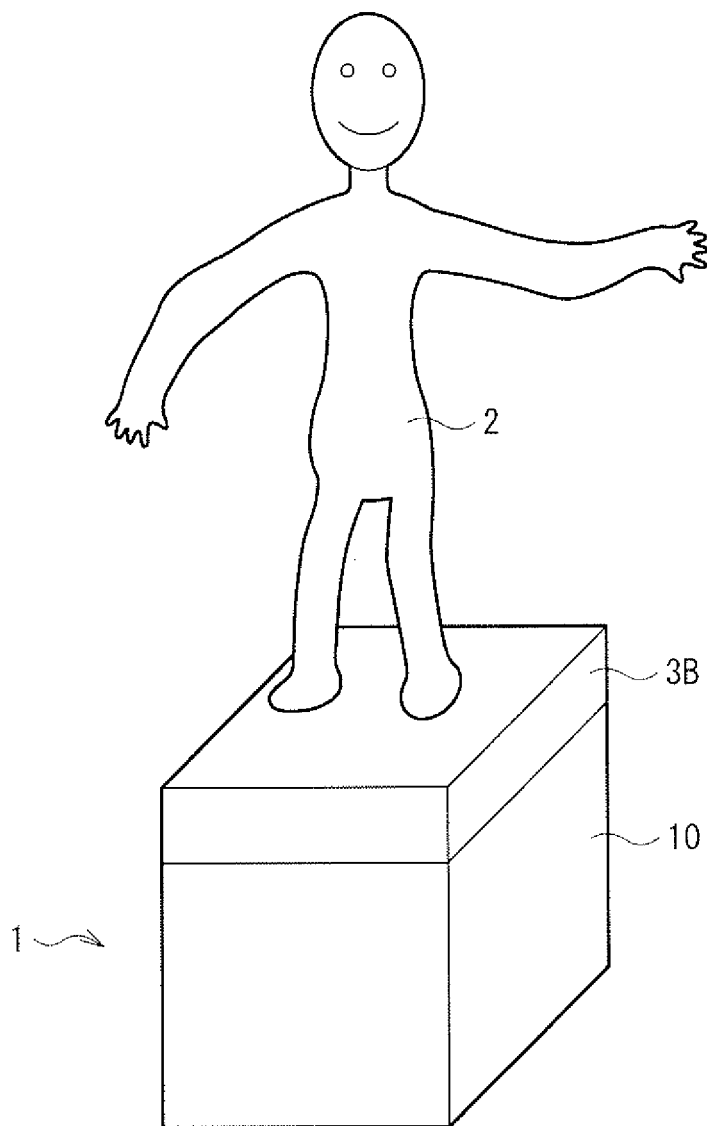
[図5B]



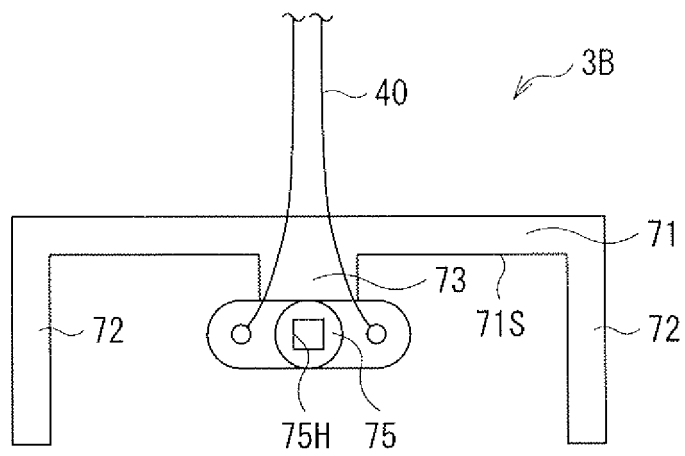
[図6A]



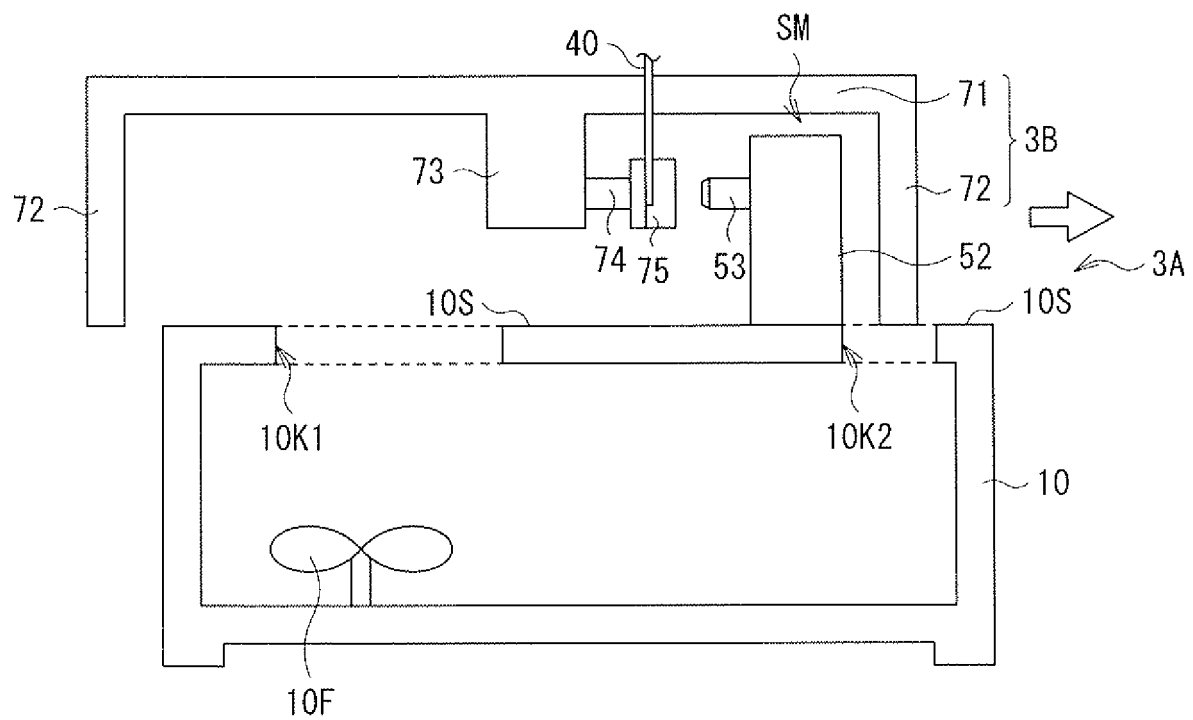
[図6B]



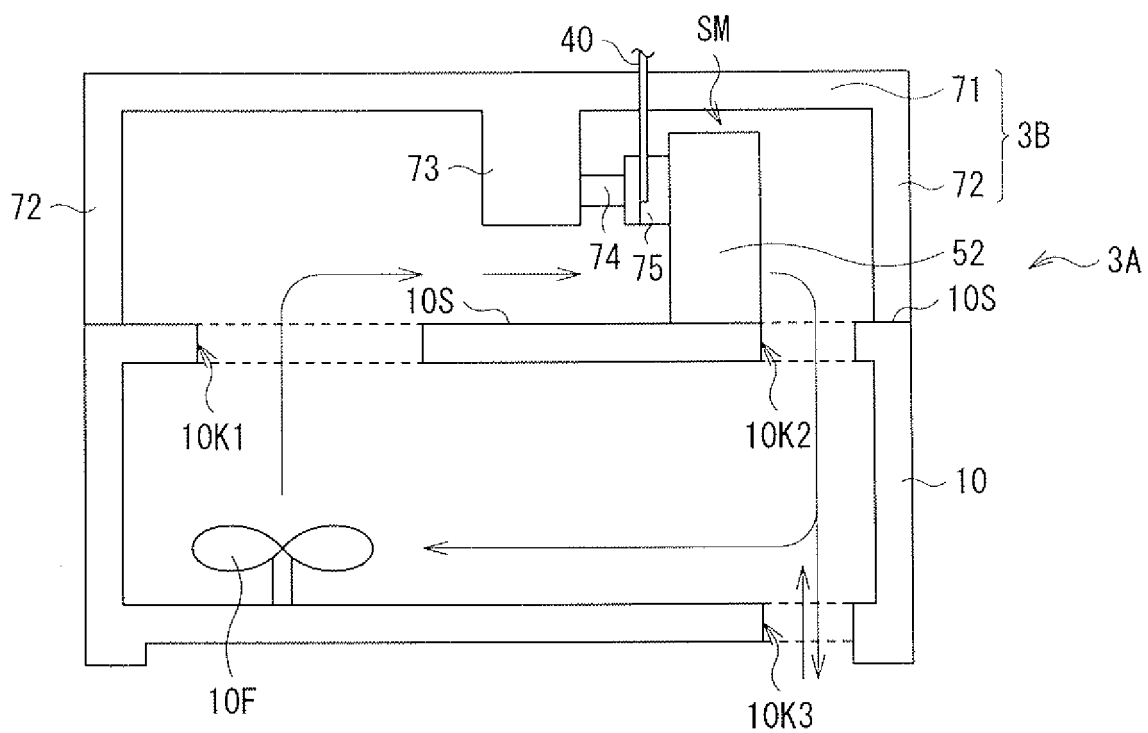
[図7A]



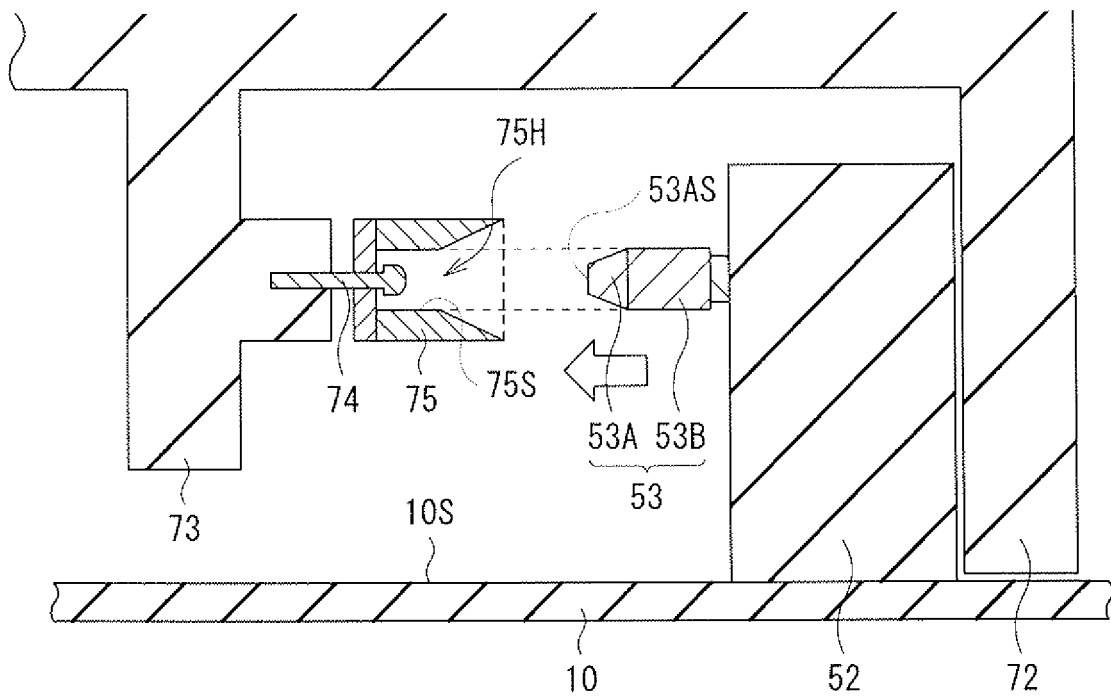
[図7B]



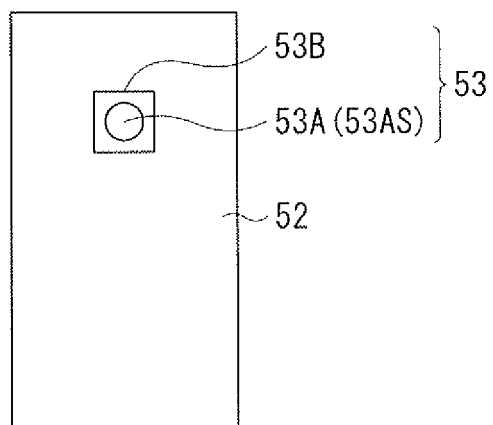
[図7C]



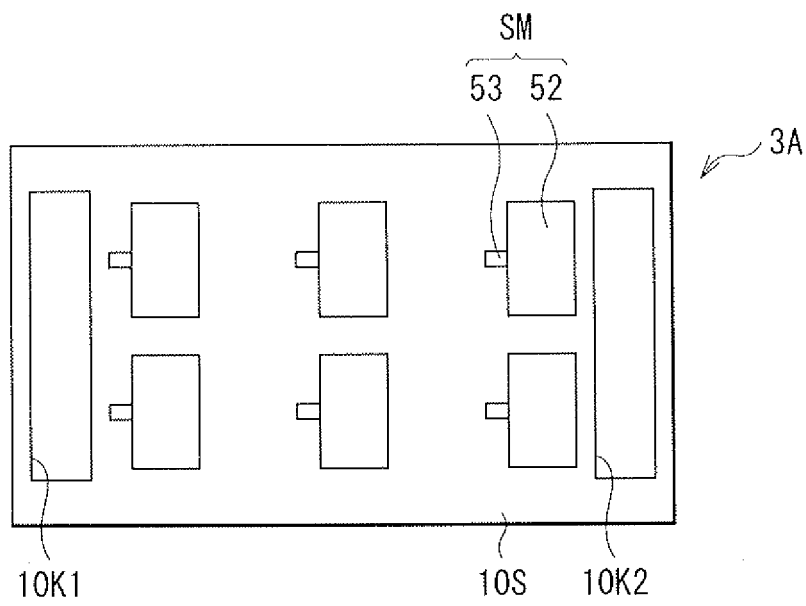
[図7D]



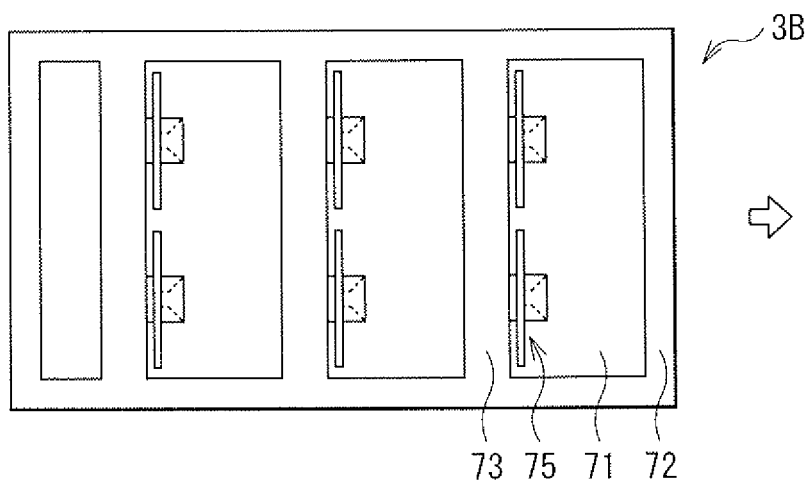
[図7E]

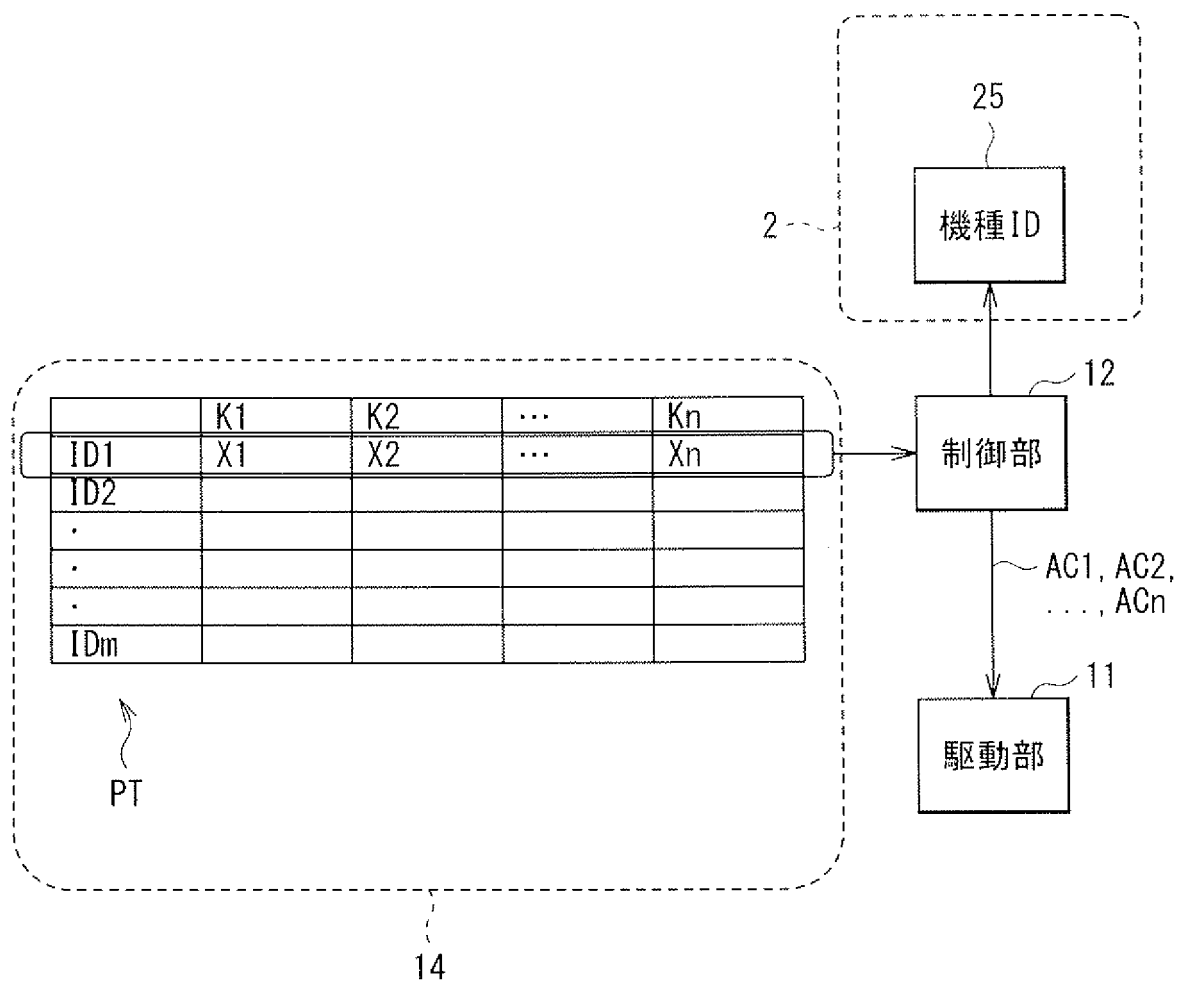
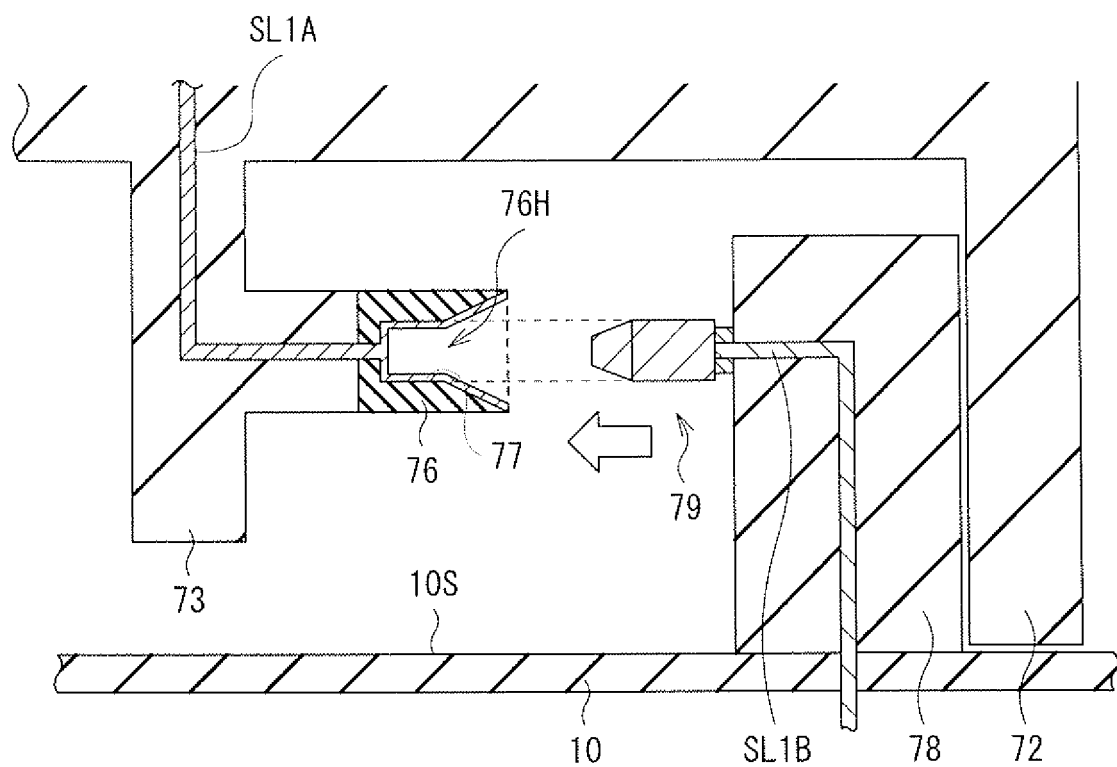


[図7F]

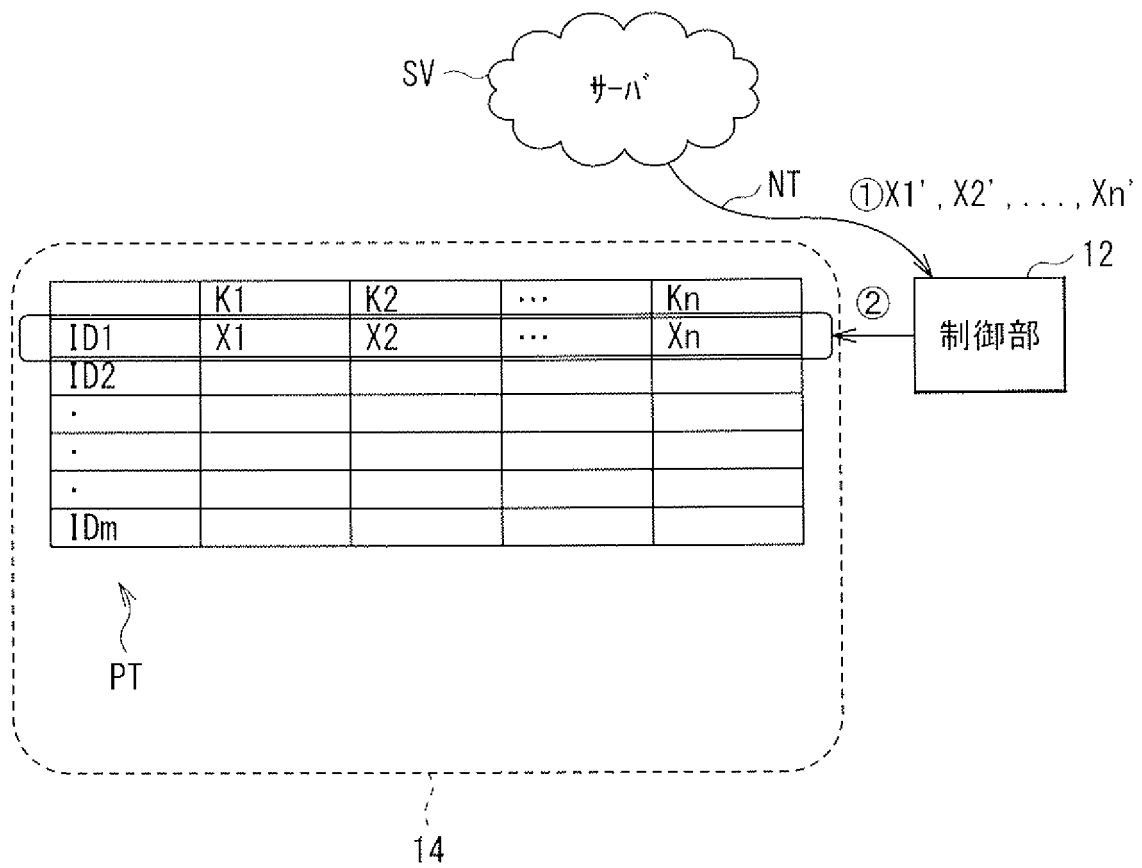


[図7G]

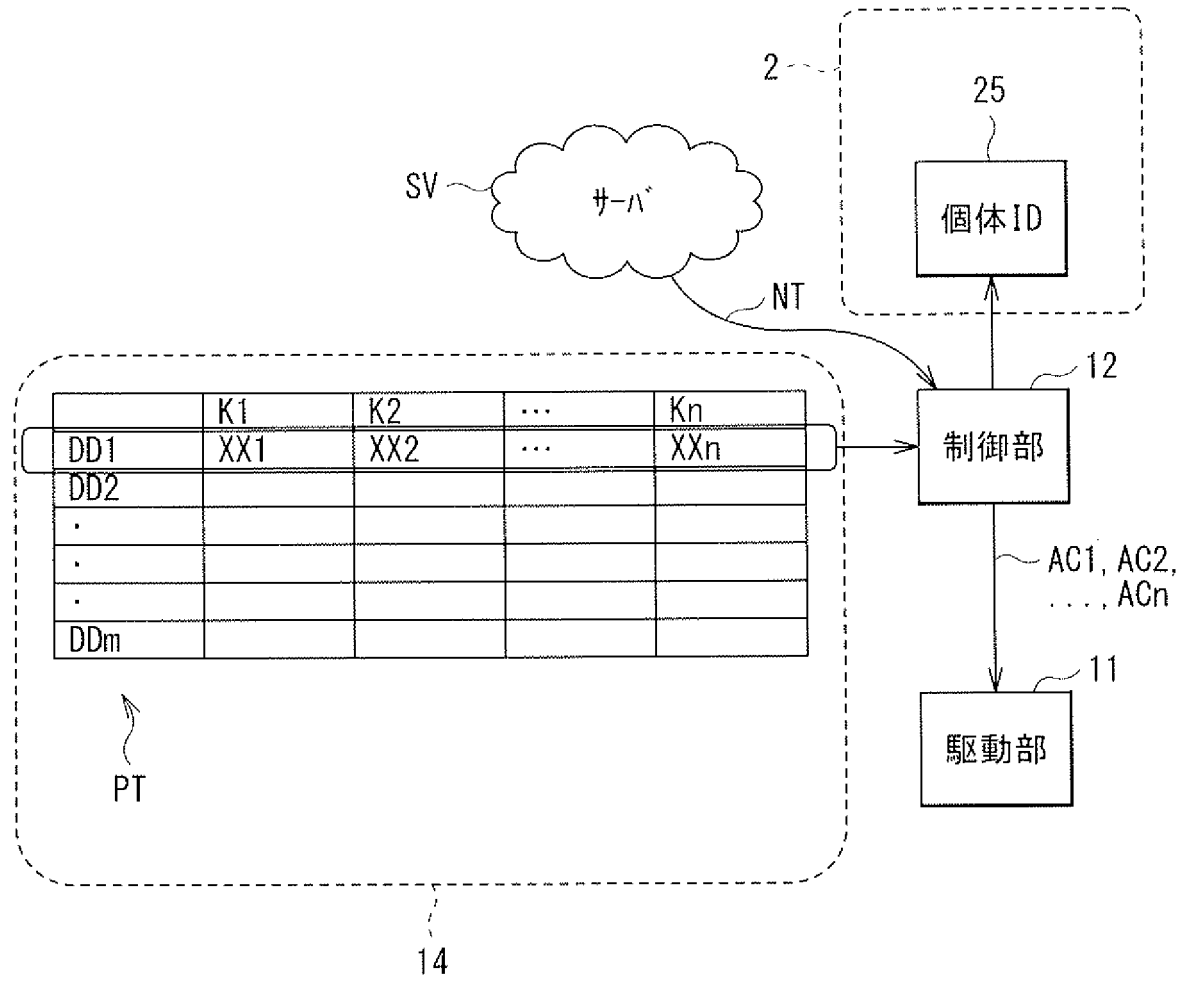




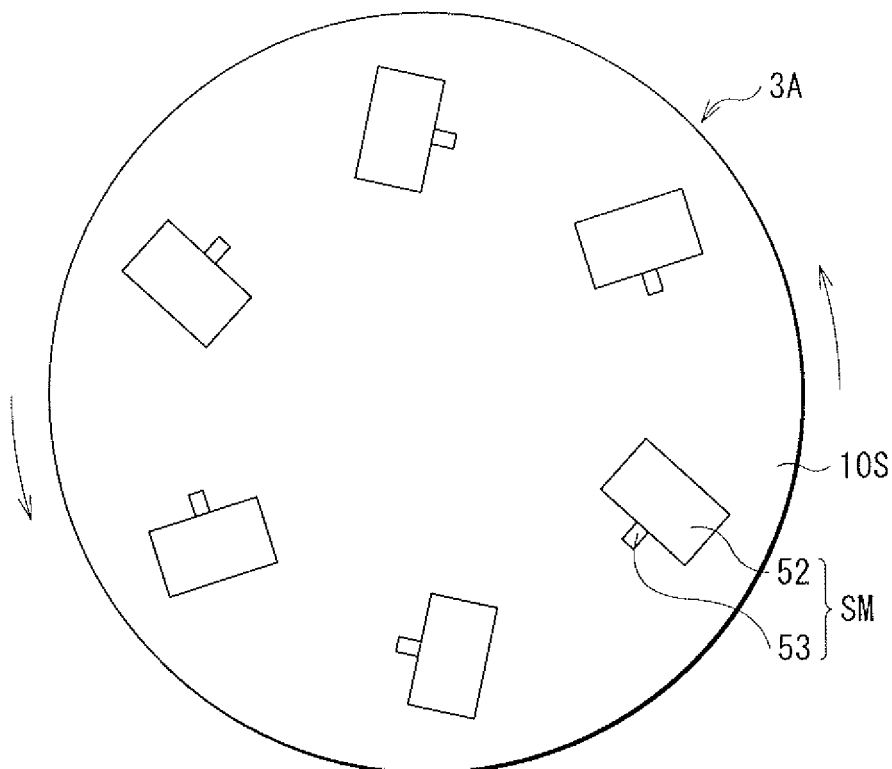
[図10]



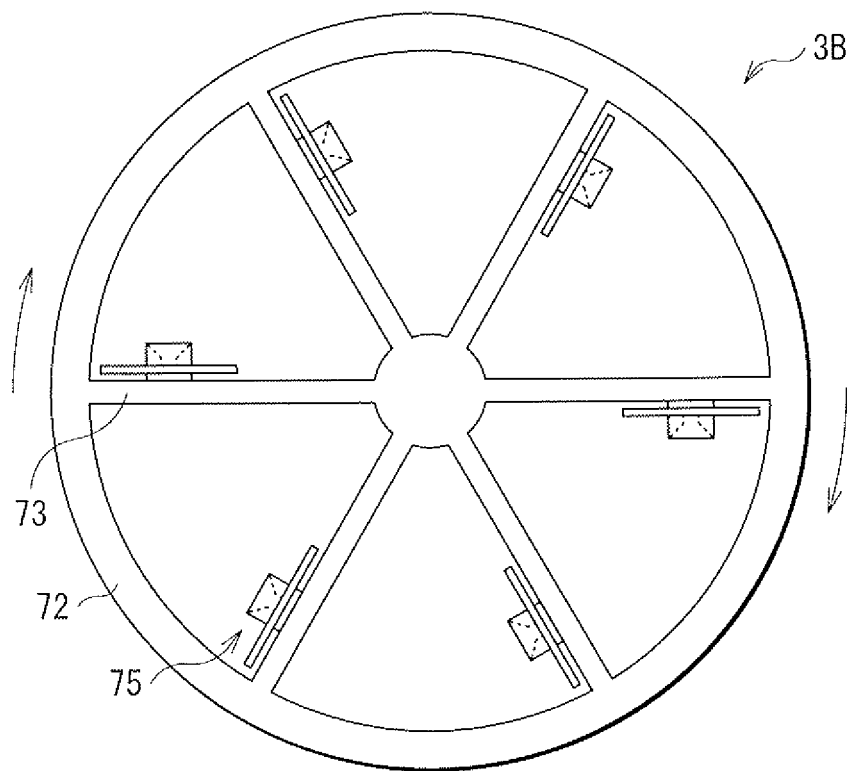
[図11]



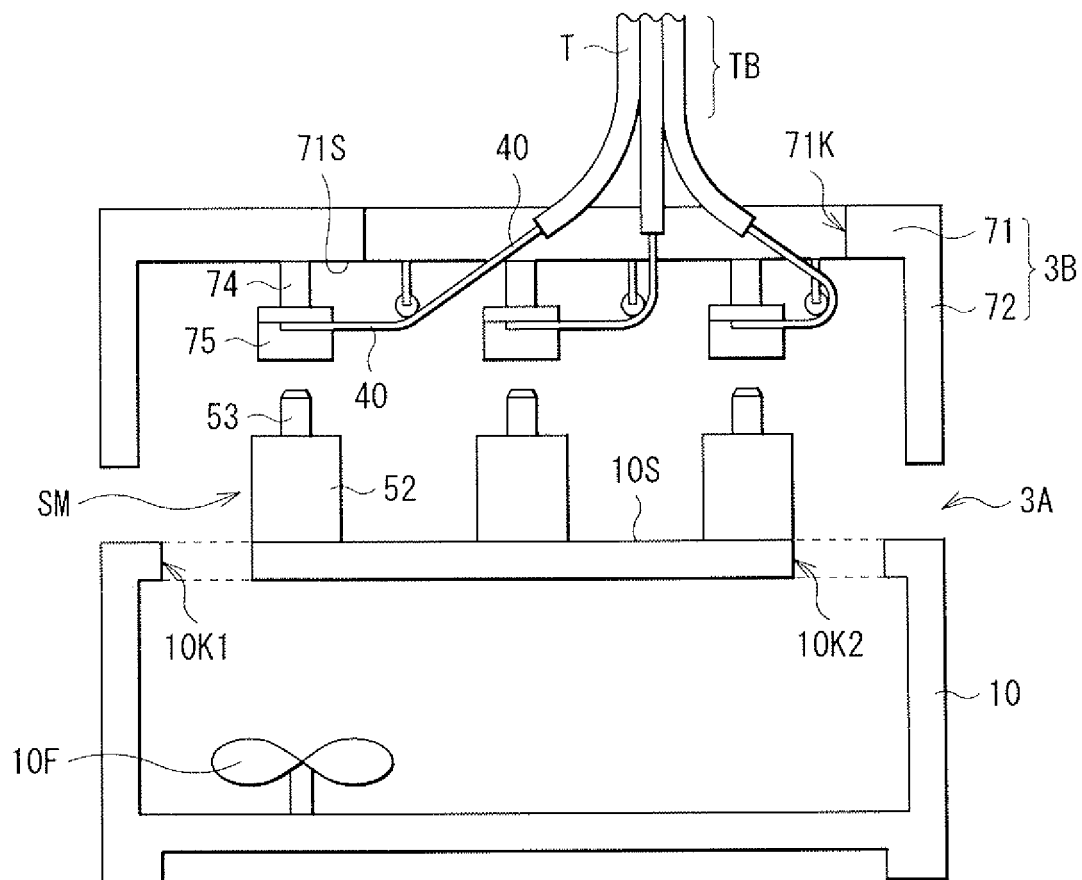
[図12A]



[図12B]

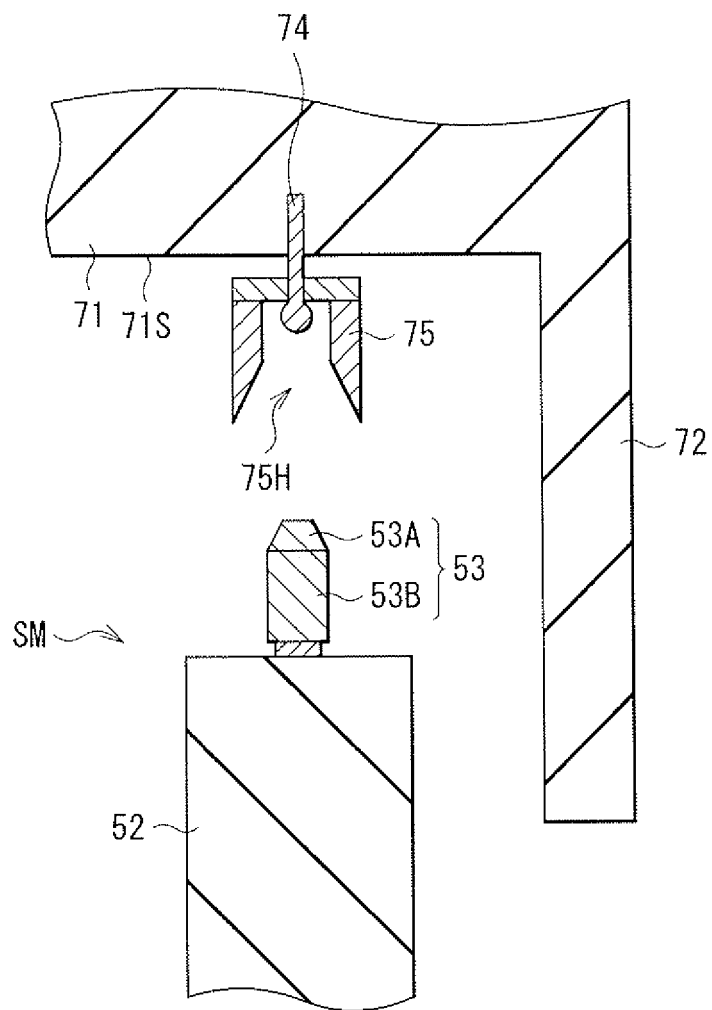


[図13A]

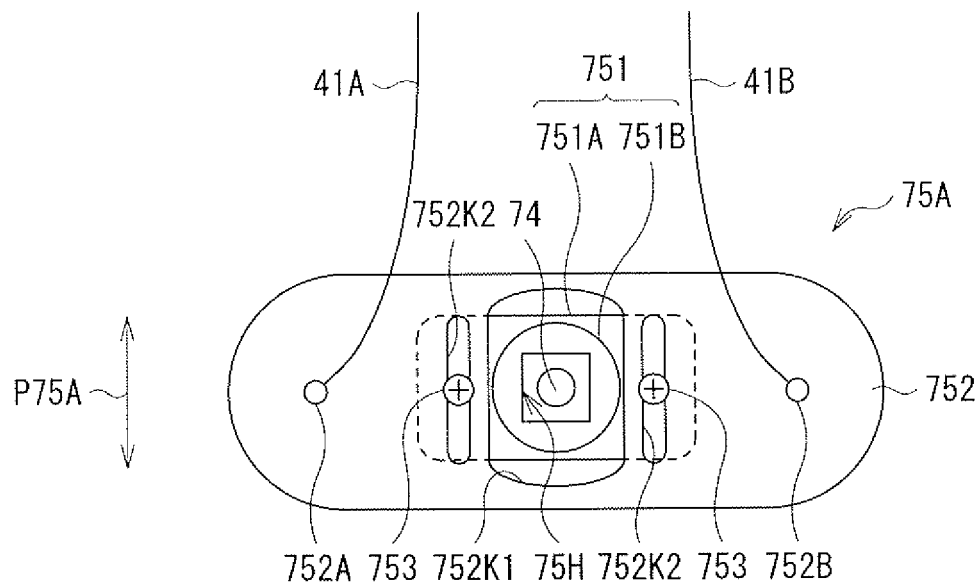




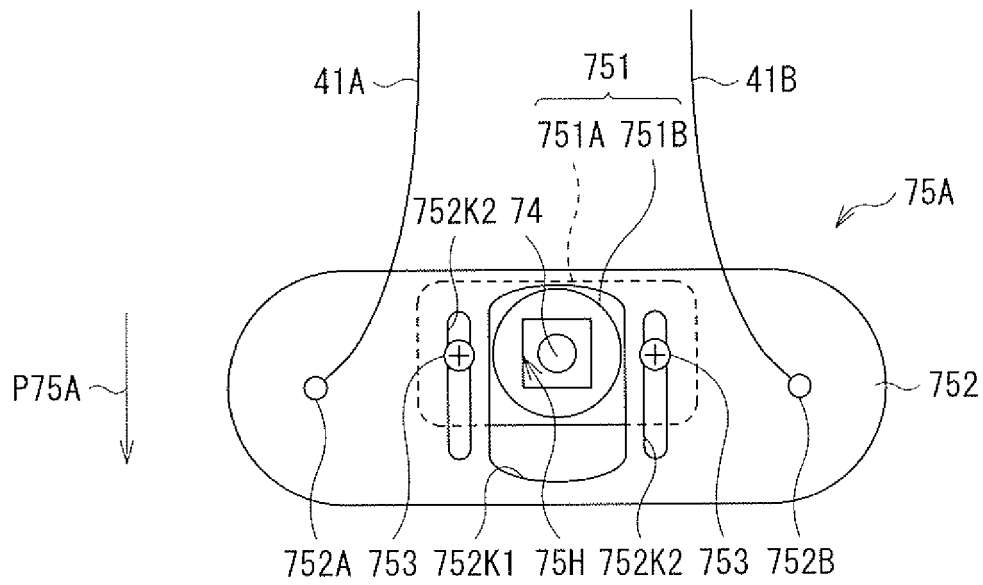
[図13C]



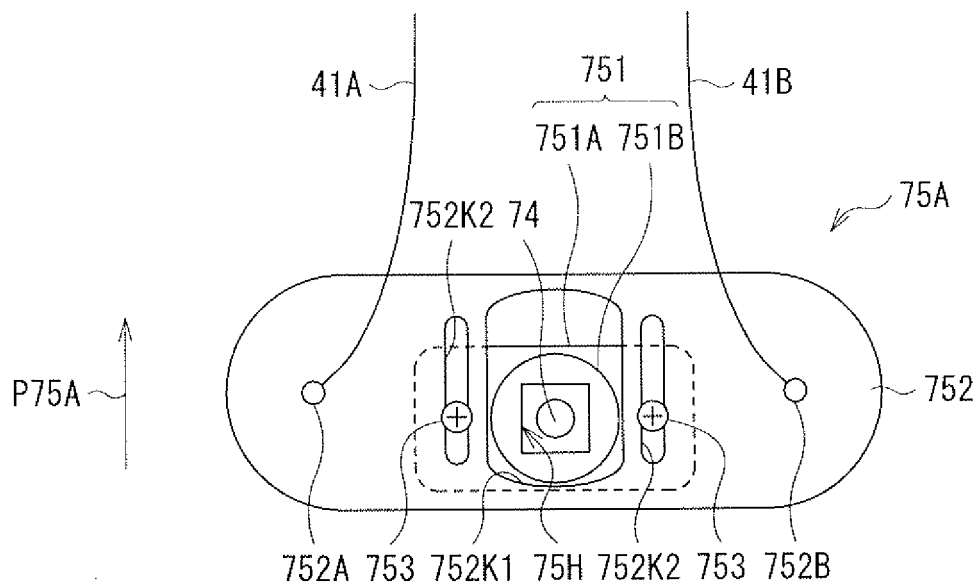
[図14A]



[図14B]



[図14C]



[図14D]

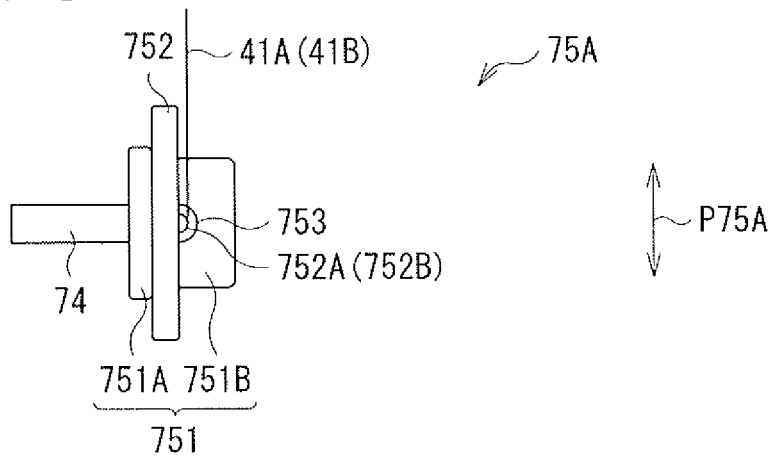
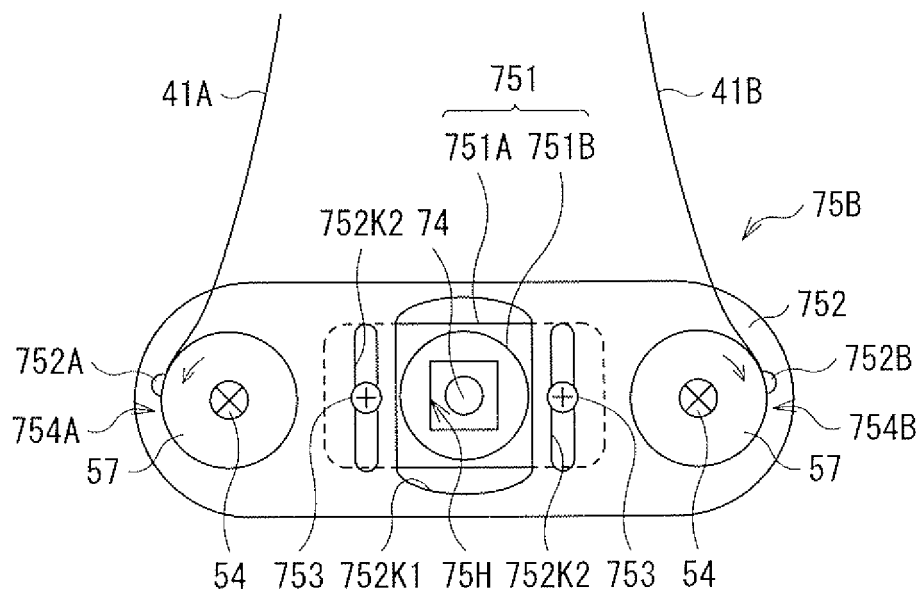
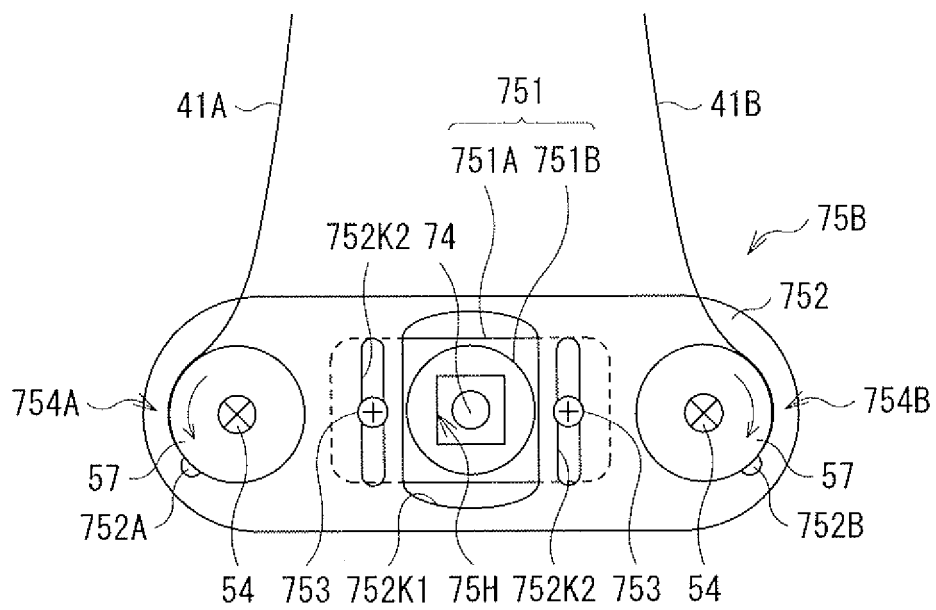


FIG. 7 is a plan view of a semiconductor device. It shows a central square pad 74 surrounded by two vertical pads 752K1 and 752K2, which are flanked by circular pads 754A and 754B. The entire structure is enclosed within a rectangular frame 751. A dashed line indicates a cross-section X-VIA.

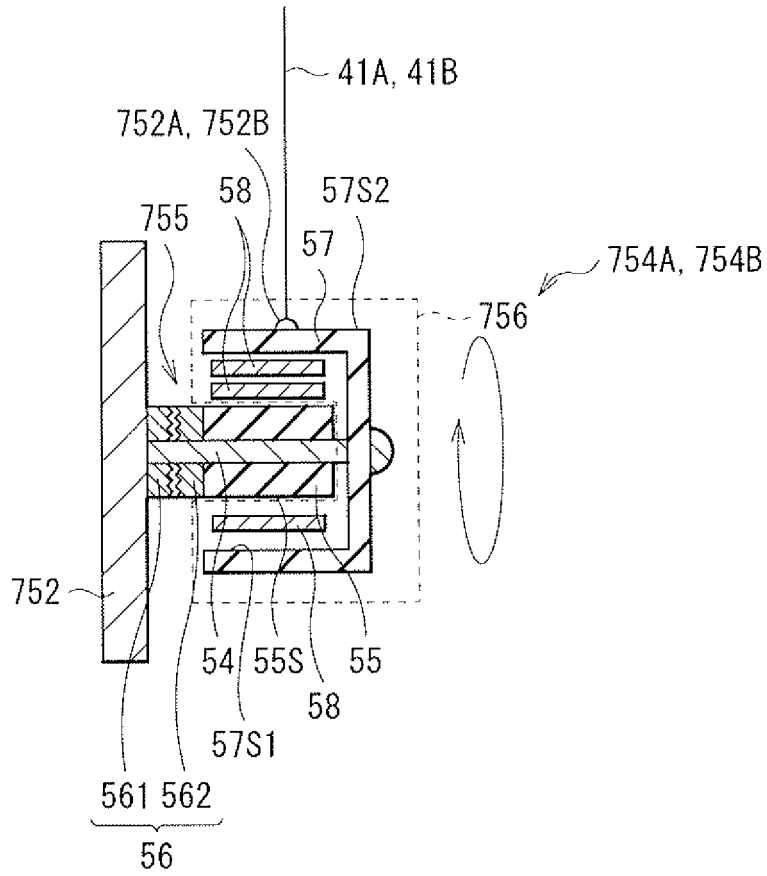
[図15B]



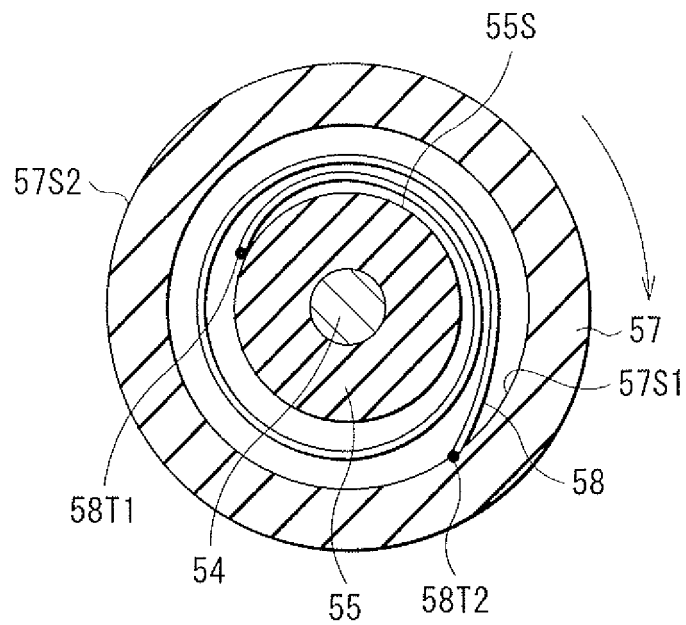
[図15C]



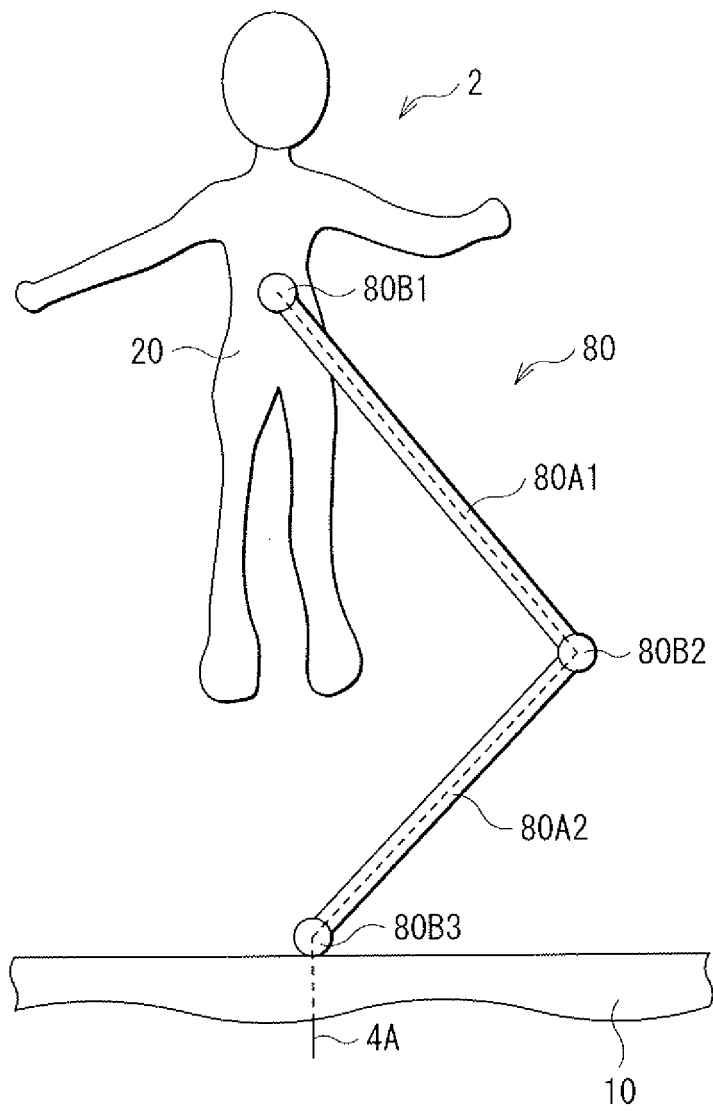
[図16A]



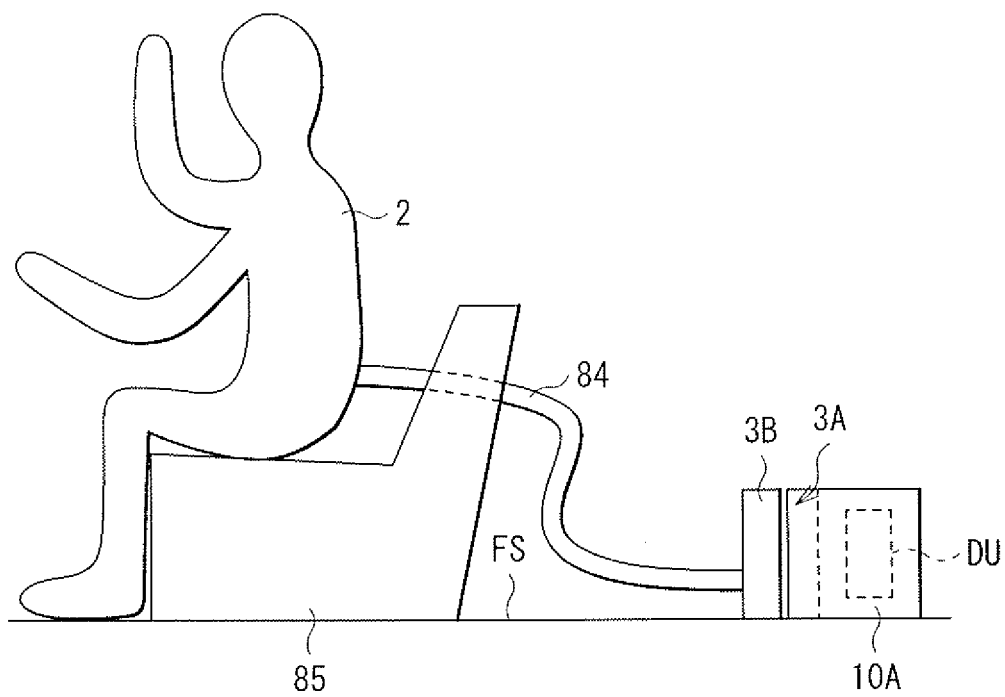
[図16B]



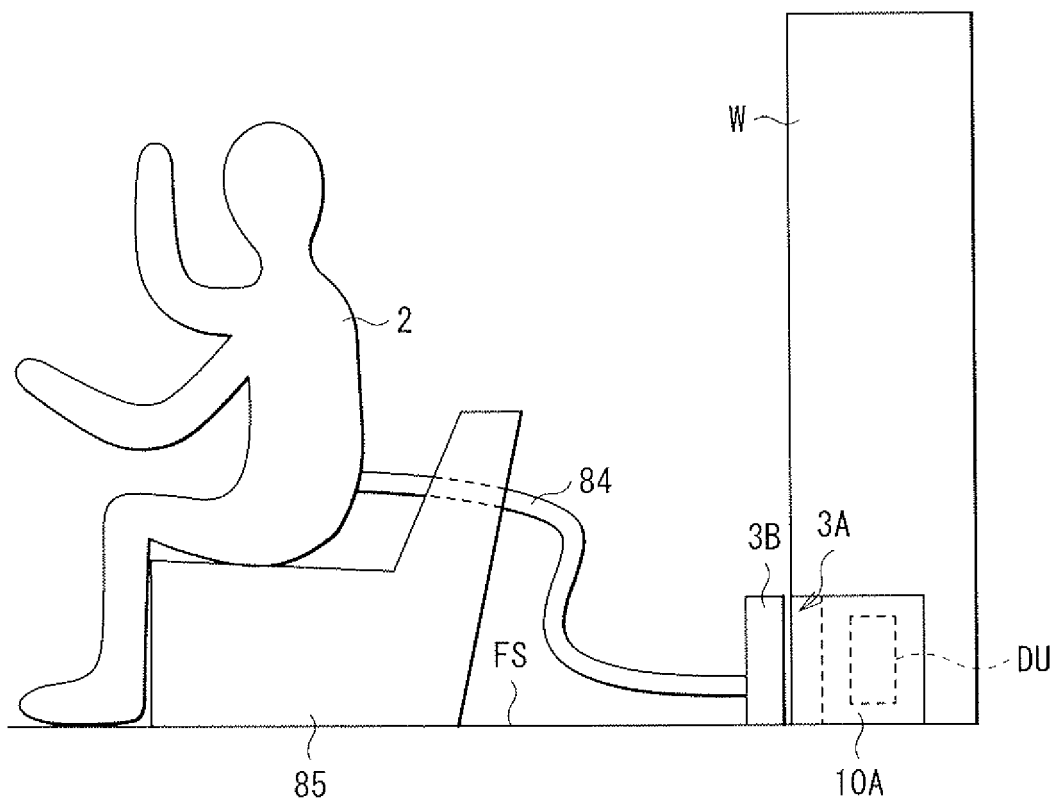
[図17]



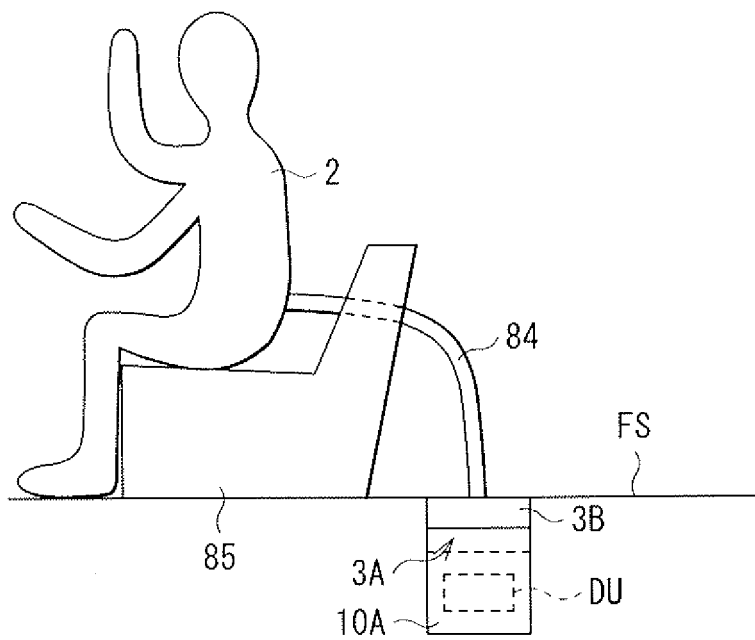
[図18A]



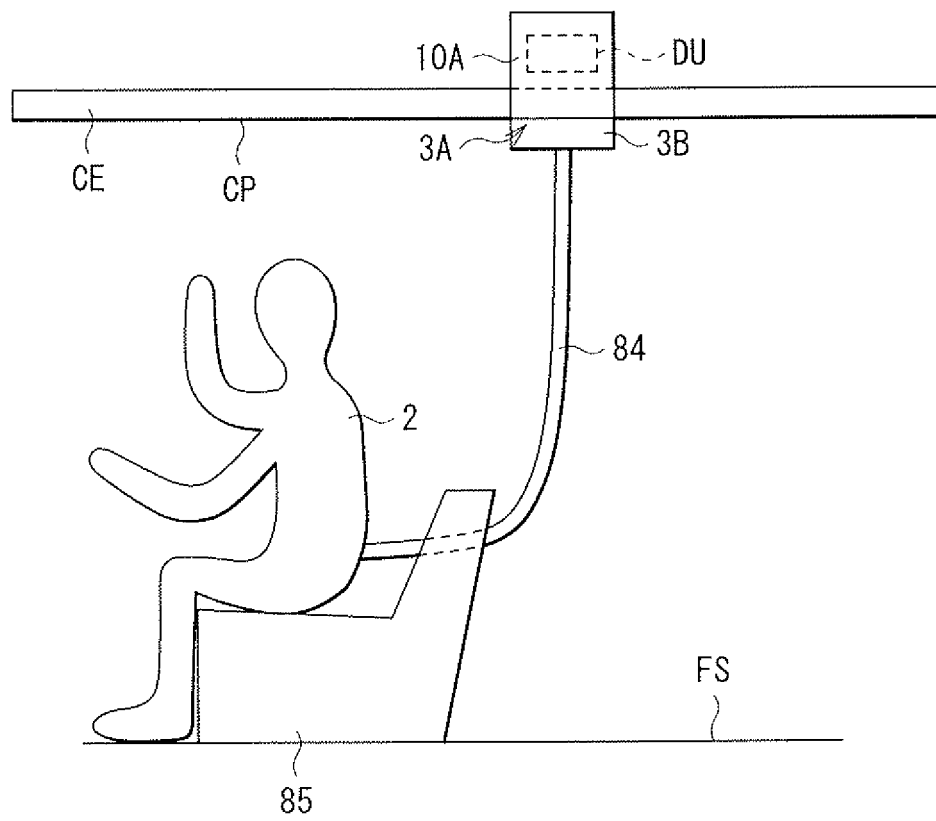
[図18B]



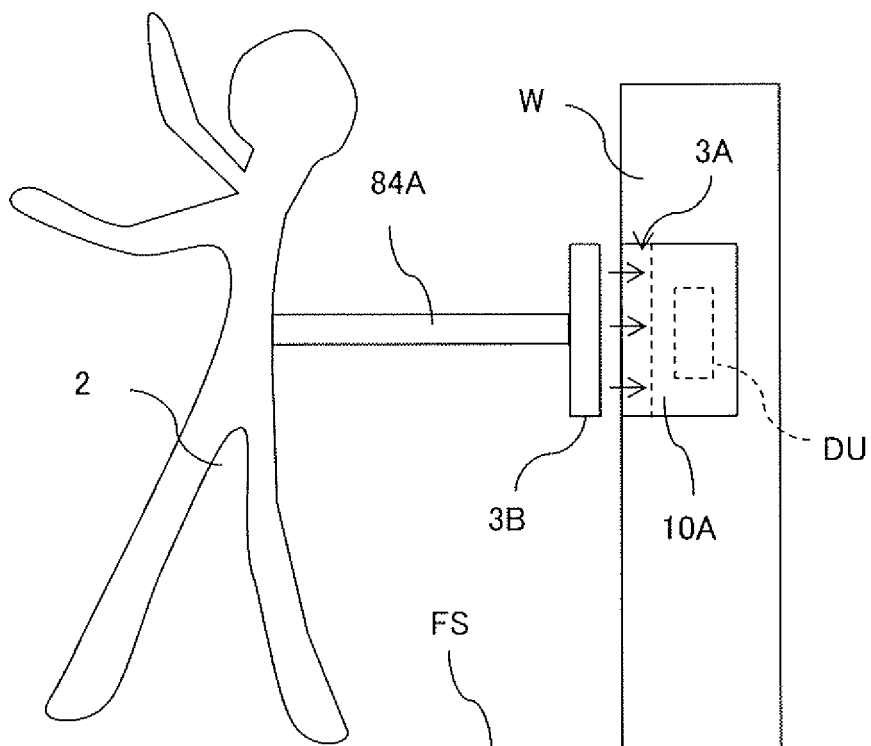
[図18C]



[図18D]



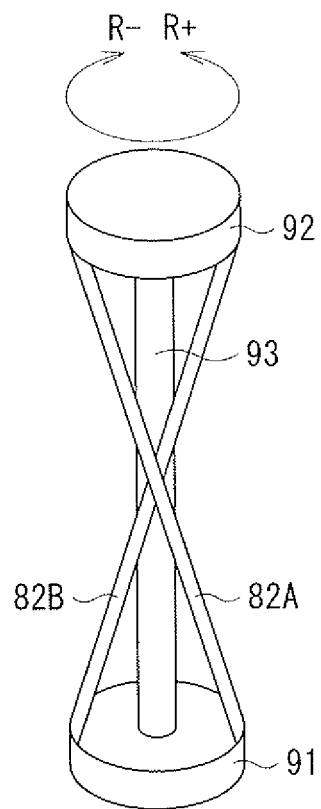
[図18E]



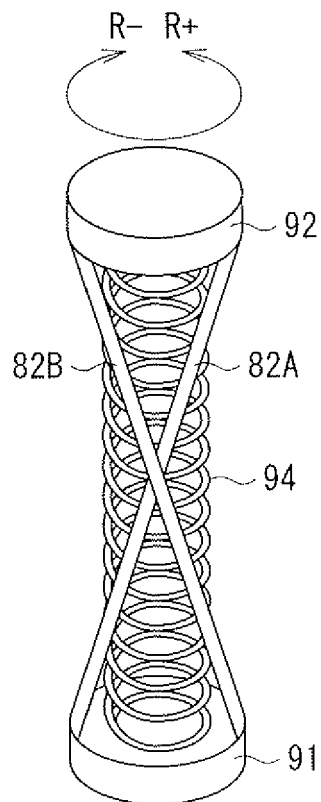




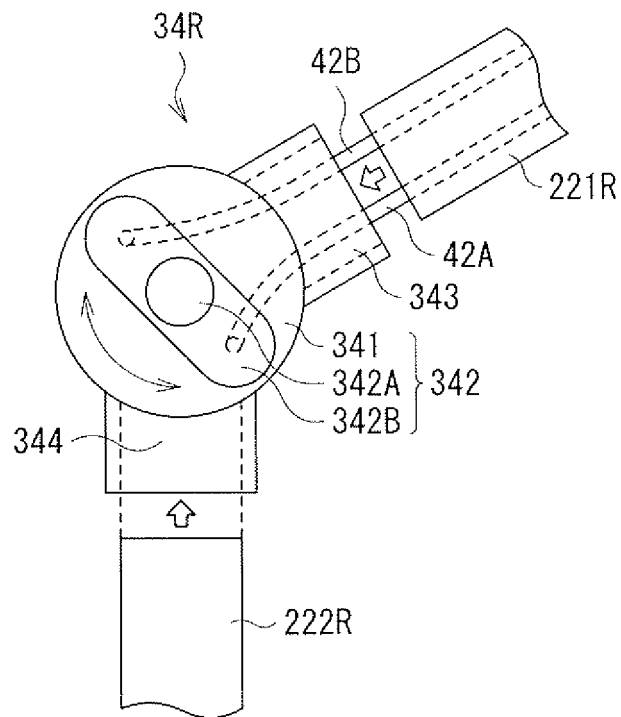
[図21A]



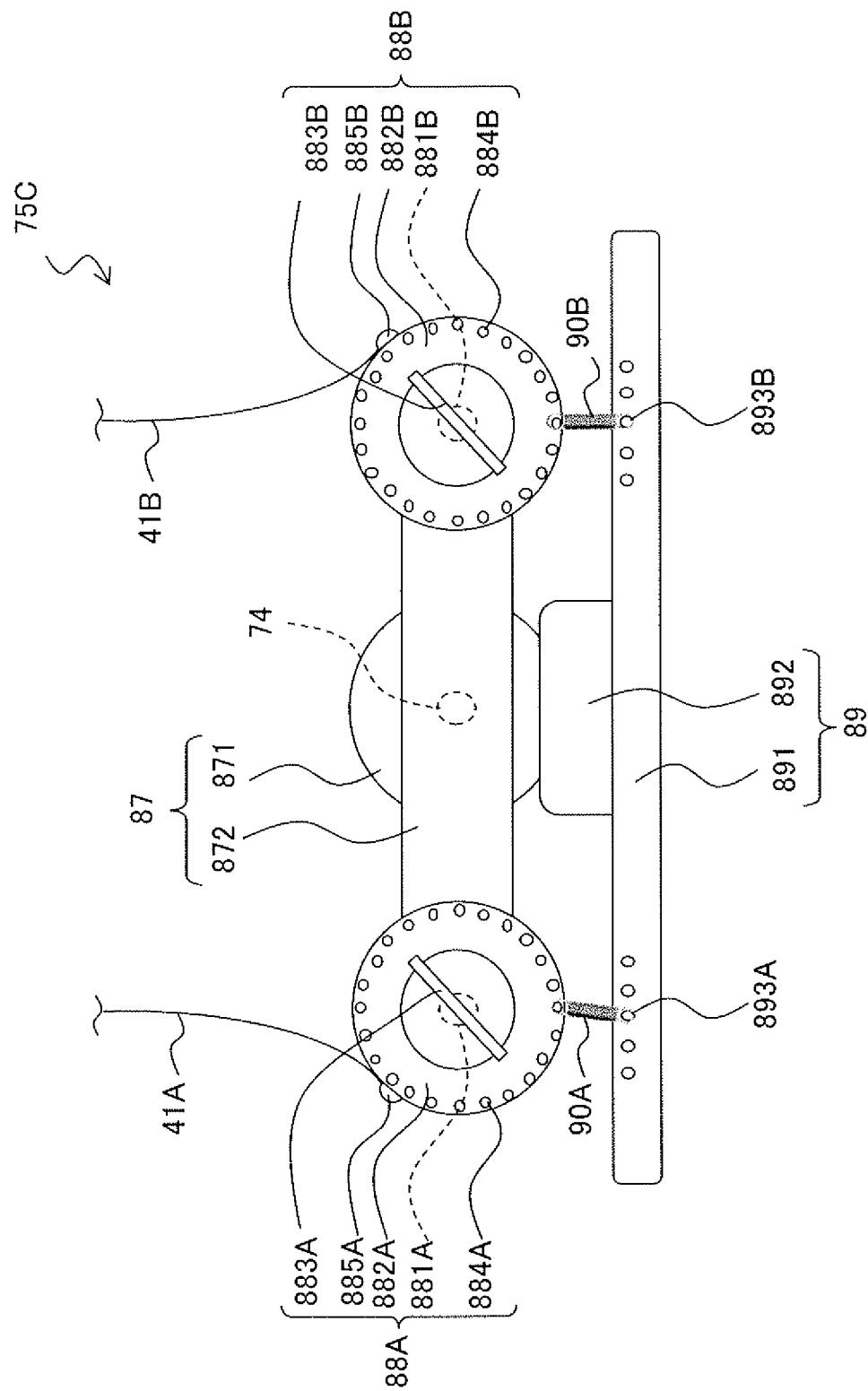
[図21B]



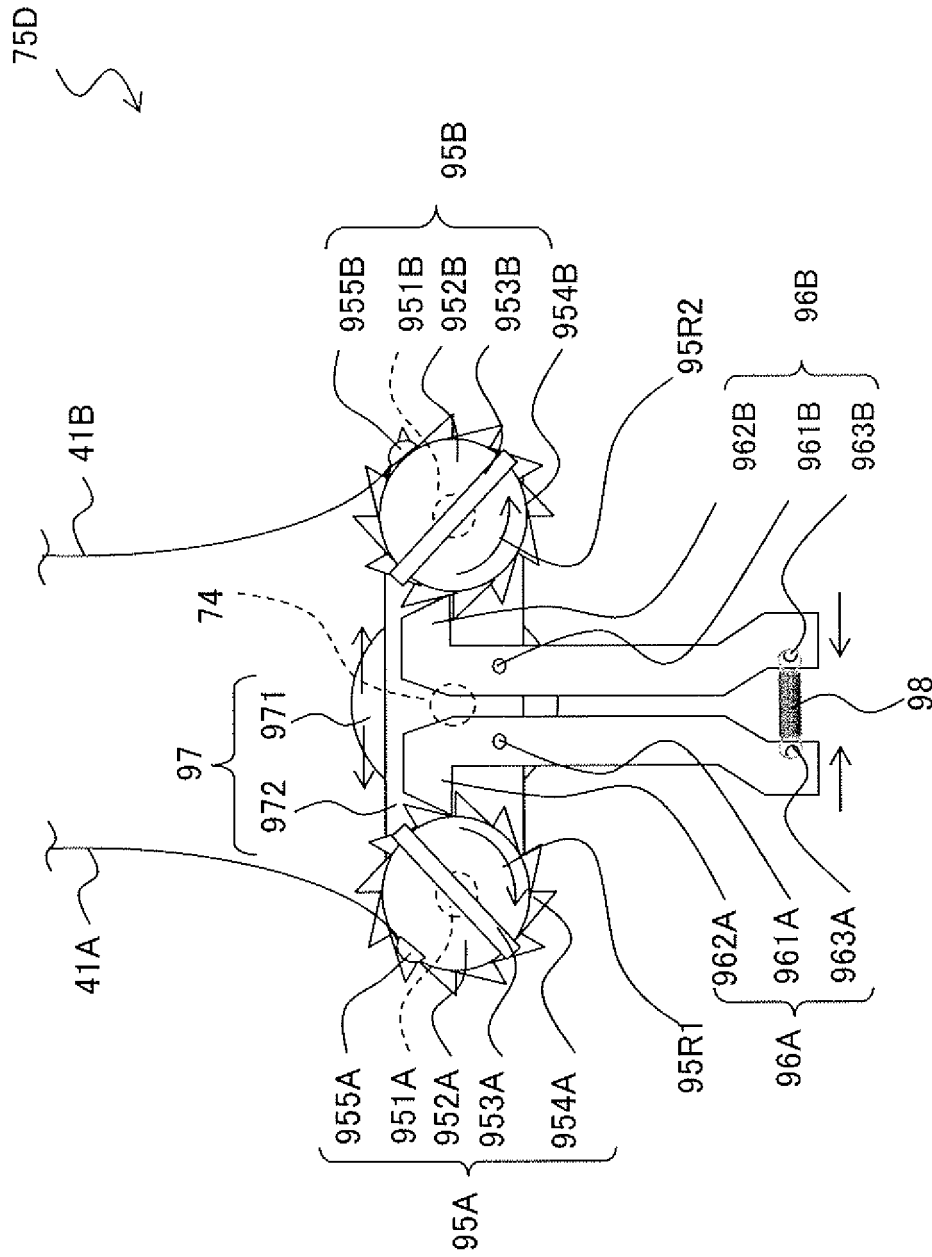
[図22]



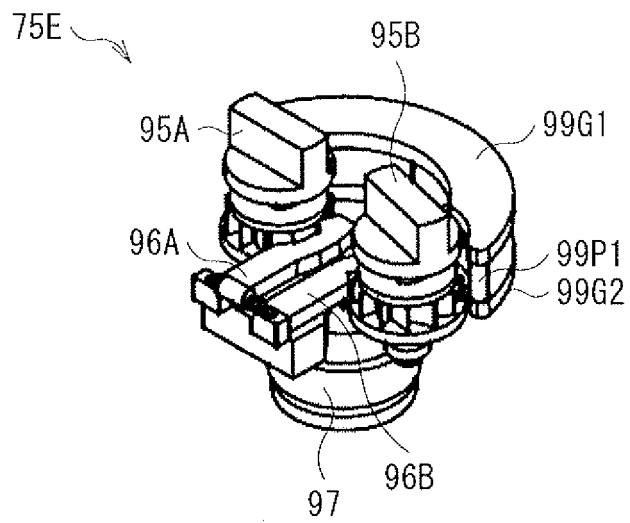
[図23]



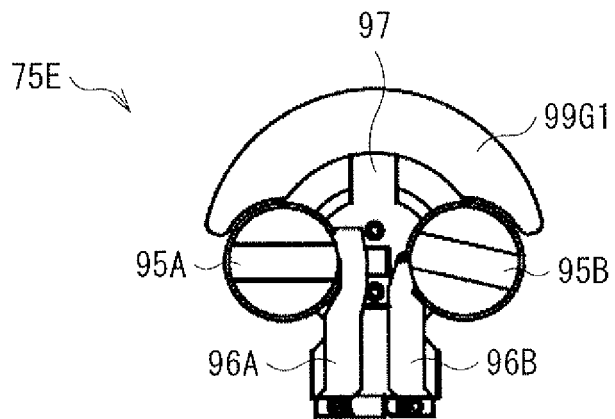
[図24]



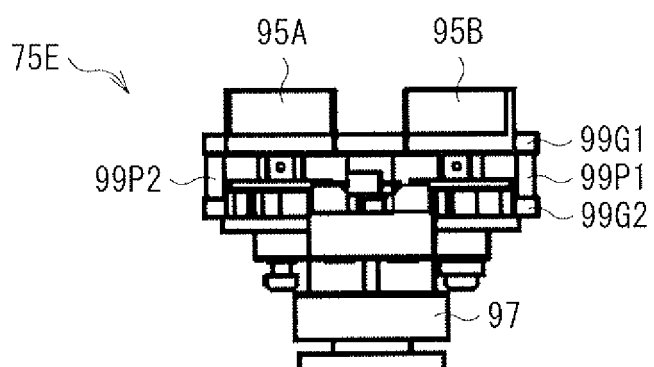
[図25A]



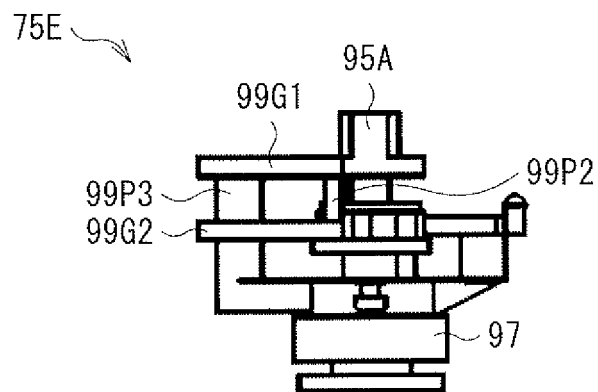
[図25B]



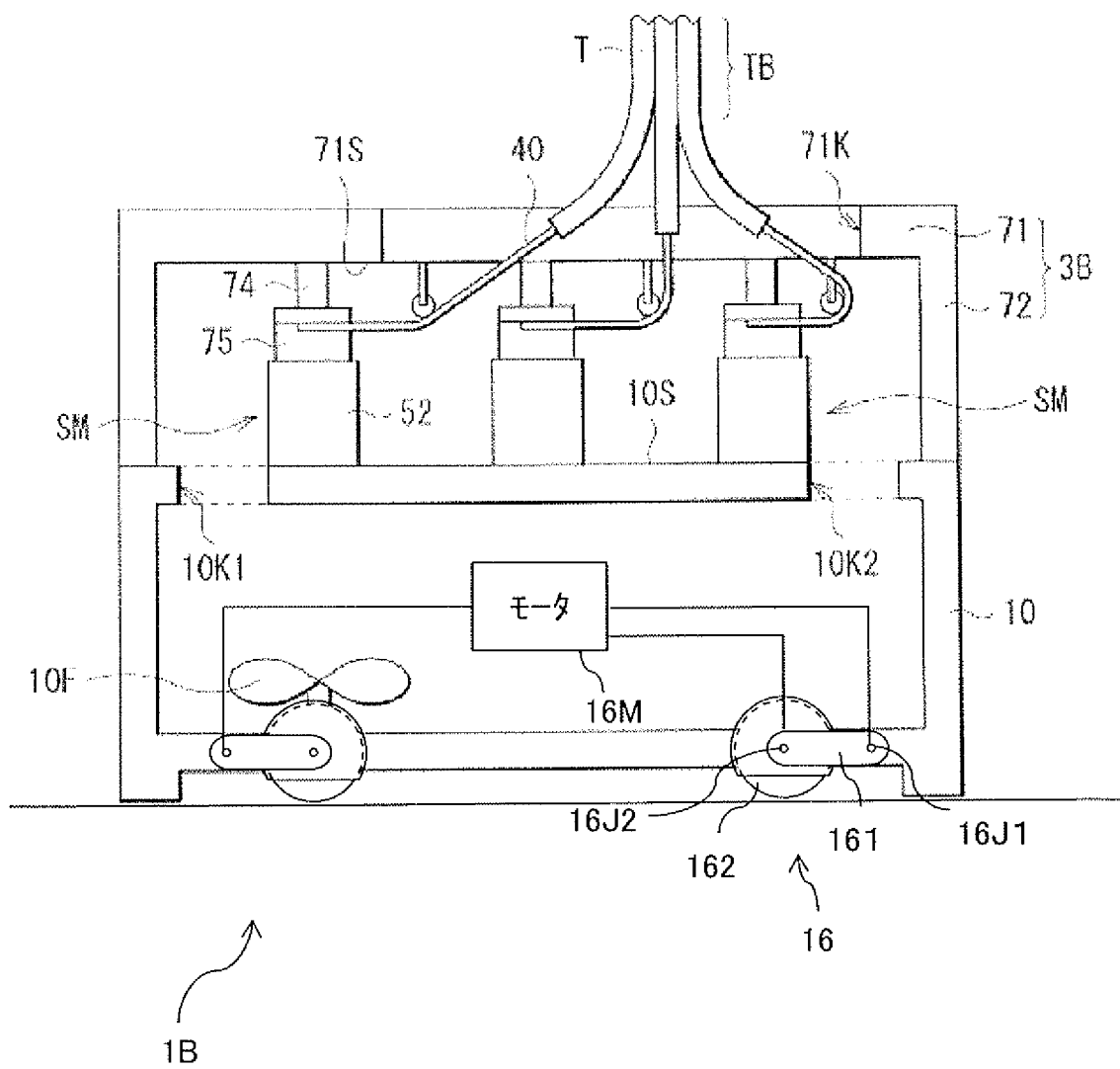
[図25C]



[図25D]

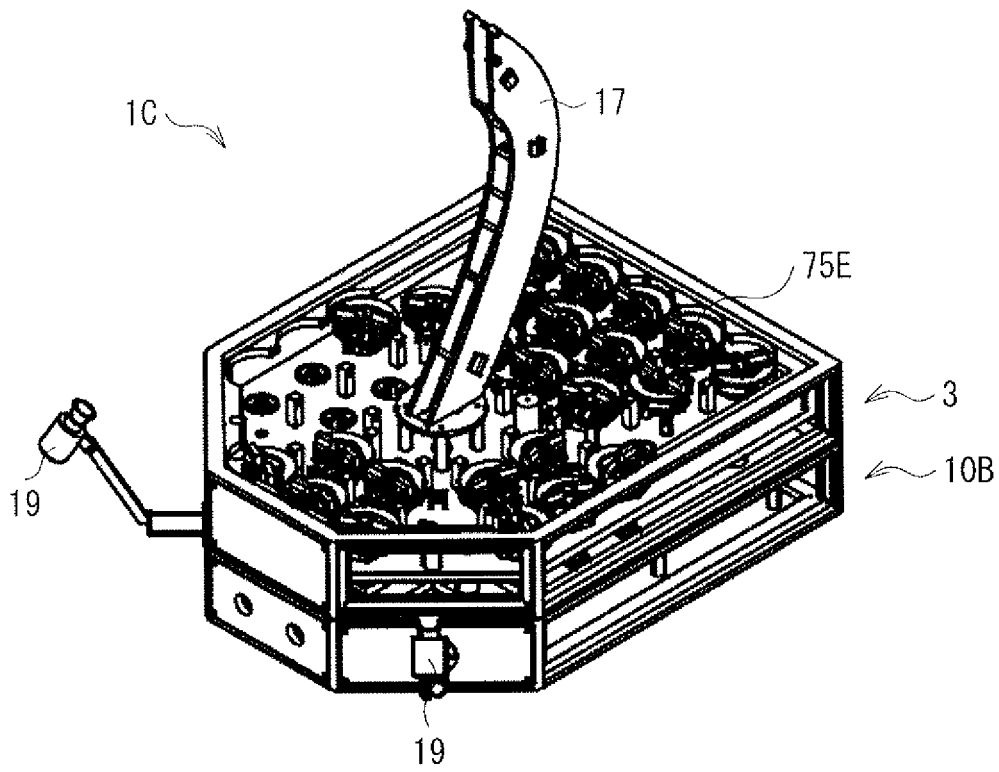


[図26A]

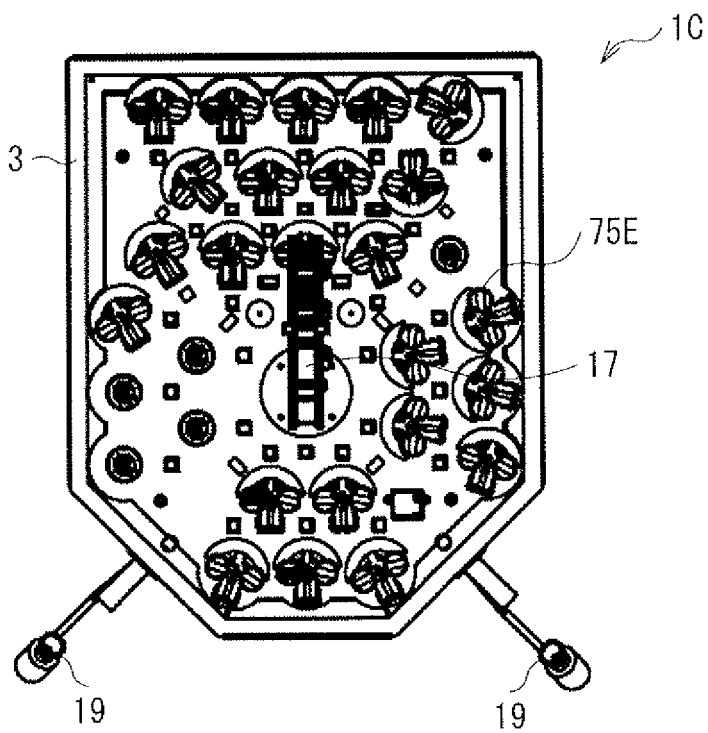




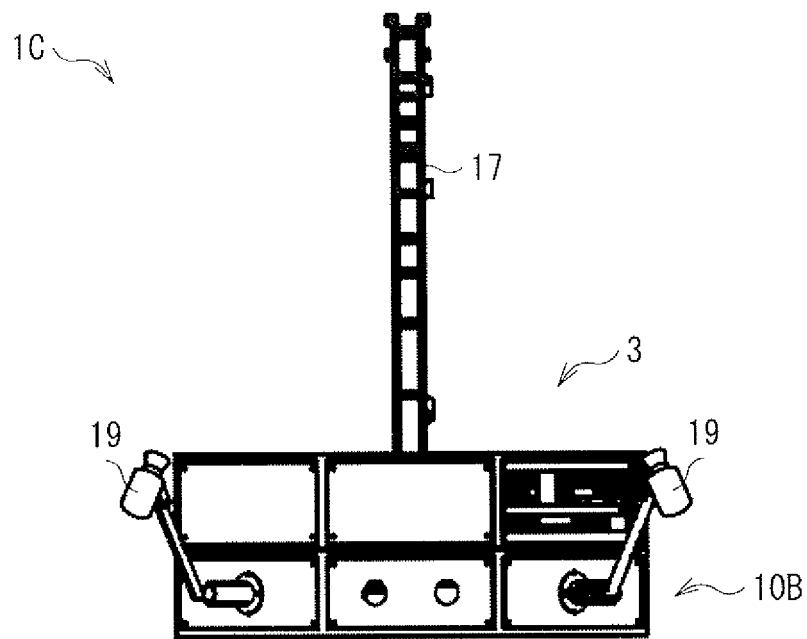
[図27A]



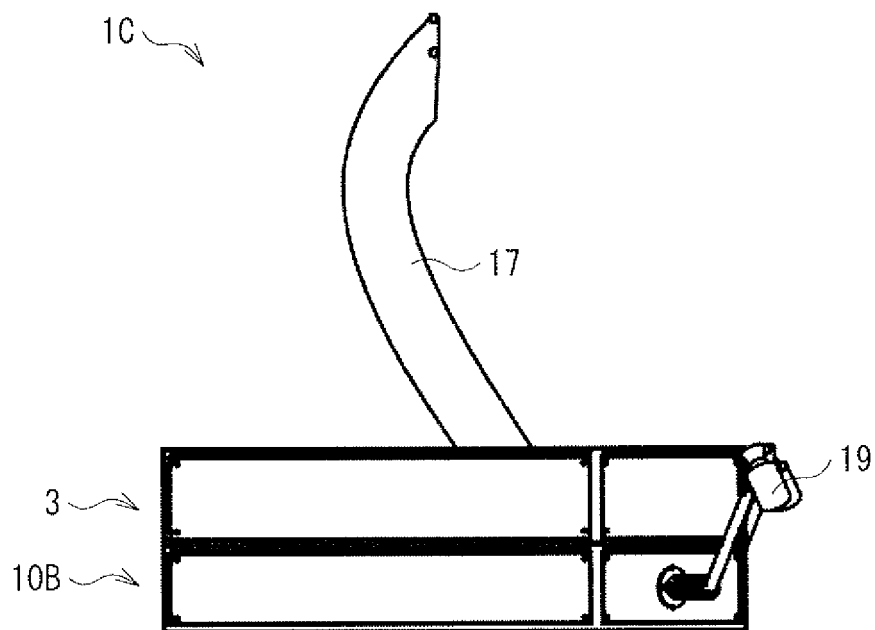
[図27B]



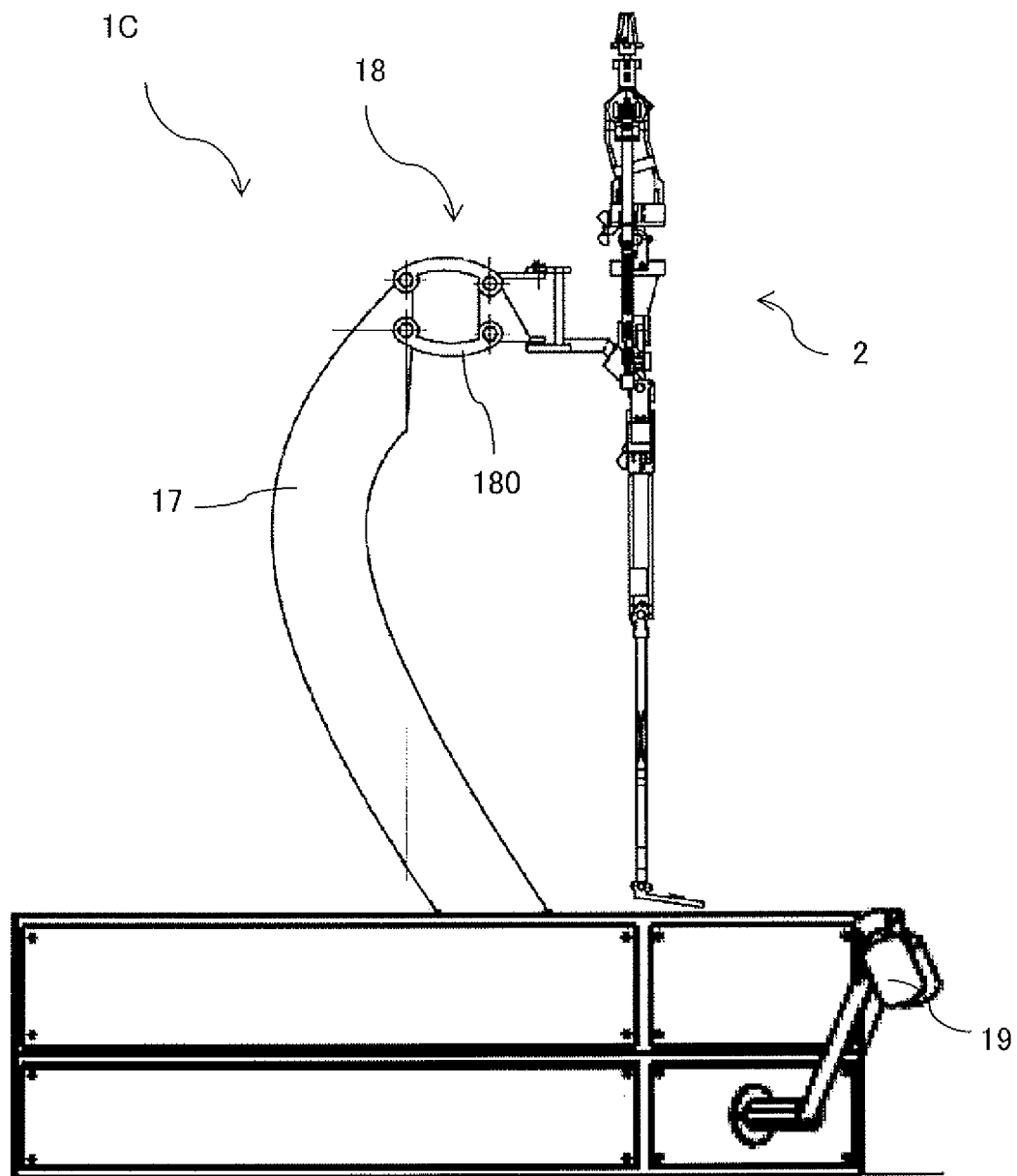
[図27C]



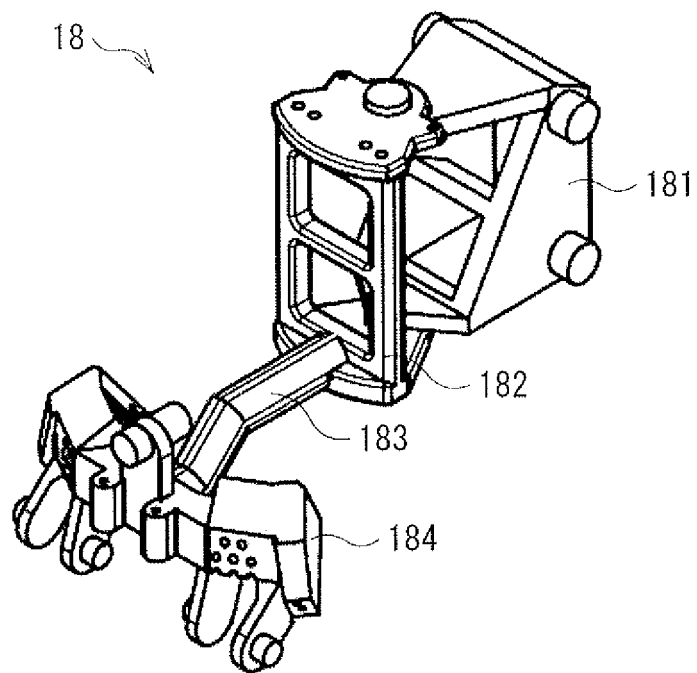
[図27D]



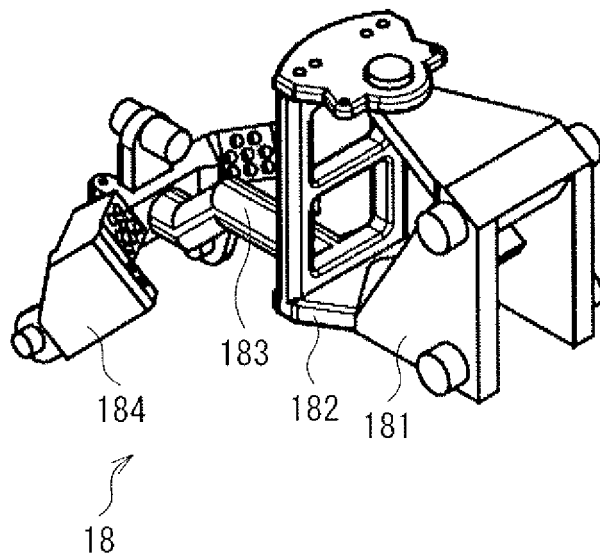
[図27E]



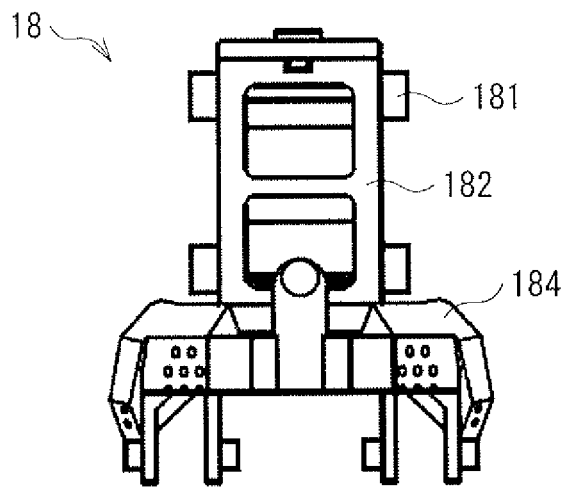
[図28A]



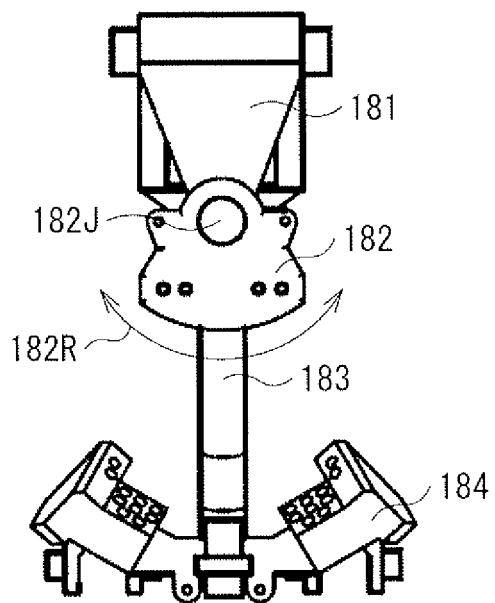
[図28B]



[図28C]



[図28D]



[図28E]

