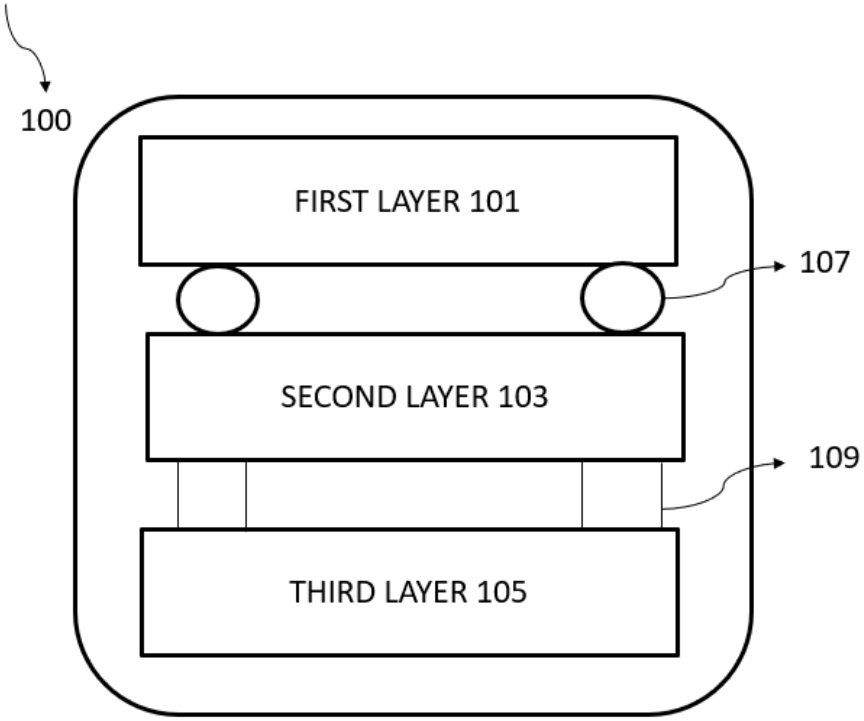


FIG. 1

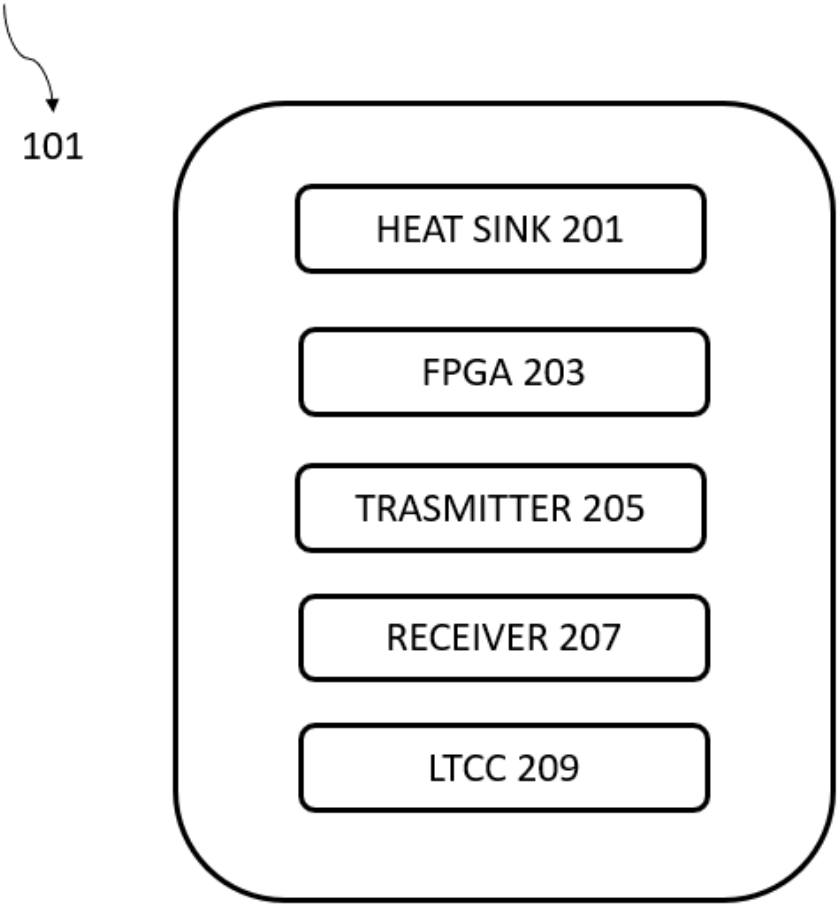

101
HEAT SINK 201
FPGA 203
TRASMITTER 205
RECEIVER 207
LTCC 209

FIG. 2

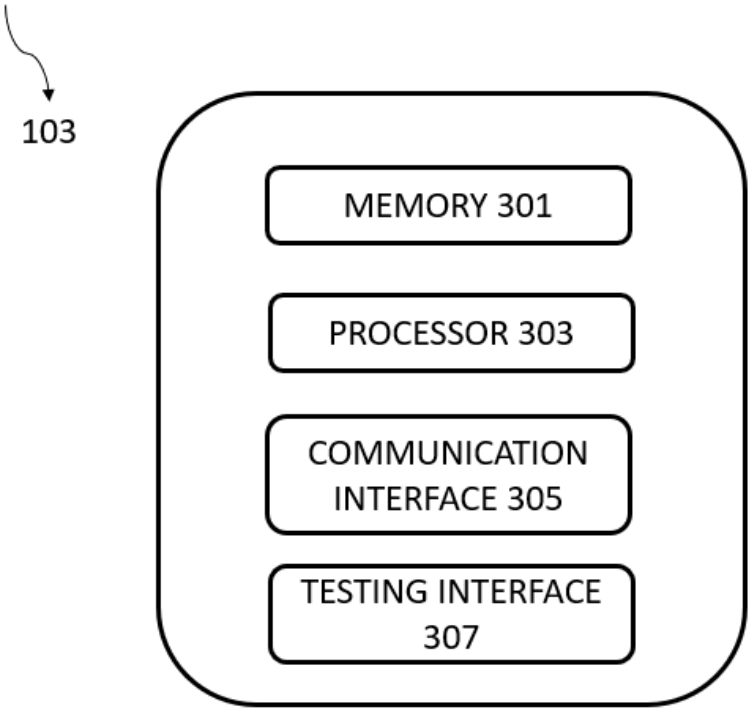

103
MEMORY 301
PROCESSOR 303
COMMUNICATION INTERFACE 305
TESTING INTERFACE 307

FIG. 3

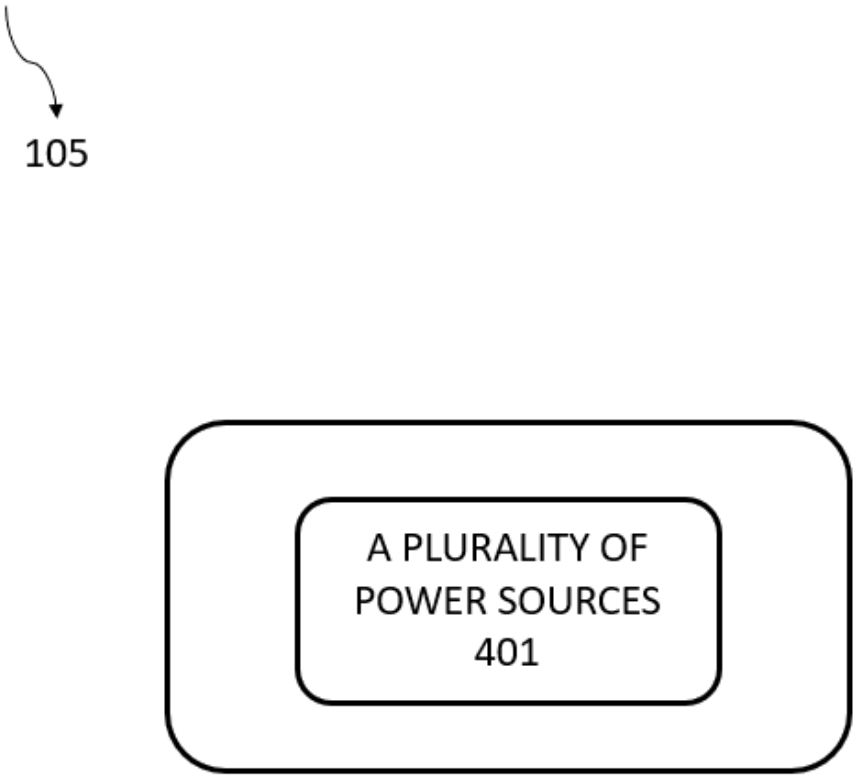


FIG. 4

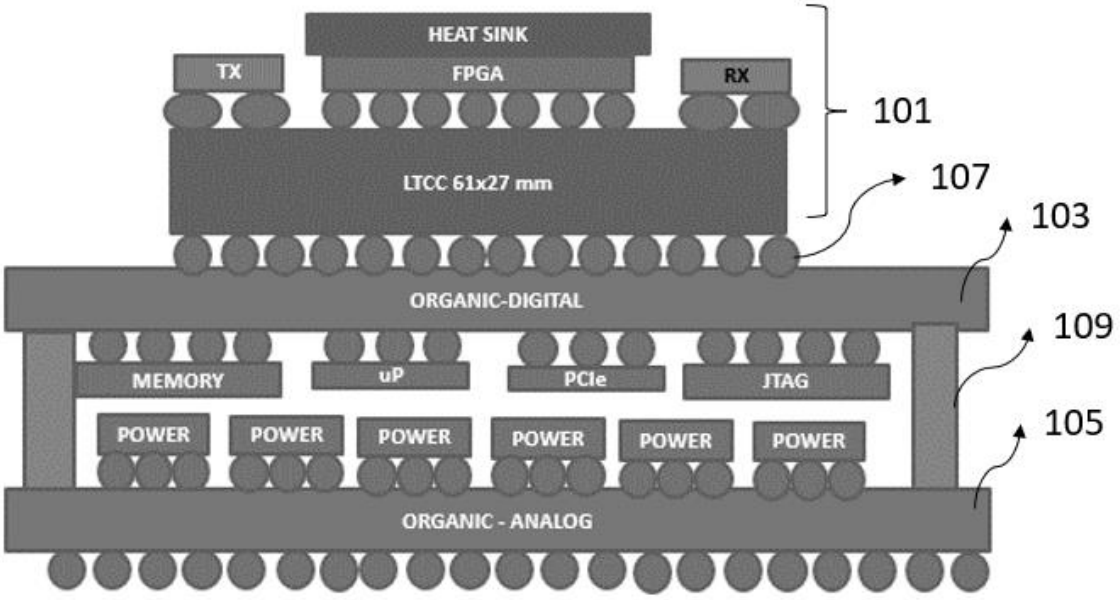

HEAT SINK
TX
FPGA
RX
101
LTCC 61x27 mm
107
103
ORGANIC-DIGITAL
109
MEMORY
uP
PCIe
JTAG
105
POWER
POWER
POWER
POWER
POWER
POWER
ORGANIC - ANALOG

FIG. 5

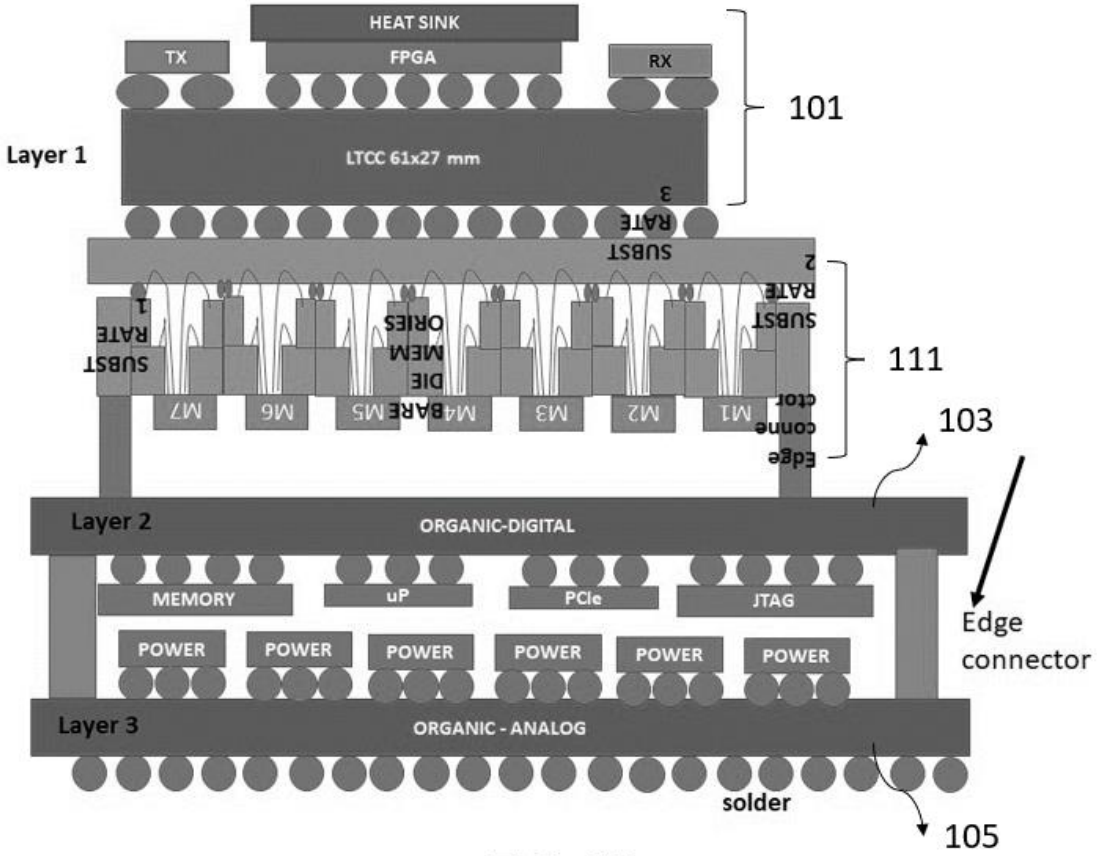

HEAT SINK
TX
FPGA
RX
101
Layer 1
LTCC 61x27 mm
111
103
Layer 2
ORGANIC-DIGITAL
MEMORY
uP
PCIe
JTAG
POWER
POWER
POWER
POWER
POWER
POWER
Edge
connector
Layer 3
ORGANIC - ANALOG
solder
105

FIG. 6A

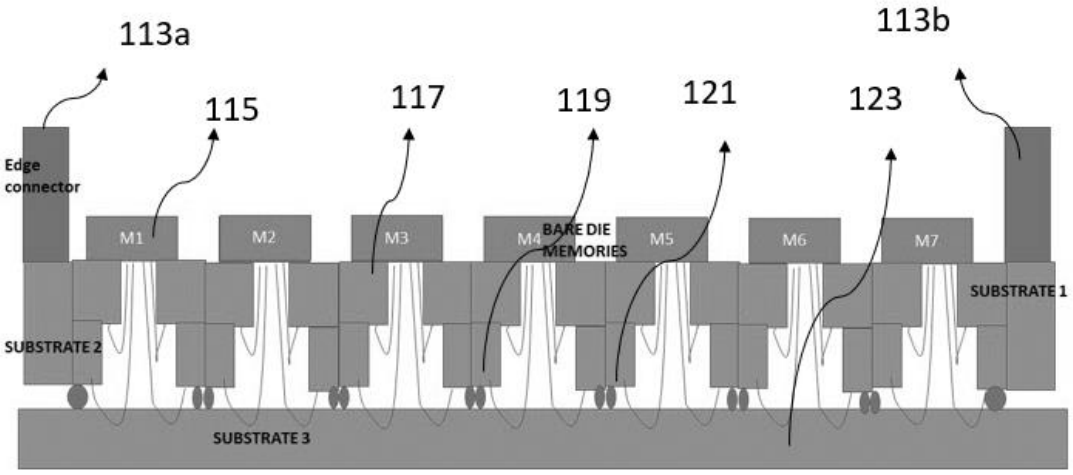

113a
113b
115
117
119
121
123
Edge connector
M1
M2
M3
M4
BARE DIE MEMORIES
M5
M6
M7
SUBSTRATE 1
SUBSTRATE 2
SUBSTRATE 3

FIG. 6B