

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
23 October 2003 (23.10.2003)

PCT

(10) International Publication Number
WO 03/088353 A1

(51) International Patent Classification⁷: H01L 21/8246,
27/105

(21) International Application Number: PCT/US03/04461

(22) International Filing Date: 14 February 2003 (14.02.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/118,732 8 April 2002 (08.04.2002) US

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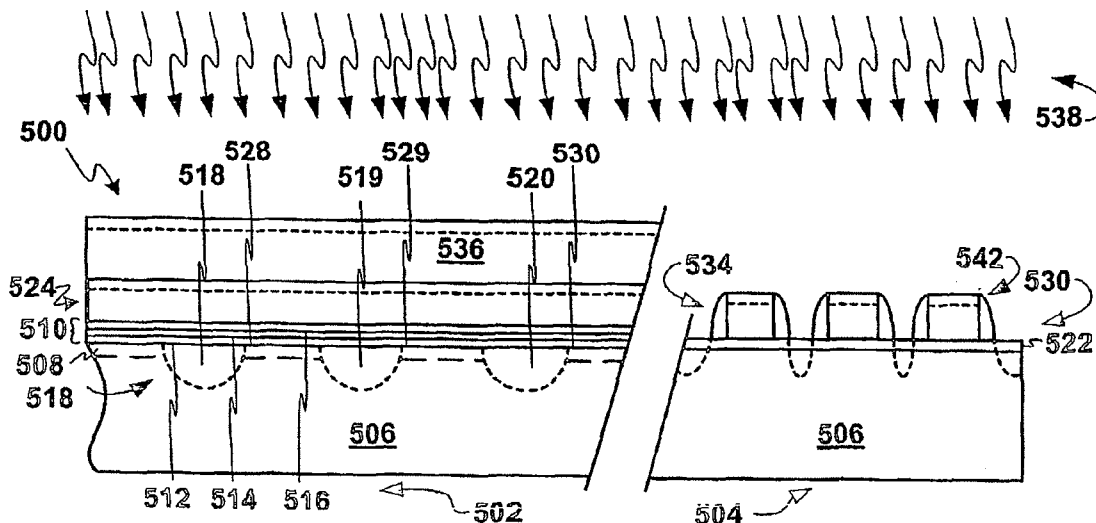
(81) Designated States (*national*): AE, AG, AL, AM, AT, AU,
AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU,
CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM,
HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK,
LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX,
MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SK, SL, TJ,
TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM,
KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW),
Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),
European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE,
ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, SE, SI,
SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN,
GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— with international search report

[Continued on next page]

(54) Title: MEMORY MANUFACTURING PROCESS WITH BITLINE ISOLATION



(57) Abstract: A method of manufacturing an integrated circuit is provided with a semiconductor substrate (506) having a core region (502) and a periphery region (504). A charge-trapping dielectric layer (510) is deposited in the core region (502), and a gate dielectric layer (522) is deposited in the periphery region (504). Bitlines (518) are formed in the semiconductor substrate (506) in the core region (502) and not in the periphery region (504). A wordline-gate layer (524) is formed and implanted with dopant in the core region (502) and not in the periphery region (504). A wordline (528) and gate (530) are formed. Source/drain junctions are implanted with dopant in the semiconductor substrate (506) around the gate (530), and the gate (530) is implanted with a gate doping implantation in the periphery region (504) and not in the core region (502).



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— before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

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