ABSTRACT

A NOVEL METHOD FOR FORMING DAMASCENE DUAL GATE FOR IMPROVED OXIDE UNIFORMITY AND CONTROL

A new method is provided to grow layers of gate oxide or other gate base materials of different thicknesses for dual gate structures. The process of the invention starts with a semiconductor surface in which Shallow Trench Isolation regions have been formed and over the surface of which a layer of gate base material has been grown. A layer of dielectric, such as nitride, is deposited over the layer of gate base material. The layer of dielectric is masked and etched over a first region where thin gate base material must be created thereby exposing the surface of the deposited layer of gate base material in that region. The layer of gate base material is etched to the desired thickness, creating a first thin layer of gate base material. A thick first layer of gate electrode material, such as poly, is deposited over the layer of dielectric thereby including the surface of the first thin layer of gate base material. The thick layer of gate electrode material is polished down to the surface of the layer of dielectric leaving gate electrode material deposited in the opening above the first thin layer of gate base material. The process that has been used to create a gate electrode having a first thickness of the layer of gate base material is repeated but this time over a second region of the gate base material thereby creating a gate electrode having a

second thickness of the layer of gate base material. The layer of dielectric is removed leaving gate electrode structures in place above thin layers of gate base materials, the latter being of different thicknesses.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)