METHOD OF FORMING DIFFERENT SILICIDE PORTIONS ON DIFFERENT SILICON-CONTAINING REGIONS IN A SEMICONDUCTOR DEVICE

TECHNICAL FIELD

Generally, the present invention relates to the field of fabrication of integrated circuits, and more, particularly, to semiconductor devices having metal-silicide portions on semiconductor regions to reduce the sheet resistance of the semiconductor regions, and a method of manufacturing these semiconductor devices.

BACKGROUND ART

In modern ultra-high density integrated circuits, device features are steadily decreasing to enhance device performance and functionality. Shrinking the feature sizes, however, entails certain problems that may partially offset the advantages obtained by the reduced feature sizes. Generally, reducing the feature sizes of, for example, a transistor element, leads to a decreased channel resistance in the transistor element and thus results in a higher drive current capability and enhanced switching speed of the transistor. In decreasing the feature sizes of these transistor elements, however, the increasing electrical resistance of conductive lines and contact regions, *i.e.*, of regions that provide electrical contact to the periphery of the transistor element, becomes a dominant issue since the cross-sectional area of these lines and regions decreases with decreasing feature sizes. The cross-sectional area, however, determines, in combination with the characteristics of the material comprising the conductive lines and contact regions, the resistance of the respective line or contact region.

The above problems may be exemplified for a typical critical feature size in this respect, also referred to as a critical dimension (CD), such as the extension of the channel of a field effect transistor that forms below a gate electrode between a source region and a drain region of the transistor. Reducing this extension of the channel, commonly referred to as channel length, may significantly improve device performance with respect to fall and rise times of the transistor element due to the smaller capacitance between the gate electrode and the channel and due to the decreased resistance of the shorter channel. Shrinking of the channel length, however, also entails the reduction in size of any conductive lines, such as the gate electrode of the field effect transistor, which is commonly formed of polysilicon, and the contact regions that allow electrical contact to the drain and source regions of the transistor, so that, consequently, the available cross-section for charge carrier transportation is reduced. As a result, the conductive lines and contact regions exhibit a higher resistance unless the reduced cross-section is compensated for by improving the electrical characteristics of the material forming the lines and contact regions, such as the gate electrode, and the drain and source contact regions.

It is thus of particular importance to improve the characteristics of conductive regions that are substantially comprised of semiconductor material such as silicon. For instance, in modern integrated circuits, the individual semiconductor devices, such as field effect transistors, capacitors, and the like, are primarily based on silicon, wherein the individual devices are connected by silicon lines and metal lines. While the resistivity of the metal lines may be improved by replacing the commonly used aluminum by, for example, copper, process engineers are confronted with a challenging task when an improvement in the electrical characteristics of silicon-containing semiconductor lines and semiconductor contact regions is required.

With reference to Figures 1a and 1b, an exemplary process for manufacturing an integrated circuit containing, for example, a plurality of MOS transistors, will now be described in order to illustrate the problems involved in improving the electrical characteristics of silicon-containing semiconductor regions in more detail.

In Figure 1a, a semiconductor structure 100 includes a substrate 101, for example, a silicon substrate, in which a first semiconductor element 110 and a second semiconductor element 130 are formed. The first semiconductor element 110 may, as depicted in Figure 1a, represent a field effect transistor of a first conductivity type, such as an n-channel transistor, and the second semiconductor element 130 may represent a field effect transistor of a second conductivity type, such as a p-channel transistor. The first semiconductor element 110 comprises shallow trench isolations (STI) 113 that are formed of an insulated material, such as silicon dioxide, and that define an active region 112 in the substrate 101. A gate electrode 115 is formed over a gate insulation layer 118 that separates the gate electrode 115 from the active region 112. Spacer elements 116 made of, for example, silicon dioxide or silicon nitride, are located at the sidewalls of the gate electrode 115. In the active region 112, source and drain regions 114 are formed and exhibit an appropriate dopant profile required to connect to a conductive channel that builds up between the drain and the source region during operation of the first semiconductor element 110.

The second semiconductor element 130 comprises substantially the same parts as the first semiconductor element 110 and corresponding parts are denoted by the same reference numerals except for a "leading 13" instead of a "leading 11." As previously noted, the second semiconductor element 130 may differ from the first semiconductor element 110 in, for example, type of conductivity, that is, type and concentration of dopants provided in the active regions 112 and 132, lateral extension of the gate electrode, also referred to as gate length, cross-sectional area, and the like. Moreover, it should be noted that although the first and second semiconductor elements 110 and 130 in Figures 1a and 1b are depicted as transistor elements, the first and second semiconductor elements 110 and 130 may represent any silicon-containing region that is used for charge carrier transportation. For example, relatively long polysilicon lines may connect semiconductor elements on different locations of a single chip area and these polysilicon lines may be regarded as first and second semiconductor elements 110, 130, the electrical characteristics of which are to be improved so as to obtain an enhanced device performance with respect to signal propagation delay.

Again referring to Figure 1a, in particular the gate length of the first and second semiconductor elements 110 and 130 determines the channel length of these devices and, therefore, as previously pointed out, significantly affects the electrical characteristics of the first and second semiconductor elements 110 and 130, whereby a reduced gate length will result in an increased resistance of the gate electrodes 115, 135 owing to the reduction of the cross-sectional area of the gate electrodes 115, 135.

A typical process flow for forming the semiconductor structure 100 may comprise the following steps. After the formation of the shallow trench isolations 113 and 133 by well-known photolithography techniques, implantation steps are performed to create a required dopant concentration in the active regions 112 and 132. Subsequently, the gate insulation layers 118 and 138 are formed according to design requirements. Thereafter, the gate electrodes 115 and 135 are formed by patterning, for instance a polysilicon layer, by means of sophisticated photolithography and trim etch methods. Then, a further implantation step for forming so-called source and drain extensions within the source and drain regions 114 and 134 is performed and the spacer elements 116 and 126 are formed by deposition and anisotropic etching techniques. The spacer elements 116 and 126 are used as an implantation mask for a subsequent implantation step in which dopant particles are implanted into the source and drain regions 114 and 134 to create the required high dopant concentrations in these regions. It is to be noted that the dopant concentration varies in Figure 1a in the horizontal direction, *i.e.*, in the length direction of the gate electrodes 115, 135, as well as in the vertical direction, which will hereinafter be referred to

as depth direction. Although the dopant profile of the source and drain regions 114 and 134 is depicted as a region having a sharp boundary, in reality the dopant profile varies continuously due to the nature of the implantation process and the subsequent annealing steps that are performed for activating the implanted atoms and for curing the crystalline damage caused by the implantation step. Usually, the dopant profile has to be selected in conformity with other parameters of the first and second semiconductor elements 110 and 130. For example, a short gate length, and thus a short channel length, requires a "shallow" dopant profile in order to avoid the so-called "short channel effect." Accordingly, the peak concentration in the depth direction may be located a few hundred nanometers below the surface of the drain and source regions 114 and 134. Moreover, p-channel transistors may require a different dopant profile than an n-channel transistor element.

As previously noted, the cross-section of the gate electrodes 115 and 135, which may be considered as polysilicon lines, as well as the contact area on top of the source and drain regions 114 and 134, significantly influence the electrical characteristics of the first and second semiconductor elements 110 and 130. Since, generally, these device areas primarily contain a semiconductor material such as silicon in crystalline, polycrystalline and amorphous form, these areas, although they usually include dopants, exhibit a relatively high resistance compared to, for example, a metal line. Consequently, these areas are treated to enhance the conductivity of these regions, thereby improving the overall performance of the devices.

To this end, according to Figure 1a, a metal layer 140 is deposited over the first and second semiconductor elements 110 and 130. Typically, the metal layer 140 comprises titanium, cobalt or other refractory metals. Subsequently, a first heat treatment, for example, a rapid thermal annealing, is carried out to initiate a chemical reaction between the silicon in the source and drain regions 114, 134, the gate electrodes 115, 135 and the metal contained in the metal layer 140. If, for example, the metal layer 140 substantially comprises cobalt, an average temperature of the first heat treatment may be set to about 400°C to create a meta-stable cobalt silicon compound exhibiting a relatively high resistivity. Since the silicon contained in the spacer elements 116, 136 and the shallow trench isolations 113, 133 is chemically bound in the form of dioxide or nitride, the metal of the metal layer 140 does not substantially react with the material of the spacer element 115, 136 and the shallow trench isolations 113, 133. After the first heat treatment, the material of the metal layer 140 that has not reacted with the underlying material is removed by, for example, a selective wet etching process. Thereafter, a second heat treatment is performed, for example, a second rapid annealing step with a temperature higher than in the first annealing step, to convert the meta-stable metal-silicon compound into a metal silicide. In the above example, when cobalt is used, a cobalt disilicide is formed in the second annealing step. The metal silicide shows a significantly lower resistance than the meta-stable metal-silicon compound, as well as a significantly lower resistance, by a factor of about 5-10, than the sheet resistance of the doped polysilicon.

Figure 1b schematically shows the finally obtained first and second semiconductor elements 110 and 130 having formed on the respective source and drain regions 114, 134 and the gate electrodes 115, 135 a metal silicide region 141. Although the metal silicide regions 141 significantly improve the electrical characteristics of the first and second semiconductor elements 110 and 130, there is still room for improvement since, in the conventional process flow, the metal silicide regions 141 have to be formed so as to meet the requirements of the first semiconductor element 110 and the second semiconductor element 130, so that optimizing the characteristics of the silicide regions 141 of the first semiconductor element 110 compromises the effect of the silicide regions 141 of the second semiconductor element 130, and vice versa.

It is thus desirable to have a semiconductor and a method of forming the same in which the characteristics of the conductive semiconductor regions may be individually optimized for different semiconductor elements.

DISCLOSURE OF INVENTION

The present invention is generally directed to a semiconductor device and a method for manufacturing the semiconductor device in which silicon-containing regions receive a metal silicide portion to enhance the electric properties of these regions, wherein the type of material and/or a thickness of the metal silicide portions are individually adjusted in different regions to obtain the electrical conductivity that is required at these different semiconductor regions to further optimize the performance of the semiconductor device.

According to one illustrative embodiment, a method of fabricating a semiconductor device comprises providing a substrate having formed thereon a first silicon-containing region and a second silicon-containing region. The method further comprises selectively forming a first metal layer on the first silicon-containing region and selectively forming a second metal layer on the second silicon-containing region. Moreover, a heat treatment is performed on the substrate to transform, at least partially, the first metal layer in a first metal silicide and the second metal layer in a second metal silicide, wherein the first and the second metal silicide differ from each other in their composition and/or their layer thickness.

According to a further illustrative embodiment, a method of fabricating a semiconductor device comprises forming a first metal layer on a first silicon-containing region and a second silicon-containing region provided on a substrate. Moreover, the first metal layer is selectively removed from the second silicon-containing region and a resist mask is formed to cover the first silicon-containing region and to expose the second silicon-containing region. Additionally, the method includes depositing a second metal layer and removing the resist mask. Moreover, a chemical reaction is initiated between the first and second metal layers and the silicon contained in the first and second region.

According to yet a further embodiment of the present invention, a method for forming a semiconductor device comprises providing a substrate having formed therein a first and a second silicon-containing region, the first and second silicon-containing regions differing from each other in at least one of crystalline structure, dimension, dopant concentration and dopant profile. Moreover, the method includes depositing a first metal layer on the first and second silicon-containing regions and forming a resist mask to expose the first silicon-containing region and to cover the second silicon-containing region. Moreover, the first metal layer is removed from the first silicon-containing region and subsequently a second metal layer is deposited over the substrate. Furthermore, the method includes removing the resist mask and heat treating the substrate to obtain a first silicide portion and a second silicide portion in the first and second silicon-containing regions, respectively, wherein a type of material in the first and the second metal layers and process parameters of the heat treatment are selected to adjust a depth of the first and second silicide portions.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements, and in which:

Figures 1a and 1b schematically show cross-sectional views of a conventionally manufactured semiconductor device; and

Figures 2a to 2f schematically show cross-sectional views of a semiconductor device during various manufacturing stages in accordance with one embodiment of the present invention.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

MODE(S) FOR CARRYING OUT THE INVENTION

Illustrative embodiments of the invention are described below. In the interest of clarity, not all features of an actual implementation are described in this specification. It will of course be appreciated that in the development of any such actual embodiment, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking for those of ordinary skill in the art having the benefit of this disclosure.

With reference to Figures 2a-2f, illustrative embodiments of the present invention will now be described, wherein, as previously pointed out, two or more different conductive silicon-containing regions receive a silicide portion, the type of material and/or the thickness of which are correspondingly designed to improve the electrical conductivity of these regions. For example, if it is necessary to obtain a similar signal propagation delay for long silicon lines connecting two different die areas, wherein one of the silicon lines exhibits a larger cross-sectional area than the other one, according to the present invention, different silicide portions are formed on these silicon lines to improve the overall characteristics and to substantially compensate for the different cross-sectional areas. The same applies to different types of transistor elements, such as n-channel transistors and p-channel transistors, that, in general, have a different dopant profile and also a different barrier height that experiences a charge carrier at the interface between the silicide portion and the doped silicon-containing region. In this case, the present invention also allows one to appropriately form corresponding silicide portions in the devices to individually optimize the performance of the devices. Similarly, short channel devices generally require a different type of silicide portion than do long channel devices since, for example, in long channel devices, the peak dopant concentration is located more deeply in the drain and source regions than in short channel devices, which require relatively shallow junctions. The present invention allows one to individually adjust the overlap of the silicided portion at a depth at which the peak dopant concentration is located so as to obtain a minimum transition resistance for charge carriers, especially when the barrier height of the metal silicide is selected in conformity with the type of dopants prevailing in the active regions of the transistor devices. Consequently, although in the following detailed description a first and second semiconductor element representing a complementary transistor pair is referred to, the present invention is to cover all aspects in which silicon-containing regions are required to receive individually adapted silicide portions to improve the performance of the individual semiconductor region or to improve the overall performance of the semiconductor device.

In Figure 2a, a semiconductor structure 200 comprises a substrate 201, for example, a silicon substrate, or any other substrate appropriate for the formation of semiconductor elements. In the substrate 201, a first semiconductor element 210 comprises an active region 212 defined by shallow trench isolations 213. A gate electrode 215 is separated from the active region 212 by a gate insulation layer 218. Spacer elements 216 of an insulating material, such as silicon dioxide or silicon nitrite, are formed adjacent to the sidewalls of the gate electrode 215. In the active region 212, source and drain regions 214 are formed.

The semiconductor structure 200 further includes a second semiconductor element 230 comprising substantially the same components as the first semiconductor element 210. Thus, corresponding parts are denoted by the same reference numbers except for a leading "23" instead of a leading "21." It should be borne in mind, however, that although depicted as being quite similar, the first and the second semiconductor elements 210 and 230 differ from each other in the sense as pointed out above. That is, the first and second semiconductor elements 210 and 230 may represent different types of field effect transistors differing, for example, in type of channel conductivity, channel length, position in the substrate 201 and the like. Moreover, the first and second semiconductor elements 210 and 230 may represent a silicon line, such as a polysilicon line connecting different regions in the substrate 201, or may represent a plurality of silicon lines, which differ in type of dopants, dopant concentration, dimensions, *i.e.*, in length or cross-section, crystalline structure, *i.e.*, polycrystalline, crystalline, amorphous and the like.

A first metal layer 240 is deposited on the first and second semiconductor elements 210 and 230. The first metal layer 240 comprises a type of material and is deposited with a thickness such that silicide portions to be formed in the first semiconductor element 210 may substantially exhibit the required electrical characteristics. For example, in one embodiment, the first metal layer may comprise at least one of cobalt, titanium, zirconium, tungsten, nickel, or any other refractory metal that reacts with silicon to form a metal silicide having a relatively low electrical resistance. In another embodiment, the first metal layer may include one or more noble metals such as platinum, palladium or gold and the like. In other embodiments, the first metal layer 240 may be provided as a compound of different metals or may be provided as a bi-layer or as a multi-layer.

A typical process flow for forming the semiconductor structure 200 may be quite similar to the processes as described with reference to Figures 1a and 1b and thus the description of these process steps is omitted.

Figure 2b schematically shows the semiconductor structure 200 with a resist mask 250 provided on the second semiconductor element 230. The resist mask 250 may be formed by means of standard photolithography techniques, wherein any overlay considerations, *i.e.*, the accuracy of positioning the resist mask 250 on the second semiconductor element 230, are of no great concern since the precise location of the resist mask 250 on the shallow trench isolation 233 is not critical.

Figure 2c schematically shows the semiconductor structure 200 after the first metal layer 240 is removed from the first semiconductor element 210. The removal of the first metal layer 240 at the first semiconductor element 210 may be accomplished by a selective wet chemical etch process.

Figure 2d schematically shows the semiconductor structure 200, wherein a second metal layer 242 is deposited over the semiconductor structure 200. The second metal layer 242 may comprise a single metal or, in other embodiments, the second metal layer 242 may comprise two or more metals, such as cobalt, titanium, zirconium, tungsten, nickel, platinum, palladium, gold and any combination thereof, wherein the type of materials contained in the second metal layer 242, the composition of these materials, *i.e.*, whether the materials are provided as a plurality of distinct layers or as compounds, and the thickness may differ from the corresponding characteristics of the first metal layer 240, so that a silicide portion to be formed in the first semiconductor element 210 will substantially exhibit electrical characteristics as required by design rules.

Depositing the second metal layer 242 may be carried out such that sidewall portions 252 of the resist mask 250 remain substantially uncovered by the material of the second metal layer 242. That is, a deposition technique may be employed that allows a minimal step coverage. For instance, a physical vapor deposition

(PVD) technique, such as sputter deposition, may be used, wherein process parameters are adjusted in such a manner that metal particles sputtered off of a target hit the semiconductor structure 200 substantially perpendicularly. Consequently, the deposition rate of material of the second metal layer 242 at the sidewall portions 252 is minimal. Adjusting the trajectories of the metal particles directed to the surface of the semiconductor structure 200 such that the metal particles substantially perpendicularly enter the substrate surface may be obtained by using a collimator in the vicinity of the substrate 201. Alternatively, or additionally, the required directionality of the incoming metal particles may also be obtained by adjusting the magnetic and electrical fields during the deposition of the second metal layer 242 such that a minimal step coverage is achieved.

Figure 2e schematically shows the semiconductor structure 200 with the resist mask 250, and, consequently, the second metal layer 242 formed on top of the resist mask 250, removed from the second semiconductor element 230. Thus, the semiconductor structure 200 comprises the second metal layer 242 on the first semiconductor element 210 and the first metal layer 240 on the second semiconductor element 230, wherein, as previously noted, the first and second metal layers 240 and 242 differ from each other in type of material and/or layer thickness so as to yield the required characteristics for the corresponding silicide portions to be formed in the first and second semiconductor elements 210 and 230.

Removing the resist mask 250 and the second metal layer 242 deposited thereon may be achieved by a selective wet etching process using a chemical agent having a significantly higher etching rate for the resist mask 250 than for the second metal layer 242. Depending on the degree of coverage of the sidewall portions 252 with metal of the second metal layer 242, the predefined thickness of the initially deposited second metal layer 242 may be correspondingly selected so that in the subsequent etching process the thickness of the second metal layer 242 over the first semiconductor element 210 will not decrease below a required minimum thickness. In removing the resist mask 250, the sidewall portions 252 are "under-etched" so that, consequently, the mechanical integrity of the second metal layer 242 on top of the resist mask 250 is broken, and the individual parts that split off the second metal layer 242 will be purged away during the etching process. Even if the sidewall portions 252 are covered by the second metal layer 242, the resist mask 250 may nevertheless be reliably removed, although at a prolonged etch time compared to a substantially metal-free sidewall portion 252, since the metal layer thickness at the sidewall portions 252 is considerably smaller than the thickness of the second metal layer 242 at substantially horizontal surface portions of the substrate 201. In one illustrative embodiment, the layer thickness of the second metal layer 242 at the sidewall portions 252 will not exceed about 10% of the layer thickness at horizontal surface portions. In this respect, it is to be noted that a degraded step coverage at other parts of the first semiconductor element 210, for example at the spacer elements 216, is of no concern since in this region no silicide portions will be formed at all.

Figure 2f schematically shows the semiconductor structure 200 with first silicide portions 241 formed in the second semiconductor element 230 and second silicide portions 243 formed in the first semiconductor element 210. Although not depicted in Figure 2f, the first and second silicide portions 241 and 243 differ from each other in their depth or thickness, *i.e.*, the penetration depth into the regions 214, 215 and 234, 235, respectively and/or in type of material/composition. Thus, the first silicide portions 241 are designed to improve the electrical conductivity within the regions 234 and 235 and are adapted to provide for a substantial overlap with the peak concentration of dopants provided in the regions 234, 235, and/or to yield a minimum barrier height between the silicide portion 241 and the regions 234, 235. The same applies to the second silicide portions 243.

That is, the first and second silicide portions 241, 243 are designed to yield a sheet resistance for each of the first and second semiconductor elements 210, 230 that may be within a corresponding predefined range.

The first and second silicide 241, 243 may be obtained by the following process steps. According to one embodiment, a heat treatment is performed, for example a rapid thermal annealing step, to initiate a chemical reaction between the metal in the first and the second metal layers 240, 242 and the silicon contained in the regions 214, 234 and 215, 235. After the first rapid thermal annealing step, with a first temperature for a first time interval, and a subsequent removal of excess metal from the surface of the semiconductor structure 200 by means of a selective etching process, a second rapid thermal annealing step may be performed for a second time interval with a second temperature that is generally higher than the first temperature to obtain a stable metal silicide having a relatively low electrical resistance. In removing the excess metal of the first and second metal layers 240, 242 between the first and second rapid thermal annealing steps, the etch agent does not need to be selective with respect to the first and second metal layers 240, 242 so that the excess metal may be removed in a common etching process.

During the first rapid thermal annealing step, diffusion of the atoms of the regions 214, 234, 215, 235 and of the atoms of the first and second metal layers 240, 242 takes place so that a continuous reaction between the silicon and the metal is maintained. The degree of diffusion, and thus the amount of metal-silicon compound formed during the reaction, depends on the type of material, the temperature and the duration of the annealing process. Generally, metals having a higher melting temperature tend to show a lower diffusion activity. Thus, the thickness of the metal-silicon compound may be partially adjusted by controlling the first average temperature and the first time interval. In the second rapid thermal annealing step, with the second temperature, a reaction takes place in which the metal-silicon compound is converted into a low-ohmic phase. Typically, the second average temperature is higher than the first temperature to obtain the stable metal silicide having a relatively low electrical resistance. The second average temperature and the second time interval may also be controlled to obtain the required sheet resistance in each of the regions 214, 215, 234, 235.

It is to be noted that although the first and second metal layers 240, 242 differ from each other, the sheet resistance in the first and second semiconductor elements 210 and 230 may nevertheless be individually adjusted in a single common heat treatment, for example, the two-step annealing described above, since the reaction characteristics of the materials comprising the first and second metal layers 240, 242 are well known and may be selected to yield the desired sheet resistance.

The particular embodiments disclosed above are illustrative only, as the invention may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. For example, the process steps set forth above may be performed in a different order. Furthermore, no limitations are intended to the details of construction or design herein shown, other than as described in the claims below. It is therefore evident that the particular embodiments disclosed above may be altered or modified and all such variations are considered within the scope and spirit of the invention. Accordingly, the protection sought herein is as set forth in the claims below.

CLAIMS

1. A method of fabricating a semiconductor device, comprising:

providing a substrate 201 having formed thereon a first silicon-containing region and a second silicon-containing region;

selectively forming a first metal layer 250 on the first silicon-containing region;

selectively forming a second metal layer 242 on the second silicon-containing region; and

heat treating the substrate 201 to transform, at least partially, the first metal layer 240 into a first metal silicide 241 and the second metal layer 242 into a second metal silicide 243, wherein the first and second metal silicide portions 241, 243 differ from each other in at least one of composition and thickness.

2. The method of claim 1, wherein selectively forming the first metal layer includes:

depositing the first metal layer 240 over the first and second silicon-containing regions;

forming a resist mask 250 on the first silicon containing region; and

removing the first metal layer 240 from the second silicon-containing region.

3. The method of claim 2, wherein selectively forming the second metal layer on the second silicon-containing region includes:

depositing the second metal layer 242 on the second silicon-containing region and the resist mask 250; and

removing the resist mask 250.

4. The method of claim 3, wherein depositing the second metal layer 242 includes controlling the metal deposition such that a step coverage of the resist mask 250 is minimal.

5. The method of claim 4, wherein the step coverage is reduced by employing a vapor deposition technique in which metal particles hit the substrate 201 substantially perpendicularly.

6. The method of claim 4, wherein a directionality of metal particles hitting the substrate 201 during deposition of the second metal layer 242 is controlled by at least one of using a collimator and controlling the magnetic and electrical fields used during deposition of the second metal layer 242.

7. The method of claim 1, wherein at least one of type of metal and layer thickness of the first 240 and the second 242 metal layers, temperature and duration of the heat treatment are selected to attain a first and a second sheet resistance in the first 241 and second 243 silicide portions such that the first and second sheet resistances are within corresponding predefined ranges.

8. The method of claim 1, wherein at least one of the first 240 and second 242 metal layers comprises at least one of cobalt, titanium, tantalum, zirconium, nickel, tungsten, a noble metal and any combination thereof.

9. The method of claim 1, wherein the first silicon-containing region includes at least one n-channel field effect transistor 210 and the second silicon-containing region includes at least one p-channel field effect transistor 230.

10. A method of fabricating a semiconductor device, comprising:

forming a first metal layer 240 on a first silicon-containing region and a second silicon-containing region provided on a substrate 201;

forming a resist mask 250 to cover the first silicon-containing region and to expose the second silicon-containing region;

removing the first metal layer 240 from the second silicon-containing region;

depositing a second metal layer 240 over the second silicon-containing region and the resist mask 250;

removing the resist mask 250; and

initiating a chemical reaction between the first 240 and second 242 metal layers and the silicon contained in the first and second regions to form first 241 and second 243 silicide portions in the first and second silicon-containing regions, respectively.

11. The method of claim 10, wherein depositing the second metal layer 242 includes controlling the metal deposition such that a step coverage of the resist mask 250 is minimal.

12. The method of claim 11, wherein the step coverage is reduced by employing a vapor deposition technique in which metal particles hit the substrate 201 substantially perpendicularly.

13. The method of claim 10, wherein a directionality of metal particles hitting the substrate 201 during deposition of the second metal layer 242 is controlled by at least one of using a collimator and controlling the magnetic and electrical fields used during deposition of the second metal layer 242.

14. A method of forming a semiconductor device, the method comprising

providing a substrate 201 having formed therein a first and a second silicon-containing region, the first and second silicon-containing regions differing from each other in at least one of crystalline structure, dimension, dopant concentration and dopant profile;

depositing a first metal layer 240 on the first and second silicon-containing regions;

forming a resist mask 250 to expose the first silicon-containing region and to cover the second silicon-containing region;

removing the first metal layer 240 from the first silicon-containing region;

depositing a second metal layer 242 over the first silicon-containing region and the resist mask 250 ;

removing the resist mask 250; and

heat treating the substrate 201 to obtain a first silicide portion 241 and a second silicide portion 243 in the first and second silicon-containing regions, respectively, wherein a type of material in the first and the second metal layers 240, 242 and process parameters of the heat treatment are selected to adjust a depth of the first and second silicide portions.