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ABSTRACT

A METHOD TO FORM AN ASYMMETRICAL NON-VOLATILE MEMORY DEVICE USING SMALL IN-SITU DOPED POLYSILICON SPACERS

A new method of forming a sharp tip on a floating gate in the fabrication of a EEPROM memory cell is described. A first gate dielectric layer is provided on a substrate. A second gate dielectric layer is deposited overlying the first gate dielectric layer. A floating gate/control gate stack is formed overlying the second gate dielectric layer. One sidewall portion of the floating gate is covered with a mask. The second gate dielectric layer not covered by the mask is etched away whereby an undercut of the floating gate is formed in the second gate dielectric layer. The mask is removed. Polysilicon spacers are formed on sidewalls of the floating gate wherein one of the polysilicon spacers fills the undercut thereby forming a sharp polysilicon tip to improve the erase efficiency of the memory cell.

FIGURE 7