What is claimed is:

1. An integrated circuit system comprising:

a substrate including a source/drain region defined by a spacer;

a gate over the substrate;

a gate dielectric between the gate and the substrate;

a recrystallized region within the gate and the source/drain region; and

a channel exhibiting the characteristics of stress memorization.

2. The system as claimed in claim 1 wherein:

the substrate includes a bulk semiconductor substrate or a silicon-on-insulator substrate.

3. The system as claimed in claim 1 wherein:

the channel includes a compressively stressed channel.

4. The system as claimed in claim 1 wherein:

the channel includes a tensile stressed channel.

5. The system as claimed in claim 1 further comprising:

a low resistance contact formed over the gate and the source/drain region.

6. The system as claimed in claim 1 wherein:

the channel includes an NFET channel formed within a CMOS device.

7. The system as claimed in claim 1 wherein:

the recrystallized region within the gate and the source/drain region induces stress within the channel.

8. The system as claimed in claim 1 wherein:

the substrate includes a shallow recess.

9. The system as claimed in claim 1 wherein:

the channel exhibits the characteristics of stress memorization due to a close proximity stress memorization layer.

10. The system as claimed in claim 1 further comprising:

a source/drain extension and a halo implant in the substrate.

What is claimed is:

1. An integrated circuit system comprising:

a substrate;

a gate dielectric directly on the substrate;

a gate directly on the gate dielectric;

a source/drain region in the substrate defining a channel, the source/drain region having a boundary characteristic of a spacer;

a stress region characteristic of a stress transferred from a stress memorization layer to the gate and the source/drain region; and

a contact spacer adjacent the gate, the contact spacer completely on the stress region characteristic of the stress memorization layer removed.

2. The system as claimed in claim 1 wherein:

the substrate includes a bulk semiconductor substrate or a silicon-on-insulator substrate.

3. The system as claimed in claim 1 wherein:

the channel includes a compressively stressed channel.

4. The system as claimed in claim 1 wherein:

the channel includes a tensile stressed channel.

5. The system as claimed in claim 1 further comprising:

a low resistance contact formed over the gate and the source/drain region.

6. The system as claimed in claim 1 wherein:

the channel includes an NFET channel formed within a CMOS device.

7. The system as claimed in claim 1 wherein:

the stress region within the gate and the source/drain region induces stress within the channel.

8. The system as claimed in claim 1 wherein:

the substrate includes a shallow recess.

9. The system as claimed in claim 1 wherein:

the channel exhibits the characteristics of stress memorization due to a close proximity stress memorization layer.

10. The system as claimed in claim 1 further comprising:
a source/drain extension and a halo implant in the substrate.