We claim :

1. A method of increasing a speed of access of computer memory, the method comprising:

detecting a first memory access, from a first process executing in a virtual machine computing environment, directed to a first range of memory;

generating, as a precondition to completing the first memory access, a first entry in a hierarchically arranged second layer address translation table, the hierarchically arranged second layer address translation table correlating host physical memory addresses to guest physical memory addresses, the first entry being at least one hierarchical level above a hierarchically lowest level of tables such that a second range of memory, identified by the first entry, can be identified without reference to any table in the hierarchically lowest level of tables, the second range of memory being greater than the first range of memory; and

in response to generating the first entry in the hierarchically arranged second layer address translation table, marking as used a first plurality of entries in a hierarchically arranged page table, the hierarchically arranged page table correlating the host physical memory addresses to host virtual memory addresses, the first plurality of entries referencing, in aggregate, the same second range of memory as the first entry in the hierarchically arranged second layer address translation table, wherein entries of the first plurality of entries are at a hierarchically lowest level of tables;

wherein the guest physical memory addresses are perceived as being addresses to physical memory by processes executing within the virtual machine computing environment;

wherein the host physical memory addresses are addresses to actual physical memory of a host computing device hosting the virtual machine computing environment;

wherein the host virtual memory addresses are addresses to virtual memory provided by a memory manager executing on the host computing device, the memory manager utilizing the hierarchically arranged page table to provide the virtual memory; and

wherein guest physical memory, identified by the guest physical memory addresses, is backed by a portion of host virtual memory, identified by a portion of the host virtual memory addresses.

2. The method of claim 1, further comprising :

detecting a second memory access from the first process executing in the virtual machine computing environment, the second memory access being directed to a third range of memory that differs from the first range of memory; and

satisfying the second memory access by reference to a second subset of the first plurality of entries in the hierarchically arranged page table;

wherein the first memory access was satisfied by reference to a first subset of the first plurality of entries in the hierarchically arranged page table, the first subset comprising different entries, in the hierarchically arranged page table, than the second subset.

3. The method of claim 1, further comprising:

detecting, after the first memory access completes, that a first subset of the first plurality of entries in the hierarchically arranged page table have had data, that was originally stored in corresponding host physical memory addresses, subsequently paged out to a non-volatile storage medium;

invalidating, in response to the detecting, the first entry in the hierarchically arranged second layer address translation table; and

generating, in place of the first entry in the hierarchically arranged second layer address translation table, a second plurality of entries in the hierarchically arranged second layer address translation table, the second plurality of entries referencing, in aggregate, at least some of the same second range of memory as the first entry, wherein entries of the second plurality of entries are at a hierarchically lowest level of tables.

4. The method of claim 3, wherein the second plurality of entries references portions of the second range of memory that were previously accessed by the first process and were not paged out.

5. The method of claim 1, further comprising:

assembling a first plurality of contiguous small page sized regions of the host physical memory into a single large page sized region of the host physical memory.

6. The method of claim 5, wherein the assembling occurs subsequent to the detecting the first memory access and prior to the generating the first entry in the hierarchically arranged second layer address translation table.

7. The method of claim 5, further comprising:

generating a second entry in the hierarchically arranged second layer address translation table, the second entry being at the least one hierarchical level above the hierarchically lowest level of tables such that a third range of memory, identified by the second entry, can be identified without reference to any table in the hierarchically lowest level of tables, the third range of memory referencing the single large page sized region of the host physical memory into which the first plurality of the contiguous small page sized regions of the host physical memory were assembled; and

in response to generating the second entry in the hierarchically arranged second layer address translation table, marking as used a second plurality of entries in the hierarchically arranged page table, the second plurality of entries referencing the first plurality of the contiguous small page sized regions of the host physical memory which were assembled into the single large page sized region of the host physical memory.

8. The method of claim 7, further comprising:

copying data from a second plurality of small page sized regions of the host physical memory to at least a portion of the first plurality of the contiguous small page sized regions, the second plurality of small page sized regions being at least party discontinuous; and

invalidating a second plurality of entries in the hierarchically arranged second layer address translation table that referenced the second plurality of small page sized regions of the host physical memory, wherein entries of the second plurality of entries are at a hierarchically lowest level of tables;

wherein the generated second entry in the hierarchically arranged second layer address translation table is utilized in place of the second plurality of entries that were invalidated.

9. The method of claim 7, further comprising:

copying data from a second set of one or more small page sized regions of the host physical memory to at least a portion of the first plurality of the contiguous small page sized regions; and

invalidating a second plurality of entries in the hierarchically arranged second layer address translation table, the second plurality of entries comprising both: (1) a first subset of entries that reference the second set of the one or more small page sized regions of the host physical memory and (2) a second subset of entries that reference at least some of the first plurality of contiguous small page sized regions of the host physical memory, wherein entries of the second plurality of entries are at a hierarchically lowest level of tables;

wherein the generated second entry in the hierarchically arranged second layer address translation table is utilized in place of the second plurality of entries that were invalidated.

10. The method of claim 5, wherein the assembling the first plurality of contiguous small page sized regions of the host physical memory comprises copying data from some of the first plurality of contiguous small page sized regions to other small page sized regions of the host physical memory that differ from the first plurality of contiguous small page sized regions.

11. The method of claim 10, wherein the copying the data from the some of the first plurality of contiguous small page sized regions to the other small page sized regions is only performed if a fragmentation of the first plurality of contiguous small page sized regions is below a fragmentation threshold.

12. The method of claim 1, further comprising:

preventing paging of the second range of memory.

13. The method of claim 12, wherein the preventing the paging of the second range of memory is only performed if one or more portions of the second range of memory are accessed more frequently than an access frequency threshold.

14. The method of claim 12, further comprising removing the prevention of paging of the second range of memory if one or more portions of the second range of memory are accessed less frequently than an access frequency threshold.

15. The method of claim 1, wherein the second range of memory is 2 MB in size.

16. A computing device comprising:

one or more central processing units;

random access memory (RAM); and

one or more computer-readable media comprising:

a first set of computer-executable instructions, which, when executed by the computing device, cause the computing device to provide a memory manager referencing a hierarchically arranged page table to translate host virtual memory addresses to host physical memory addresses that identify locations on the RAM;

a second set of computer-executable instructions, which, when executed by the computing device, cause the computing device to provide a virtual machine computing environment, wherein processes executing within the virtual machine computing environment perceive guest physical memory addresses as being addresses to physical memory, and wherein further guest physical memory, identified by the guest physical memory addresses, is backed by a portion of host virtual memory, identified by a portion of the host virtual memory addresses; and

a third set of computer-executable instructions, which, when executed by the computing device, cause the computing device to:

detect a first memory access, from a first process executing in the virtual machine computing environment, directed to a first range of memory;

generate, as a precondition to completing the first memory access, a first entry in a hierarchically arranged second layer address translation table, the hierarchically arranged second layer address translation table correlating the host physical memory addresses to the guest physical memory addresses, the first entry being at least one hierarchical level above a hierarchically lowest level of tables such that a second range of memory, identified by the first entry, can be identified without reference to any table in the hierarchically lowest level of tables, the second range of memory being greater than the first range of memory; and

in response to generating the first entry in the hierarchically arranged second layer address translation table, mark as used a first plurality of entries in the hierarchically arranged page table, the first plurality of entries referencing, in aggregate, the same second range of memory as the first entry in the hierarchically arranged second layer address translation table, wherein entries of the first plurality of entries are at a hierarchically lowest level of tables.

17. The computing device of claim 16, wherein the third set of computer-executable instructions comprises further computer-executable instructions, which, when executed by the computing device, cause the computing device to :

detect, after the first memory access completes, that a first subset of the first plurality of entries in the hierarchically arranged page table have had data, that was originally stored in corresponding host physical memory addresses, subsequently paged out to a non-volatile storage medium;

invalidate, in response to the detecting, the first entry in the hierarchically arranged second layer address translation table; and

generate, in place of the first entry in the hierarchically arranged second layer address translation table, a second plurality of entries in the hierarchically arranged second layer address translation table, the second plurality of entries referencing, in aggregate, at least some of the same second range of memory as the first entry, wherein entries of the second plurality of entries are at a hierarchically lowest level of tables.

18. The computing device of claim 16, wherein the third set of computer-executable instructions comprises further computer-executable instructions, which, when executed by the computing device, cause the computing device to :

assemble a first plurality of contiguous small page sized regions of the host physical memory into a single large page sized region of the host physical memory;

wherein the assembling occurs subsequent to the detecting the first memory access and prior to the generating the first entry in the hierarchically arranged second layer address translation table.

19. The computing device of claim 16, wherein the third set of computer-executable instructions comprises further computer-executable instructions, which, when executed by the computing device, cause the computing device to :

prevent paging of the second range of memory.

20. One or more computer-readable storage media comprising computer-executable instructions, which when executed, cause a computing device to :

detect a first memory access, from a first process executing in a virtual machine computing environment, directed to a first range of memory;

generate, as a precondition to completing the first memory access, a first entry in a hierarchically arranged second layer address translation table, the hierarchically arranged second layer address translation table correlating host physical memory address to guest physical memory addresses, the first entry being at least one hierarchical level above a hierarchically lowest level of tables such that a second range of memory, identified by the first entry, can be identified without reference to any table in the hierarchically lowest level of tables, the second range of memory being greater than the first range of memory; and

in response to generating the first entry in the hierarchically arranged second layer address translation table, mark as used a first plurality of entries in a hierarchically arranged page table, the hierarchically arranged page table correlating the host physical

memory addresses to host virtual memory addresses, the first plurality of entries referencing, in aggregate, the same second range of memory as the first entry in the hierarchically arranged second layer address translation table, wherein entries of the first plurality of entries are at a hierarchically lowest level of tables;

wherein the guest physical memory addresses are perceived as being addresses to physical memory by processes executing within the virtual machine computing environment;

wherein the host physical memory addresses are addresses to actual physical memory of a host computing device hosting the virtual machine computing environment;

wherein the host virtual memory addresses are addresses to virtual memory provided by a memory manager executing on the host computing device, the memory manager utilizing the hierarchically arranged page table to provide the virtual memory; and

wherein guest physical memory, identified by the guest physical memory address, is backed by a portion of host virtual memory, identified by a portion of the host virtual memory addresses.