BIT MAPPING SCHEME FOR AN LDPC CODED 16APSK SYSTEM

FIELD OF THE INVENTION

[0001] The invention relates to digital communications and in particular to a bit mapping scheme for an LDPC coded 16APSK System.

RELATED APPLICATIONS

[0002] This application relates to Application Serial No. _____, titled "A Bit Mapping Scheme for an LDPC Coded 32APSK System" filed on #####, and Application Serial No.____, titled "An Interleaving Scheme for an LDPC Coded 16APSK System" filed on ##### .

BACKGROUND OF THE INVENTION

[0003] Forward Error Control (FEC) coding is used by communications systems to ensure reliable transmission of data across noisy communication channels. Based on Shannon's theory, these communication channels exhibit a fixed capacity that can be expressed in terms of bits per symbol at a given Signal to Noise Ratio (SNR), which is defined as the Shannon limit. One of the research areas in communication and coding theory involves devising coding schemes offering performance approaching the Shannon limit while maintaining a reasonable complexity. It has been shown that LDPC codes using Belief Propagation (BP) decoding provide performance close to the Shannon limit with tractable encoding and decoding complexity.

[0004] In a recent paper Yan Li and William Ryan, "*Bit-Reliability Mapping in LDPC-Codes Modulation systems*", IEEE Communications Letters, vol. 9, no. 1, January 2005, the authors studied the performance of LDPC-coded modulation systems with 8PSK. With the authors' proposed bit reliability mapping strategy, about 0.15 dB performance improvement over the non-interleaving scheme is achieved. Also the authors show that gray mapping is more suitable for high order modulation than other mapping scheme such as natural mapping.

BRIEF SUMMARY OF THE INVENTION

[0005] Various embodiments of the present invention are directed to a bit mapping scheme in a 16APSK modulation system. The techniques of these embodiments are particularly well suited for use with LDPC codes.

[0006] LDPC codes were first described by Gallager in the 1960s. LDPC codes perform remarkably close to the Shannon limit. A binary (*N*, *K*) LDPC code, with a code length *N* and dimension *K*, is defined by a parity check matrix **H** of (*N-K*) rows and *N* columns. Most entries of the matrix **H** are zeros and only a small number the entries are ones, hence the matrix **H** is sparse. Each row of the matrix **H** represents a check sum, and each column represents a variable, e.g., a bit or symbol. The LDPC codes described by Gallager are regular, i.e., the parity check matrix **H** has constant-weight rows and columns.

[0007] Regular LDPC codes can be extended to form irregular LDPC codes, in which the weight of rows and columns vary. An irregular LDPC code is specified by degree distribution polynomials $v(x)$ and $c(x)$, which define the variable and check node degree distributions, respectively. More specifically, the irregular LDPC codes may be defined as follows:

$$v(x) = \sum_{j=1}^{d_{v\max}} v_j x^{j-1} , \qquad (1)$$

and

$$c(x) = \sum_{j=1}^{d_{c\max}} c_j x^{j-1} , \qquad (2)$$

where the variables $d_{v\max}$ and $d_{c\max}$ are a maximum variable node degree and a check node degree, respectively, and $v_j(c_j)$ represents the fraction of edges emanating from variable (check) nodes of degree j. While irregular LDPC codes can be more complicated to represent and/or implement than regular LDPC codes, it has been shown, both theoretically and empirically, that irregular LDPC codes with properly selected degree distributions outperform regular LDPC codes. FIG. 1 illustrates a parity check matrix representation of an exemplary irregular LDPC code of codeword length six.

[0008] LDPC codes can also be represented by bipartite graphs, or Tanner graphs. In Tanner graph, one set of nodes called variable nodes (or bit nodes) corresponds to the bits of the codeword and the other set of nodes called constraints nodes (or check nodes) corresponds the set of parity check constrains which define the LDPC code. Bit nodes and check nodes are connected by edges, and a bit node and a check node are said to be neighbors or adjacent if they are connected by an edge. Generally, it is assumed that a pair of nodes is connected by at most one edge.

[0009] FIG. 2 illustrates a bipartite graph representation of the irregular LDPC code illustrated in FIG. 1.

[0010] LDPC codes can be decoded in various ways such as majority-logic decoding and iterative decoding. Because of the structures of their parity check matrices, LDPC codes are majority-logic decodable. Although majority-logic decoding requires the least complexity and achieves reasonably good error performance for decoding some types of LDPC codes with relatively high column weights in their parity check matrices (e.g., Euclidean geometry LDPC and projective geometry LDPC codes), iterative decoding methods have received more attention due to their better performance versus complexity tradeoffs. Unlike majority-logic decoding, iterative decoding processes the received symbols recursively to improve the reliability of each symbol based on constraints that specify the code. In a first iteration, an iterative decoder only uses a channel output as input, and generates reliability output for each symbol.

[0011] Subsequently, the output reliability measures of the decoded symbols at the end of each decoding iteration are used as inputs for the next iteration. The decoding process continues until a stopping condition is satisfied, after which final decisions are made based on the output reliability measures of the decoded symbols from the last iteration. According to the different properties of reliability measures used during each iteration, iterative decoding algorithms can be further divided into hard decision, soft decision and hybrid decision algorithms. The corresponding popular algorithms are iterative bit-flipping (BF), belief propagation (BP), and weighted bit-flipping (WBF) decoding, respectively. Since BP algorithms have been proven to provide maximum likelihood decoding when the underlying Tanner graph is acyclic, they have become the most popular decoding methods.

[0012] BP for LDPC codes is a type of message passing decoding. Messages transmitted along the edges of a graph are log-likelihood ratio (LLR) $\log\frac{p_0}{p_1}$ associated with variable nodes corresponding to codeword bits. In this expression p_0 and p_1 denote the probability that the associated bit value becomes either a 0 or a 1, respectively. BP decoding generally includes two steps, a horizontal step and a vertical step. In the horizontal step, each check node c_m sends to each adjacent bit b_n a check-to-bit message which is calculated based on all bit-to-check messages incoming to the check c_m except one from bit b_n. In the vertical step, each bit node b_n sends to each adjacent check node c_m a bit-to-check message which is calculated based on all check-to-bit messages incoming to the bit b_n except one from check node c_m. These two steps are repeated until a valid codeword is found or the maximum number of iterations is reached.

[0013] Because of its remarkable performance with BP decoding, irregular LDPC codes are among the best for many applications. Various irregular LDPC codes have been accepted or being considered for various communication and storage standards, such as DVB-S2/DAB, wireline ADSL, IEEE 802.11n, and IEEE 802.16.

[0014] The threshold of an LDPC code is defined as the smallest SNR value at which, as the codeword length tends to infinity, the bit error probability can be made arbitrarily small. The value of threshold of an LDPC code can be determined by analytical tool called density evolution.

[0015] The concept of density evolution can also be traced back to Gallager's results. To determine the performance of BF decoding, Gallager derived formulas to calculate the output BER for each iteration as a function of the input BER at the beginning of the iteration, and then iteratively calculated the BER at a given iteration. For a continuous alphabet, the calculation is more complex. The probability density functions (pdf's) of the belief messages exchanged between bit and check nodes need to be calculated from one iteration to the next, and the average BER for each iteration can be derived based on these pdf's. In both check node processing and bit node processing, each outgoing belief message is a function of incoming belief messages.

For a check node of degree d_c, each outgoing message U can be expressed by a function of $d_c - 1$ incoming messages,

$$U = F_c(V_1, V_2, \ldots, V_{d_c-1}),$$

where F_c denotes the check node processing function which is determined from BP decoding. Similarly, for bit node of degree d_v, each outgoing message V can be expressed by a function of $d_v - 1$ incoming messages and the channel belief message U_{ch},

$$V = F_V(U_{ch}, U_1, U_2, \ldots, U_{d_v-1}),$$

where F_v denotes the bit node processing function. Although for both check and bit node processing, the pdf of an outgoing message can be derived based on the pdf's of incoming messages for a given decoding algorithm, there may exist an exponentially large number of possible formats of incoming messages. Therefore the process of density evolution seems intractable. Fortunately, it has been proven in that for a given message-passing algorithm and noisy channel, if some symmetry conditions are satisfied, then the decoding BER is independent of the transmitted sequence x. That is to say, with the symmetry assumptions, the decoding BER of all-zero transmitted sequence $x = 1$ is equal to that of any randomly chosen sequence, thus the derivation of density evolution can be considerably simplified. The symmetry conditions required by efficient density evolution are channel symmetry, check node symmetry, and bit node symmetry. Another assumption for the density evolution is that the Tanner graph is cyclic free.

[0016] According to these assumptions, the incoming messages to bit and check nodes are independent, and thus the derivation for the pdf of the outgoing messages can be considerably simplified. For many LDPC codes with practical interests, the corresponding Tanner graph contains cycles. When the minimum length of a cycle (or girth) in a Tanner graph of an LDPC code is equal to $4 \times l$, then the independence assumption does not hold after the l-th decoding iteration with the standard BP decoding. However, for a given iteration number, as the code length increases, the independence condition is satisfied for an increasing iteration number.

Therefore, the density evolution predicts the asymptotic performance of an ensemble of LDPC codes and the "asymptotic" nature is in the sense of code length.

[0017] According to various embodiments of the invention, the bit mapping schemes provide good threshold of LDPC codes. Furthermore, the bit mapping schemes can facilitate the design of an interleaving arrangement in a 16APSK modulation system.

[0018] According to various embodiments of the invention, the disclosed bit mapping offers good performance of LDPC coded 16APSK system and simplifies an interleaving arrangement in 16APSK systems.

[0019] According to various embodiments of the invention, a method of bit mapping in a 16APSK system, wherein the system utilizes an FEC code, comprises: transmitting a digital signal from a transmitter; and receiving the digital signal at a receiver; wherein the digital signal utilizes a 16APSK system with FEC coding, and the signal is bit-mapped prior to the transmitting according to a formula embodied by Figure 4.

[0020] According to various embodiments of the invention, the FEC code is regular LDPC code.

[0021] According to various embodiments of the invention, the FEC code is irregular LDPC code.

[0022] According to various embodiments of the invention, the FEC code is regular repeat-accumulate code.

[0023] According to various embodiments of the invention, the FEC code is irregular repeat-accumulate code.

[0024] According to various embodiments of the invention, a digital communication system, comprises: a transmitter to transmit a digital signal; and a receiver to receive the digital signal; wherein the digital signal utilizes a 16APSK system with FEC coding, and the signal is bit-mapped prior to the transmitting according to a formula embodied by Figure 4.

[0025] According to various embodiments of the invention, a digital communication system comprises: a transmitter to transmit a digital signal; and a receiver to receive the digital signal; wherein the digital signal utilizes a 16APSK system with FEC coding, and the signal is bit-mapped using gray mapping, and bits of the digital signal are ordered based on the values of a log likelihood ratio from a communications channel.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the corresponding drawings and in which like reference numerals refer to similar elements and in which:

[0027] FIG. 1 is a parity check matrix representation of an exemplary irregular LDPC code of codeword length six.

[0028] FIG. 2 illustrates a bipartite graph representation of the irregular LDPC code illustrated in FIG. 1.

[0029] FIG. 3 illustrates the bit mapping block in 16APSK modulation, according to various embodiments of the invention.

[0030] FIG. 4 illustrates a bit map for 16APSK symbol, according to various embodiments of the invention.

[0031] FIG. 5 depicts an example of a communications system which employs LDPC codes and 16APSK modulation, according to various embodiments of the invention.

[0032] FIG. 6 depicts an example of a transmitter employing 16APSK modulation in FIG. 5, according to various embodiments of the invention.

[0033] FIG. 7 depicts an example of a receiver employing 16APSK demodulation in FIG. 5, according to various embodiments of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0034] Referring to the accompanying drawings, a detailed description will be given of exemplary encoded bit mapping methods using LDPC codes according to various embodiments of the invention.

[0035] Although the invention is described with respect to LDPC codes, it is recognized that the bit mapping approach can be utilized with other codes. Furthermore, it is recognized that this approach can be implemented with uncoded systems.

[0036] .FIG. 5 is an exemplary diagram of a communications system employing LDPC codes with 16APSK modulation, according to various embodiments of the present invention. The exemplary communications system includes a transmitter 501 which generates signal waveforms across a communication channel 502 to a receiver 503. The transmitter 501 contains a message source for producing a discrete set of possible messages. Each of these messages corresponds to a signal waveform. The waveforms enter the channel 502 and are corrupted by noise. LDPC codes are employed to reduce the disturbances introduced by the channel 502, and a 16APSK modulation scheme is employed to transform LDPC encoded bits to signal waveforms.

[0037] FIG. 6 depicts an exemplary transmitter in the communications system of FIG. 5 which employs LDPC codes and 16APSK modulation. The LDPC encoder 602 encodes information bits from source 601 into LDPC codewords. The mapping from each information block to each LDPC codeword is specified by the parity check matrix (or equivalently the generator matrix) of the LDPC code. The LDPC codeword is interleaved and modulated to signal waveforms by the interleaver/modulator 603 based on a 16APSK bit mapping scheme. These signal waveforms are sent to a transmit antenna 604 and propagated to a receiver shown in FIG. 7.

[0038] FIG. 7 depicts an exemplary receiver in FIG. 5 which employs LDPC codes and 16APSK demodulator. Signal waveforms are received by the receiving antenna 701 and distributed to demodulator/deinterleavor 702. Signal waveforms are demodulated by demodulator and deinterleaved by deinterleavor and then distributed to a LDPC decoder 703

which iteratively decodes the received messages and output estimations of the transmitted codeword. The 16APSK demodulation rule employed by the demodulator/deinterleaver 702 should match with the 16APSK modulation rule employed by the interleaver/modulator 603.

[0039] According to various embodiments of the invention, as shown in FIG. 3, the exemplary 16APSK bit-to-symbol mapping circuit utilizes four bits (b_{4i}, b_{4i+1}, b_{4i+2}, b_{4i+3}) each iteration and maps them into an I value and a Q value, with i=0, 1, 2, ... The bit mapping logic is shown in FIG. 4. According to various embodiments of the invention, the mappings of bits are defined by:

$$(I(i),Q(i)) = \begin{cases} (R_2\sin(\pi/12),-R_2\cos(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,0,0,0) \\ (R_1\sin(\pi/4),-R_1\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,0,0,1) \\ (R_2\sin(\pi/4),-R_2\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,0,1,0) \\ (R_2\cos(\pi/12),-R_2\sin(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,0,1,1) \\ (R_2\sin(\pi/12),R_2\cos(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,1,0,0) \\ (R_1\sin(\pi/4),R_1\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,1,0,1) \\ (R_2\sin(\pi/4),R_2\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,1,1,0) \\ (R_2\cos(\pi/12),R_2\sin(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,1,1,1) \\ (-R_2\sin(\pi/12),-R_2\cos(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,0,0,0) \\ (-R_1\sin(\pi/4),-R_1\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,0,0,1) \\ (-R_2\sin(\pi/4),-R_2\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,0,1,0) \\ (-R_2\cos(\pi/12),-R_2\sin(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,0,1,1) \\ (-R_2\sin(\pi/12),R_2\cos(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,1,0,0) \\ (-R_1\sin(\pi/4),R_1\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,1,0,1) \\ (-R_2\sin(\pi/4),R_2\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,1,1,0) \\ (-R_2\cos(\pi/12),R_2\sin(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,1,1,1) \end{cases}$$

[0040] According to various embodiments of the invention, the bit mapping scheme of FIG. 4 uses gray mapping, meaning the binary representations of adjacent points differ by only one bit. Density evolution analysis shows that given an LDPC coded 16APSK system, the exemplary gray mapping scheme can provide the best threshold. The bit mapping scheme of FIG. 4 also arranges bits in an order based on the values of a log likelihood ratio from the communications channel. This arrangement simplifies the design of interleaving scheme for 16APSK system.

[0041] Although the invention has been described by the way of exemplary embodiments, it is to be understood that various other adaptations and modifications may be made within the spirit and scope of the invention. Therefore, it is the object of the appended claims to cover all such variations and modifications as come within the true spirit and scope of the invention.

CLAIMS

We claim:

1. A method of digital mapping in a 16APSK system, the method comprising:

transmitting a digital signal from a transmitter; and

receiving the digital signal at a receiver;

wherein the digital signal is bit-mapped prior to the transmitting according to the following formula, wherein R_1 is a radius of an inner ring and R_2 is a radius of an outer ring:

$$(I(i),Q(i)) = \begin{cases} (R_2\sin(\pi/12),-R_2\cos(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,0,0,0) \\ (R_1\sin(\pi/4),-R_1\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,0,0,1) \\ (R_2\sin(\pi/4),-R_2\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,0,1,0) \\ (R_2\cos(\pi/12),-R_2\sin(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,0,1,1) \\ (R_2\sin(\pi/12),R_2\cos(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,1,0,0) \\ (R_1\sin(\pi/4),R_1\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,1,0,1) \\ (R_2\sin(\pi/4),R_2\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,1,1,0) \\ (R_2\cos(\pi/12),R_2\sin(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,1,1,1) \\ (-R_2\sin(\pi/12),-R_2\cos(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,0,0,0) \\ (-R_1\sin(\pi/4),-R_1\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,0,0,1) \\ (-R_2\sin(\pi/4),-R_2\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,0,1,0) \\ (-R_2\cos(\pi/12),-R_2\sin(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,0,1,1) \\ (-R_2\sin(\pi/12),R_2\cos(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,1,0,0) \\ (-R_1\sin(\pi/4),R_1\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,1,0,1) \\ (-R_2\sin(\pi/4),R_2\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,1,1,0) \\ (-R_2\cos(\pi/12),R_2\sin(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,1,1,1) \end{cases}$$

2. The method of claim 1, wherein the system utilizes an FEC code.

3. A digital communication system, comprising:

a transmitter to transmit a digital signal;

wherein the digital signal utilizes a 16APSK system with FEC coding, and the signal is bit-mapped using gray mapping, and bits of the digital signal are ordered based on the values of a log likelihood ratio from a communications channel.

4. The method of claim 3, wherein the FEC code is regular LDPC code.

5. The method of claim 3, wherein the FEC code is irregular LDPC code.

6. The method of claim 3, wherein the FEC code is regular repeat-accumulate code.

7. The method of claim 3, wherein the FEC code is irregular repeat-accumulate code.

8. A digital communication system, comprising:

a transmitter to transmit a digital signal, wherein the transmitter modulates at least one mapping group having four bits (b_{4i}, b_{4i+1}, b_{4i+2}, b_{4i+3}), for i=0, 1, 2, ..., to a 16APSK symbol based on formula:

$$(I(i),Q(i)) = \begin{cases} (R_2\sin(\pi/12),-R_2\cos(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,0,0,0) \\ (R_1\sin(\pi/4),-R_1\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,0,0,1) \\ (R_2\sin(\pi/4),-R_2\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,0,1,0) \\ (R_2\cos(\pi/12),-R_2\sin(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,0,1,1) \\ (R_2\sin(\pi/12),R_2\cos(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,1,0,0) \\ (R_1\sin(\pi/4),R_1\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,1,0,1) \\ (R_2\sin(\pi/4),R_2\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,1,1,0) \\ (R_2\cos(\pi/12),R_2\sin(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,1,1,1) \\ (-R_2\sin(\pi/12),-R_2\cos(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,0,0,0) \\ (-R_1\sin(\pi/4),-R_1\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,0,0,1) \\ (-R_2\sin(\pi/4),-R_2\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,0,1,0) \\ (-R_2\cos(\pi/12),-R_2\sin(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,0,1,1) \\ (-R_2\sin(\pi/12),R_2\cos(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,1,0,0) \\ (-R_1\sin(\pi/4),R_1\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,1,0,1) \\ (-R_2\sin(\pi/4),R_2\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,1,1,0) \\ (-R_2\cos(\pi/12),R_2\sin(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,1,1,1) \end{cases}$$

where R_1 is a radius of an inner ring and R_2 is a radius of an outer ring.

9. A digital communication system, comprising:

a receiver to receive a digital signal, wherein the receiver comprises a demodulator to map 16APSK symbols to estimating messages of groups of four bits (b_{4i}, b_{4i+1}, b_{4i+2}, b_{4i+3}), for i=0, 1, 2, ..., based on a 16APSK constellation specification as follows:

$$(I(i),Q(i)) = \begin{cases} (R_2\sin(\pi/12),-R_2\cos(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,0,0,0) \\ (R_1\sin(\pi/4),-R_1\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,0,0,1) \\ (R_2\sin(\pi/4),-R_2\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,0,1,0) \\ (R_2\cos(\pi/12),-R_2\sin(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,0,1,1) \\ (R_2\sin(\pi/12),R_2\cos(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,1,0,0) \\ (R_1\sin(\pi/4),R_1\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,1,0,1) \\ (R_2\sin(\pi/4),R_2\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,1,1,0) \\ (R_2\cos(\pi/12),R_2\sin(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,1,1,1) \\ (-R_2\sin(\pi/12),-R_2\cos(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,0,0,0) \\ (-R_1\sin(\pi/4),-R_1\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,0,0,1) \\ (-R_2\sin(\pi/4),-R_2\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,0,1,0) \\ (-R_2\cos(\pi/12),-R_2\sin(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,0,1,1) \\ (-R_2\sin(\pi/12),R_2\cos(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,1,0,0) \\ (-R_1\sin(\pi/4),R_1\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,1,0,1) \\ (-R_2\sin(\pi/4),R_2\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,1,1,0) \\ (-R_2\cos(\pi/12),R_2\sin(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,1,1,1) \end{cases}$$

where R_1 is a radius of an inner ring and R_2 is a radius of an outer ring.

10. A computer readable medium to store a computer program in which a 16APSK modulation maps groups of four bits (b_{4i}, b_{4i+1}, b_{4i+2}, b_{4i+3}), for i=0, 1, 2, ..., to 16APSK symbols based on formula:

$$(I(i),Q(i)) = \begin{cases} (R_2\sin(\pi/12),-R_2\cos(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,0,0,0) \\ (R_1\sin(\pi/4),-R_1\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,0,0,1) \\ (R_2\sin(\pi/4),-R_2\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,0,1,0) \\ (R_2\cos(\pi/12),-R_2\sin(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,0,1,1) \\ (R_2\sin(\pi/12),R_2\cos(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,1,0,0) \\ (R_1\sin(\pi/4),R_1\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,1,0,1) \\ (R_2\sin(\pi/4),R_2\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,1,1,0) \\ (R_2\cos(\pi/12),R_2\sin(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (0,1,1,1) \\ (-R_2\sin(\pi/12),-R_2\cos(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,0,0,0) \\ (-R_1\sin(\pi/4),-R_1\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,0,0,1) \\ (-R_2\sin(\pi/4),-R_2\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,0,1,0) \\ (-R_2\cos(\pi/12),-R_2\sin(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,0,1,1) \\ (-R_2\sin(\pi/12),R_2\cos(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,1,0,0) \\ (-R_1\sin(\pi/4),R_1\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,1,0,1) \\ (-R_2\sin(\pi/4),R_2\cos(\pi/4)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,1,1,0) \\ (-R_2\cos(\pi/12),R_2\sin(\pi/12)), & (b_{4i},b_{4i+1},b_{4i+2},b_{4i+3}) = (1,1,1,1) \end{cases}$$

where R_1 is a radius of an inner ring and R_2 is a radius of an outer ring.