

APPARATUS AND METHOD FOR IMPROVED DEPOSITION OF  
CONFORMAL LINER FILMS AND PLUGS IN HIGH ASPECT RATIO  
CONTACTS

5     Field of the Invention

                    This invention relates generally to the formation of  
conductive liners and the formation of conductive plugs or non-  
conductive plugs for creating electrical interconnections or circuit  
elements for integrated circuits (IC's). More particularly, the  
10     invention relates to the formation of conductive liners and  
conductive plugs in substrate contacts or apertures having high  
aspect ratios.

Background of the Invention

                    In the manufacturing of integrated circuits, and  
15     particularly, logic and memory circuits, the circuit structures utilized  
are increasingly dense and compact. Furthermore, current

integrated circuits are utilizing an increasingly larger number of interconnecting metal levels as well as increasingly higher interconnect densities per level. During IC fabrication, patterned series of holes, apertures and trenches are formed in the substrate, and specifically the holes/apertures are formed in the material layers of an IC substrate to provide for interconnection between the material layers. For example, when one substrate material layer is formed on top of another layer, a hole is made in the top layer to provide for interconnection to a lower layer. These holes and apertures are oftentimes referred to in the art as contacts or vias and will be collectively referred to herein as "contacts". When making an interconnection between the layers, the contacts are filled with an appropriate metal plug. Sometimes the metal plug is preceded by the deposition of a liner film.

In the fabrication of IC devices, the various metal interconnect layers make electrical contact to the semiconductor substrate or to other levels of interconnections through the contacts. The contacts are formed in the various metal interconnect layers by etching, masking or other techniques known to a person of ordinary skill in the art. Once a contact is formed, the interconnecting metal layers or plugs are deposited into the

contact to provide for the electrical interconnection between the layers. Such films and layers can be deposited by generally known techniques such as chemical vapor deposition (CVD) or physical vapor deposition (PVD).

5                   One conventionally known physical vapor deposition technique is sputter deposition. In sputter deposition, a target of material, such as a metal target, is positioned in a vacuum chamber generally opposite a substrate which is to receive a layer or plug of material. A working gas is introduced into the vacuum chamber  
10 proximate the target and is electrically excited to create a gas plasma including positively charged gas ions. The target is negatively biased and the ionized plasma species bombard the negative target, thus dislodging material or "sputtering" the target. The dislodged or sputtered material deposits onto the substrate  
15 surface and thus covers the substrate surface and thereby lines or fills any contacts formed in the exposed substrate surface.

                  In the drive toward more dense and compact circuit structures on a substrate, the critical dimensions of the interconnect contacts are made increasingly smaller. The "aspect  
20 ratio" of a contact is the ratio of the contact length to its width (or diameter if the contact hole is circular). With smaller contact

dimensions, the contact aspect ratios are becoming increasingly higher. Such high aspect ratio contacts are difficult to fill due to the obstruction of the sputtered material by the high contact walls and resulting shadowing of portions of the contacts interior.

5        However, the smaller architecture of current IC technology is desirable for improved performance and lower cost.

             While sputter deposition has proven to be generally useful for conductive liner films and conductive plugs, the conventional sputter deposition techniques present problems when  
10        depositing such films and plugs into contacts having very high aspect ratios, e.g., aspect ratios  $\geq 1.5$ . As such, when the aspect ratio of a contact exceeds 1, conventional sputter deposition becomes less effective at depositing material into the bottom and sides of the contact. The physical shadowing of the contact side  
15        walls results in a tapered sidewall deposition, and the contact has little deposition in the bottom corner. As may be appreciated, this problem becomes worse as the contact aspect ratios increase.

             One known technique of improving bottom and side wall coating or coverage in high aspect ratio contacts is to use a  
20        plate collimator. The plate collimator is typically positioned parallel to the substrate. A collimator has a series of tubes, the walls of

which intercept some of the material sputtered from the target.

The sputtered material or flux incident at an angle far from  $0^\circ$  (with respect to the collimator perpendicular) are removed. Only the

portion of the flux incident within an angle proportional to the ratio

5 of the collimator hole diameter to hole height is allowed to pass through the collimator. As this ratio decreases, the aspect ratio of the collimator tubes increases, and a greater percentage of the total flux is incident on the substrate within a very small angle from

perpendicular. However, while high aspect ratio plate collimators

10 may offer suitable deposition, they produce a large reduction in the deposition rate and reduce the efficiency of target utilization

because much of the sputtered material is deposited on the collimator. The invention allows lower aspect ratio collimators to achieve deposition profiles similar to high aspect collimators and

15 reduces the impact on deposition rate and target utilization.

Further, the invention allows greater utilization of the collimator by reducing the rate of material build-up thereon.

Relatively recently, the use of titanium and titanium nitride has become desirable for lining contacts. Collimator

20 techniques for depositing conductors such as titanium and titanium nitride will generally produce films which exhibit low resistivity, low

impurity concentrations and regular crystal morphologies.

However, conventional collimation processes still have undesirable drawbacks which reduce the reliability of subsequent

interconnection processes. One such drawback is that the

5 deposition inside the contact still may be generally non-uniform

with inadequate material in the corners of the contact. For

example, Fig. 1 illustrates a substrate 10 having an upper surface

12 receiving a layer of deposited material 14. A contact 16 formed

in substrate 10 has sidewall 18 and a bottom surface 20. As

10 shown in Fig. 1, sputter deposition by conventionally known

collimation techniques produces a liner film 22 on the sidewall 18

which is tapered from top to bottom and which can produce

discontinuities in the bottom corners 21 of the contact 16. The

tapered sidewall film 22 and the corner discontinuities may result in

15 electrical failure of the interconnection.

An additional drawback results from the buildup of material at the opening of the contact 16 proximate surface 12.

Referring again to Fig. 1, the rounded buildup 24, which is

commonly referred to as "overhang", protrudes into the contact

20 opening and shadows the sidewall 18 of the contact 16. The

overhang then results in voids, sometimes referred to as keyholes,

within the plug subsequently deposited in the contact. Referring to Fig. 2, a conductive liner film 26, such as titanium or titanium nitride, might be deposited by sputter deposition or CVD (see Fig. 1), and then a plug layer 28, such as aluminum or tungsten, would  
5 be deposited over the liner film 26 to fill the contact 16. A plug layer of aluminum might be deposited by sputtering or a plug layer of tungsten might be deposited by CVD. During the plug filling process, the rounded overhang 24 at the contact opening grows faster than the plug layer 28 resulting in the contact opening  
10 closing off before the contact is completely filled with the deposited material. Depending upon the processing temperature, the plug layer 28 may not flow to the bottom of the contact 16, leaving a void 30 therein often referred to as a keyhole. Such keyholes appear due to premature contact closing both in sputter deposited  
15 aluminum and CVD deposited tungsten and are particularly troublesome in contacts having high aspect ratios. The keyhole voids result in an unreliable electrical contact which degrades the manufacturing yield and reduces the number of usable devices per substrate.

20 Accordingly, it is an objective of the invention to improve the capability of filling contacts with conductive materials.

It is a further objective of the present invention to produce conformal liner layers in contacts having high aspect ratios.

It is a further objective of the present invention to increase the reliability of the electrical contacts made within high aspect ratio contact holes.

It is a further objective of the present invention to reduce the tapered sidewalls and overhang in conductive layers deposited into contacts.

It is still a further objective of the present invention to produce conductive plugs which are free from openings, keyholes or voids and thus provide more reliable electrical interconnections between wafer layers.

It is another objective of the present invention to increase the manufacturing yield of substrates having high aspect ratio contacts and thus increasing the number of usable devices from a substrate wafer.

It is a further objective of the present invention to extend collimator lifetime.

**Summary of the Invention**

The present invention provides improved bottom and sidewall coverage during sputter deposition, and particularly provides improved coverage for substrates utilizing contacts with high aspect ratios. The invention is utilized to deposit liner films and conductor plugs which are more uniformly conformal to thus enhance the electrical reliability of the interconnects formed therewith. Additionally, the present invention reduces the overhang buildup at the opening of the contact to provide for void-free interconnect plugs. The invention further facilitates plugging contacts with conductive materials.

The present invention utilizes a sputter deposition system comprising a collimator in combination with an electrical biasing system which is operably coupled to the substrate during sputter deposition to bias the substrate. The collimator is positioned between a material target and a substrate and it is configured to intercept sputtered particles of a predetermined angular incidence to promote uniform deposition into the substrate contacts, and particularly into contacts having high aspect ratios. An electrical biasing system is operably coupled to the substrate during sputter deposition for biasing the substrate such that ions

from the sputtering plasma bombard the substrate surface and effectively etch the surface contemporaneously with the sputter deposition. The collimator provides near-normal incidence of the sputter deposition particles for growing a film in high aspect ratio contacts. By electrically biasing the wafer negatively with respect to the collimator, the contemporaneous ion bombardment of the growing layer occurs. The collimator affects the ion bombardment of the substrate with near-normal incidence of the ions on the growing substrate layer to produce the benefits and results of the present invention.

The contemporaneous sputter deposition and normally incident ion bombardment effectively redistributes the material which is contained in the rounded deposits or overhang at the opening of the contact. The redistributed material is transferred into the contact and onto the flat field of the substrate resulting in a more uniformly conformal liner film or plug within the contact. The present invention provides more uniform conformal liner layer without a substantial overhang at the opening of the contact. Material layers subsequently deposited onto the substrate and plugs deposited into the contacts are generally free of voids or keyholes thus minimizing electrical failures of the interconnects provided by

such layers and plugs. This, in turn, increases manufacturing yield of devices and circuits from a substrate. Furthermore, the present invention provides significantly improved flat field uniformity characteristics over conventional non-biased collimation (i.e.,  
5 collimation without substrate bias). For example, the sheet resistance uniformity and reflectivity is improved with respect to a non-biased collimation technique.

In the preferred embodiment of the present invention, a collimator having an aspect ratio between 1 and 2 is utilized. The  
10 combination of such a collimator and a biased substrate provides uniformly conformal deposition and reduces the overhang to the extent that would normally only be possible with a collimator having a higher aspect ratio, such as 2 to 3. With the lower aspect ratio collimator utilized with the present invention, the deposition  
15 rate is not as significantly reduced as would be the case with a higher aspect ratio collimator. That is, less of the sputter deposited material is collected by the collimator and thus more is available for deposition on the substrate. The present invention is particularly useful for deposition of liner layers and plugs within sub-micron  
20 (mm), high aspect ratio contacts.

The above and other objects and advantages of the present invention shall be made apparent from the accompanying drawings and the description thereof.

Brief Description of the Drawings

5                   The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and, together with a general description of the invention given above, and the detailed description of the embodiments given below, serve to explain the principles of the  
10                   invention.

Fig. 1 is a cross-sectional view of a contact having a material layer deposited with conventional collimator;

Fig. 2 is a cross-sectional view of a contact illustrating a material layer deposited in the substrate contact of Fig.  
15                   1;

Fig. 3 is a diagrammatic cross-sectional view of a sputter deposition configuration for practicing the present invention;

Fig. 4A is a graph of deposition rate and substrate current as a function of RF bias voltage in accordance with the  
20                   principles of the present invention, while Fig. 4B is a graph of deposition rate and substrate current as a function of a DC bias

voltage further in accordance with the principles of the present invention;

Fig. 4C is a graph of the ratio of net sputtered flux obtained using a collimator and substrate bias to the sputtered flux using a collimator without substrate bias plotted as a function of DC bias voltage;

Fig. 4D is a bar graph of deposition rate as a function of substrate bias voltage;

Fig. 5A is a bar graph of the measured resistivity of a substrate as a function of substrate bias voltage, while Fig. 5B is a bar graph of sheet resistance uniformity of a substrate coated in accordance with the principles of the present invention as a function of substrate bias voltage.

Figs. 6A, 6B and 6C are sheet resistance uniformity maps for 0 V, 250 V, and 450 V RF substrate bias voltages, respectively;

Fig. 7 is a bar graph of the measured reflectivity of substrates coated in accordance with the principles of the present invention as a function of substrate bias voltage.

Figs. 8A, 8B and 8C are photographs of various substrate contact liners with a conformal film deposited with 450 V RF substrate bias in accordance with the invention.

Detailed Description of Specific Embodiments

5                    Fig. 3 illustrates an equipment configuration for practicing the present invention. Specifically, the sputter deposition system 30 for practicing the present invention includes a processing housing 32 which defines therein a processing chamber 34 for containing a substrate. Housing 32 is operably coupled to a  
10                    vacuum system 36 for creating a vacuum in chamber 34. A suitable system for practicing the present invention is the Eclipse Mark II available from Materials Research Corporation of Congers, New York. Within chamber 34 a substrate 38 is supported on a substrate support 40 which is preferably operable to clamp  
15                    substrate 38 thereto and provides a backside heating gas (not shown) between the backside of substrate 38 and a surface of support 40 for efficient heating of the substrate.

                    Positioned opposite substrate 38 in the chamber 34 is a target mount 42 which is bonded to a target 44 of material to be  
20                    deposited onto the upper surface 45 of substrate 38. Positioned between the target 44 and substrate 38 is a collimator 46 having a

plurality of apertures 48 defined therein. The apertures 48 may be either hexagonally or circularly shaped and collimator 46 provides interception of particles sputtered from target 44 to yield sputter particles which are properly directed to impinge upon substrate surface 45 and fill or line contacts formed therein to provide a liner layer or plug. A shield 50 surrounds target 44 and prevents sputter deposition particles from depositing onto the walls of chamber 34. The shield 50 is preferably grounded and may be removed and replaced during periodic maintenance of the system 30.

10                   The target support 42 and target 44 are electrically connected to a DC power supply for biasing the target 44. As illustrated in Fig. 3, target 44 is negatively biased with respect to collimator 46 which is maintained at ground potential. During deposition, gas is introduced into chamber 34 from a process gas supply 54. The gas is preferably introduced between the cathode target 44 and collimator 46. Power is coupled to the process gas in chamber 34 to ignite a plasma which is illustrated in Fig. 3 as a plasma cloud 56. Contained within plasma cloud 56 are various positively charged ions 58 which are attracted to the negative cathode target 44 and thereby bombard the target. Target particles are dislodged or sputtered from target 44 as illustrated by reference

numeral 60 and appropriate arrows. Some of the sputtered particles 60 travel in the process chamber 34 toward substrate 38. Some of these particles 60 have angles of flight which cause them to collide with the collimator 46 at or exceeding a predetermined angle of incidence such that they are intercepted. Those target particles 60 which have angles of incidence relative to the plane of the collimator below the predetermined angle are not intercepted by collimator 46 and deposit upon substrate surface 45. The predetermined angle of incidence below which sputtered particles are intercepted by the collimator is a function of the diameter and depth of the collimator apertures 48, as is well known to those skilled in the art and therefore not further discussed herein.

The apertures 48 of collimator 46 have a defined height or depth 62 and width or diameter 64. The ratio of the depth 62 to the width 64 is defined as the aspect ratio of the collimator 46. As may be appreciated, collimator apertures 48 with high aspect ratios have deep depths 62 and/or narrow widths 64 and will generally intercept a greater number of sputter particles 60 than will collimator apertures having smaller aspect ratios (i.e., wide and/or shallow apertures). For example, sputter particle 60b has an angle of incidence  $\phi$  from target surface 57 relative to the plane of

the collimator which will ensure that it strikes the sidewalls of one of the apertures 48. However, sputtered particle 60a has a flight path which is more normal to surface 57 and thus has an angle of incidence  $\theta$  which will avoid collision with the sidewalls of

5 collimator apertures 48 to pass through the collimator and deposit onto substrate surface 45 and thus contribute to creating a material layer or plug in a contact located on the substrate surface 45.

Collimators generally are utilized to provide sputter deposition of particles which have an angle of incidence to surface 45 which is

10 close to normal incidence. Those sputter particles 60 having flight paths which are angled away from a  $90^\circ$  or normal flight path will generally be intercepted by collimator 46. The greater the aspect ratio of the collimator apertures, the greater the percentage of sputtered particles which will be intercepted. As discussed

15 hereinabove, collimators provide assistance in filling contacts by removing those sputtered particles which tend to deposit as an overhang close the opening of the contact. However, it is appreciated the interception of sputter particles by the collimator 46 will reduce the deposition rate of the sputter deposition and will

20 decrease the efficiency of target utilization because a large number

of the sputtered particles deposit onto the collimator 46 rather than substrate 38.

To fill contacts having very high aspect ratios, a collimator with a high aspect ratio apertures, such as 2.5 or above, might be utilized. However, the resulting reduction in the deposition rate reduces the efficiency of the sputter deposition process and increases the overall cost thereof. The present invention provides conformal coating of high aspect ratio contacts utilizing a collimator 46 having an aspect ratio which is lower than the aspect ratio normally required with conventional collimator techniques. The invention thereby effectively increases the deposition rate over that achieved with a conventional collimator. In other words, the present invention provides a conformal liner in a sub-micron, high aspect ratio contact which would normally only be possible with a collimator having a relatively high aspect ratio.

In accordance with the principles of the present invention, substrate support 40 and substrate 38 are operably connected to a biasing source to provide a bias to the substrate 38 during sputter deposition. Referring to Fig. 3, substrate 38 is coupled to either an AC or pulsed DC source 70 or a DC source 72 for biasing the substrate.

Substrate 38 is negatively biased with respect to the collimator 46 which is typically maintained at ground potential. Ionized plasma particles of plasma cloud 56, such as particles 59, are attracted to the negatively biased substrate 38 to bombard surface 45. For example, while some of the particles 58 are attracted to the negative cathode target 44, other of the ionized particles 59 in the plasma 56 are attracted to the negatively biased substrate 38. Ionized particles 59 are attracted to surface 45 and bombard the surface and thereby etch the layer of sputter deposited material thereon.

Furthermore, in accordance with the principles of the present invention, some of the ionized particles 59 attracted to substrate 38 will collide with the collimator as illustrated by particle 59a to be intercepted by the collimator and prevented from etching surface 45. Other ionized particles, for example particle 59b, will pass through the collimator 46 to etch surface 45. In that way, the invention provides collimated etching and focuses the etching particles to have generally normal incidence upon surface 45. The invention provides more effective etching and redistribution of sputter deposited material within the contacts than conventional collimation.

One particular advantage of the invention is the redistribution of the sputter deposited material in the contacts to eliminate voids formed in the corners at the junctures of the sidewalls and bottom. Additionally, the contemporaneous sputter etch provided by the invention redistributes the overhang material into the contacts to provide a more uniform conformal liner layer. Reduction of the overhang will also aid in elimination of voids in the corners. While the present invention is useful with all contacts, it is particularly useful with sub-micron contacts having high aspect ratios. By providing a more uniform conformal liner, with little overhang at the contact opening, subsequent conductive plugs may be deposited into the contact without creating voids or keyholes therein. Therefore, the invention provides increased yield of devices and chips from a substrate and further provides increased reliability of the devices. In addition, the flat field properties of substrates yielded by the contemporaneous sputter deposition and etching of the invention are acceptable for the industry.

Various process runs were made utilizing the present invention to determine the flat field properties. For the process runs, an Eclipse Mark II system available from MRC was utilized as noted above. Substrates were processed with no bias (zero volts),

200 and 400 volt DC bias, and 250 and 450 volt RF bias (at 13.56 MHz). A series of 1500-5000 Å films were deposited between one and five wafers to obtain flat field data as discussed hereinbelow.

The wafer-to-wafer flat field properties were measured at the center

5 of the wafers, and averaged over two to five wafers depending upon the total number of wafers run at a given bias condition. Film

thicknesses of 2000 Å titanium (Ti) were deposited on virgin silicon (Si) wafers with 10 kÅ silicon dioxide (SiO<sub>2</sub>) to obtain reflectivity

and sheet resistance data. Film thicknesses of 2000 Å Ti were

10 deposited on virgin Si wafers with native oxide to obtain stress

data. Film thicknesses of 2000-5000 Å Ti were deposited on

patterned/active wafers for contact fill information.

The collimator utilized had an aspect ratio of 1.5, and

it is preferable to utilize a collimator with an aspect ratio in the

15 range of 1.25-2.0 for the invention. The holes of the collimator

were hexagonal and had a diameter of .625 inch, while the

thickness of the collimator plate was .938 inch. The spacing

maintained between the collimator and the substrate was 1.500

inches.

20 The sputter cathode utilized was an ICC-12 rotating magnet with a Ti target. The target to collimator spacing was

maintained at 1.452 inches. The rotating magnet behind the target to provide uniform sputter deposition was rotated at 140 rpm. 15 kW of power was delivered to the cathode target, and the substrate support 40 or backplane was maintained at 300°C with a  
5 backplane pressure of 6-8 Torr for thermal heat exchange purposes. A flow rate of 25 sccm argon (Ar) was utilized and resulted in a 1.1 mTorr operating pressure maintained within chamber 34.

### Process Results

#### Deposition Rate

10 Deposition rate was measured as a function of RF and DC bias. Total backplane current was also measured. DC backplane to ground current was measured with a multi-meter connected in series with the DC power supply or as a voltage drop over a series-connected precision resistor. The RF current  
15 measurements were made with a current transformer, such as a Current Monitor Model 4100 available from Pearson of Palo Alto, California, which had a sensitivity of 0.50 V/A and a  $\pm 3$  dB bandwidth of 140 Hz to 35 MHz. The current transformer output was terminated in 50 ohms at a monitoring oscilloscope.

20 The deposition rates were calculated from thickness measurements by using a pen-stripping lift-off process wherein a

strip of the sputter deposited layer is removed and the thickness of the film proximate the strip is measured for calculation of the deposition rate. The thickness measurements were made with a profiler, such as the Model P-1 Long Scan Profiler available from  
5 Tencor Instruments of Mountain View, California.

Fig. 4A illustrates graphs of measured wafer-to-ground current and the deposition rate for various RF bias voltages. As illustrated by Fig. 4A, for the deposition measurements more bias values were utilized than for determining the other flat-field  
10 properties. The reference arrows indicate which X-axis in the figure is associated with the particular curve. Referring to Fig. 4A, the current increased with RF bias whereas the deposition rate decreased.

Fig. 4B illustrates a graph of deposition rate and wafer-to-ground current as a function of the DC bias voltage. Fig. 4B  
15 shows a similar inverse relationship between the current and deposition rate as that illustrated in Fig. 4A wherein the current increases with increased DC bias whereas the deposition rate generally decreases. The increasing bias of the substrate reduces  
20 the effective deposition rate due to the resputtering that occurs at

the substrate 38 as increasing numbers of plasma ions 59 are attracted to the negatively biased substrate.

Net deposition rates were calculated for the measured DC bias currents. Assuming that the actual neutral and ion fluxes are spatially uniform, an estimate of the net deposition rate is given by the following equation:

#### EQUATION 1

Where  $\phi$  is the particle flux, and subscripts c and w refer to wafer deposition from the cathode, and wafer sputtering, respectively,

which occurs in the present invention. The flux of particles received by the wafer from the cathode is given by equation 2:

#### EQUATION 2

The flux of particles sputtered from the wafer is given by equation 3:

$$\phi_c = \rho \frac{R_d V}{w}$$

15

#### EQUATION 3

Where  $\rho$  = target material mass density,  $R$  = deposition rate,  $N_A$  = Avogadro's number,  $w$  = target material atomic weight

(mass/mol),  $I$  = ion current through wafer,  $Y$  = sputtering yield,  $e$

= process gas ion charge, and  $A$  = wafer area. Yield  $Y$  for the

argon/titanium system was obtained from the following equation:

#### EQUATION 4

$$Y = \frac{5.2}{U} \frac{Z_t}{Z_p} \left[ \frac{Z_p}{Z_t + Z_p} \right]^{0.67} E^{1/2}$$
 Where t = target, p = particle,  $Z_t$  = target atomic number,  $Z_p$  = ion energy in keV, Z = atomic number, and U = binding energy of surface atom in eV (from Applied Physics A36, 37 (1985)).

Both the theoretical and observed flux ratios  $\Phi_{\text{net}} / \Phi_c$  are shown in Fig. 4C. The theoretical curve 80 of Fig. 4C accurately predicts the measured reduction in deposition rate with increasing DC bias as a result of resputtering at the substrate 38. However, at 400 volts DC bias there is an anomalously high deposition rate which may be due to an uncertainty in the actual thickness measurement of the deposition.

Referring to Fig. 4D, the deposition rates are plotted in a bar format as a function of bias voltage. From the measured deposition rates, there is evidence that the DC bias may be more effective at resputtering the substrate than RF biasing for a given bias level.

### Sheet Resistance

The sheet resistance was measured at the wafer centers with a 4D Automatic Four Point Probe Meter, Model 280C available from Prometrics. Resistivity was derived by multiplying the sheet resistance measurement by the thickness of the deposited film, both at the center of the wafer. Resistivity is plotted in a bar graph format as a function of the bias voltage in Fig. 5A. As illustrated, the resistivity of the wafer tended to increase with the increasing bias voltage. The higher resistivity probably results from increased film defects and degradation of the film grain structure in the deposited layer as it is contemporaneously etched during deposition. Additionally, the incorporation of argon into the titanium is expected during biased deposition which will also act to increase the resistivity.

Fig. 5B illustrates the sheet resistance uniformity within a wafer (WiW) as a function of the bias voltage. As is illustrated, the sheet resistant uniformity generally improves with increased bias voltage. That is, there is a smaller percentage variation within the wafer for increased wafer bias.

Figs. 6A, 6B and 6C illustrate the improved sheet resistance uniformity for increasing RF bias. Fig. 6A illustrates the

interwafer sheet resistance uniformity for zero volts bias, whereas  
Figs. 6B and 6C illustrate the interwafer sheet resistance uniformity  
for 250 volt RF bias and 450 volt RF bias, respectively. As seen,  
the substrate of Fig. 6C has a substantially improved sheet  
5 resistance uniformity contour at 450 volt bias.

#### Reflectivity

Reflectivity measurements were made with a  
NanoSpec/AFT Microarea Gauge, available from Nanometrics of  
Sunnyvale, California, and are illustrated in a bar-graph format in  
10 Fig. 7. The range in reflectivity was predominantly above a typical  
acceptable lower limit of 120% for most of the biasing conditions.

#### Stress

Stress measurements were also made using a Model  
F2300 available from Flexus of Sunnyvale, California. The results  
15 of the stress measurements indicate that the residual stress  
decreased as RF bias was increased.

#### Process Run Data

Tables 1-4 below illustrate the various raw data  
measurements from several of the process runs made utilizing the  
20 present invention. Results of the process runs shown in the tables  
hereinbelow and from the Figs. discussed hereinabove illustrate that

the present invention produces acceptable flat-field performance as compared to standard, non-collimated processes.

The present invention further provides improved step coverage performance and deposition of conformal films and plugs within high aspect ratio, sub-micron contacts and in fact produces significant improvements in liner and plug deposition over prior art apparatus and methods. Figs. 8A, 8B and 8C are photographs of various contacts of substrates processed in accordance with the principles of the present invention and illustrating the improved step coverage and conformal film coverage.

Figs. 8A-8C show a deposition of titanium in sub-0.5 micron contacts in accordance with the principles of the present invention using a collimator having an aspect ratio of 1.5:1 and a 450 volt RF bias on the wafer. Fig. 8A illustrates a contact 90 having an aspect ratio of 3.5:1. The deposited film 92 is conformal and does not taper dramatically to the bottom corners to leave voids in the corners as resulted with prior art devices and methods (see Fig. 1). Furthermore, overhang 96 at the top of the contact is significantly reduced. Fig. 8B illustrates a more narrow contact 98 having a higher aspect ratio of 4.5:1, while Fig. 8C is an enlarged portion of the contact of Fig. 8B. As illustrated in Fig. 8B, and

more clearly in 8C, even with a sub-0.5 micron contact having a high aspect ratio of 4.5:1, the film 100 is very conformal and does not drastically taper down to the bottom corner 102 or produce voids in the corner 102. As illustrated in Fig. 8C, the film 100 is conformal on the sidewalls 104 and bottom 106 of the contact 98 and overhang 108 at the top of the contact is reduced (see Fig. 8B). Accordingly, the invention provides improved step coverage and conformality for the deposition in very small, high aspect ratio contacts. The reduction in overhang provided by the invention further reduces keyholing when a subsequent layer or plug is deposited in the lined contact (see Fig. 2).

TABLE 1

| REFLECTIVITY    |              |        |       |       |       |       |       |       |
|-----------------|--------------|--------|-------|-------|-------|-------|-------|-------|
| BIAS<br>(volts) | WAFER<br>NO. | CENTER |       |       | EDGE  |       |       |       |
|                 |              | 405nm  | 436nm | 480nm | 405nm | 436nm | 480nm |       |
| 5               | 0 V dc       | 3      | 111.4 | 123.0 | 137.3 | 108.9 | 120.7 | 134.7 |
|                 | 0 V dc       | 4      | 110.2 | 121.8 | 136.2 | 107.9 | 119.5 | 133.6 |
|                 | 0 V dc       | 5      | 108.8 | 120.6 | 135.1 | 106.8 | 118.3 | 132.1 |
|                 | 0 V dc       | 6      | 108.8 | 120.4 | 134.7 | 108.0 | 119.6 | 133.9 |
|                 | 0 V dc       | 7      | 108.5 | 120.1 | 134.6 | 106.1 | 117.8 | 131.9 |
| 10              | 250 rf       | 3      | 111.3 | 122.8 | 137.3 | 109.6 | 120.6 | 134.7 |
|                 | 250 rf       | 4      | 111.4 | 123.0 | 137.5 | 109.7 | 121.1 | 135.0 |
|                 | 450 rf       | 3      | 110.6 | 122.2 | 136.2 | 108.3 | 119.9 | 133.1 |
|                 | 450 rf       | 4      | 109.3 | 120.7 | 134.6 | 110.2 | 121.7 | 135.9 |
|                 | 200 dc       | 3      | 113.3 | 125.1 | 139.3 | 113.5 | 125.3 | 139.7 |
| 15              | 200 dc       | 4      | 113.5 | 125.2 | 139.3 | 113.1 | 125.0 | 139.0 |
|                 | 400 dc       | 3      | 107.4 | 118.4 | 132.2 | 108.6 | 119.7 | 133.5 |
|                 | 400 dc       | 4      | 106.2 | 117.8 | 131.2 | 106.8 | 118.0 | 132.0 |

TABLE 2

| DEPOSITION RATE |              |           |               |       |         |
|-----------------|--------------|-----------|---------------|-------|---------|
|                 | Bias (volts) | Wafer No. | Thickness (Å) | (Å/s) | Time(s) |
| 5               | 100 rf       | 3         | 1811.1        | 9.6   | 189     |
|                 | 250 rf       | 6         | 1767.0        | 9.3   | 189     |
|                 | 325 rf       | 9         | 1738.0        | 9.2   | 189     |
|                 | 450 rf       | 12        | 1738.0        | 9.2   | 189     |
|                 | 0 dc         | 15        | 1693.0        | 8.9   | 190     |
| 10              | 100 dc       | 3         | 1741.0        | 9.2   | 190     |
|                 | 200 dc       | 6         | 1706.0        | 9.0   | 190     |
|                 | 300 dc       | 9         | 1649.0        | 8.7   | 190     |
|                 | 400 dc       | 3         | 1709.0        | 9.0   | 190     |
|                 | 400 dc       | 12        | 1695.0        | 8.9   | 190     |
| 15              | 0 dc         | 3         | 1941.0        | 10.3  | 189     |
|                 | 0 dc         | 6         | 1968.0        | 10.4  | 189     |
|                 | 0 dc         | 9         | 1968.0        | 10.4  | 189     |
|                 | 0 dc         | 12        | 1935.0        | 10.2  | 189     |
|                 | 0 dc         | 15        | 1942.0        | 10.3  | 189     |
| 20              | 200 dc       | 7         | 1296.0        | 9.1   | 142     |
|                 | 200 dc       | 13        | 1676.0        | 8.9   | 189     |
|                 | 400 dc       | 10        | 1687.0        | 8.9   | 189     |
|                 | 400 dc       | 3         | 1676.0        | 8.9   | 189     |
|                 | 250 rf       | 3         | 4652.0        | 9.8   | 474     |
| 25              | 450 rf       | 12        | 1767.0        | 9.3   | 189     |
|                 | 450 rf       | 15        | 1763.0        | 9.3   | 8.9     |

TABLE 3

| Stress       |                |                         |
|--------------|----------------|-------------------------|
| BIAS (volts) | WAFER NO.      | (dyne/cm <sup>2</sup> ) |
| 0 dc         | 8              | -2.22E + 09             |
| 5 0 dc       | 9              | -2.11E + 09             |
| 250 rf       | 5              | -1.88E + 09             |
| 250 rf       | 6              | -1.86E + 09             |
| 450 rf       | 5              | -5.49E + 07             |
| 450 rf       | 6              | -6.89E + 06             |
| 10 200 dc    | 5              | -9.68E + 09             |
| 200 dc       | 6              | 3.67E + 09              |
| 200 dc       | 6 (second run) | 1.30E + 09              |
| 200 dc       | 7              | 4.58E + 09              |
| 400 dc       | 5              | -1.52E + 08             |
| 15 400 dc    | 6              | -2.54E-08               |

TABLE 4

| SHEET RESISTANCE |           |                               |                          |          |
|------------------|-----------|-------------------------------|--------------------------|----------|
| BIAS (volts)     | WAFER NO. | $\sigma(\mu\Omega\text{-cm})$ | $R_s (\Omega/\text{sq})$ | Unif (%) |
| 0 dc             | 3         | 62.02                         | 3.179                    | 4.77     |
| 0 dc             | 4         | 24.04                         | 3.283                    | 4.00     |
| 0 dc             | 5         | 63.70                         | 3.265                    | 4.16     |
| 0 dc             | 6         | 62.66                         | 3.212                    | 4.34     |
| 0 dc             | 7         | 61.69                         | 3.162                    | 4.42     |
| 250 rf           | 3         | 69.32                         | 3.737                    | 2.39     |
| 250 rf           | 4         | 69.55                         | 3.749                    | 1.97     |
| 450 rf           | 3         | 77.23                         | 4.375                    | 1.23     |
| 450 rf           | 4         | 76.80                         | 4.351                    | 1.19     |
| 200 dc           | 3         | 61.79                         | 3.633                    | 2.27     |
| 200 dc           | 4         | 61.20                         | 3.599                    | 1.59     |
| 400 dc           | 3         | 67.49                         | 4.014                    | 2.04     |
| 400 dc           | 4         | 68.83                         | 4.094                    | 2.16     |

While the present invention has been illustrated by a description of various embodiments and while these embodiments have been described in considerable detail, it is not the intention of the applicants to restrict or in any way limit the scope of the appended claims to such detail. Additional advantages and modifications will readily appear to those skilled in the art. The

invention in its broader aspects is therefore not limited to the  
specific details, representative apparatus and method, and  
illustrative example shown and described. Accordingly, departures  
may be made from such details without departing from the spirit or  
5 scope of applicant's general inventive concept.

What is claimed is:



WO 97/41598

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PCT/IB97/00522

Claims

1. A sputter deposition system including a vacuum chamber containing a sputtering plasma therein for sputter depositing a layer of material into substrate contacts having very small dimensions, the sputter deposition system comprising:
  - a target of deposition material positioned in the vacuum chamber and coupled to a target bias source for negatively biasing the target such that ions from the sputtering plasma bombard the target and produce material particles to deposit on a surface of a substrate in the chamber and into the substrate contacts;
  - a collimator positioned opposite the target and configured to intercept sputtered particles of a predetermined angular incidence to the substrate surface to promote uniform deposition into the substrate contacts;
  - an electrical biasing system operably coupled to the substrate during sputter deposition, the biasing system operable to bias the substrate such that ions from the sputtering plasma bombard the substrate surface and effectively etch the surface generally contemporaneously with the sputter deposition and redistribute the deposited particles in the contacts to reduce





THIS SHEET HAS BEEN  
REPLACED

WO 97/41598

PCT/IB97/00522

deposition overhang in the contacts and to further promote uniform  
deposition into the contacts;

whereby substrate contacts having large aspect ratios  
may be uniformly coated with a layer of material and filled with  
material with reduced numbers of voids.

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WO 97/41598

THIS SHEET HAS BEEN  
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PCT/IB97/00522

2. The sputter deposition system of claim 1 wherein the collimator is operably coupled to the substrate biasing system and the target bias source and acts as a common reference potential to both the target and the biased substrate.
3. The sputter deposition system of claim 1 wherein the substrate biasing system includes one of an AC source and a pulsed DC source for biasing the substrate during sputter deposition.
4. The sputter deposition system of claim 3 wherein the biasing source operates under 200 MHz.
5. The sputter deposition system of claim 3 wherein the biasing source operates under 20 MHz.
6. The sputter deposition system of claim 1 wherein the substrate biasing system includes a DC source for biasing the substrate with DC voltage during sputter deposition.





THIS SHEET HAS BEEN  
REPLACED

WO 97/41598

PCT/IB97/00522

7. The sputter deposition system of claim 1 wherein the substrate biasing system is operable to bias the substrate in the range of 10 to 5000 Volts.

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THIS SHEET HAS BEEN  
REPLACED

WO 97/41598

PCT/IB97/00522

8. A sputter deposition system including a vacuum chamber containing a sputtering plasma therein for sputter depositing a layer of material into substrate contacts having very small dimensions, the sputter deposition system comprising:
- a target of deposition material positioned in the vacuum chamber and coupled to a target bias source for negatively biasing the target such that ions from the sputtering plasma bombard the target and produce material particles to deposit on a surface of a substrate in the chamber and into the substrate contacts;
  - a collimator positioned opposite the target and configured to intercept sputtered particles of a predetermined angular incidence to the substrate surface to promote uniform deposition into the substrate contacts.
  - an electrical biasing system operably coupled to the substrate during sputter deposition, the biasing system operable to negatively bias the substrate such that ions from the sputtering plasma bombard the substrate surface and effectively etch the surface generally contemporaneously with the sputter deposition and redistribute the deposited particles in the contacts to reduce





WO 97/41598

THIS SHEET HAS BEEN  
REPLACED

PCT/IB97/00522

deposition overhang in the contacts and to promote uniform  
deposition into the contacts;

whereby substrate contacts having large aspect ratios  
may be uniformly coated with a layer of material and filled with  
material with reduced numbers of voids.

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REPLACED

WO 97/41598

PCT/IB97/00522

9. A sputter deposition system for sputter depositing a layer of material into substrate contacts having very small dimensions, the sputter deposition system comprising:
- a vacuum chamber;
  - a gas supply for providing gas into the chamber;
  - an excitation system for exciting the gas into a sputtering plasma containing ions;
  - a support for supporting, inside the chamber, a substrate with contacts having small dimensions;
  - a target support for supporting a target of deposition material in the chamber opposite the substrate support, the target support operable to bias a target thereon such that ions from the sputtering plasma bombard the target and produce material particles to deposit on a surface of the substrate and into the contacts;
  - a collimator positioned between the target support and the substrate support and configured to intercept sputtered particles of a predetermined angular incidence to the substrate surface to promote uniform deposition into and to promote voidless filling of the substrate contacts;

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WO 97/41598

THIS SHEET HAS BEEN  
REPLACED

PCT/IB97/00522

an electrical biasing system operably coupled to the substrate support during sputter deposition to bias the substrate thereon such that ions from the sputtering plasma bombard the substrate surface and effectively etch the surface contemporaneously with the sputter deposition and redistribute the deposited particles in the contacts to reduce deposition overhang in the contacts and to further promote uniform deposition into the contacts;

whereby substrates with contacts having very small aspect ratios may be uniformly coated with a layer of material and filled with material with reduced numbers of voids.





10. The sputter deposition system of claim 9 wherein the collimator is operably coupled to the substrate biasing system and the biased target support and acts a common reference potential to both the target and the biased substrate.
11. The sputter deposition system of claim 9 wherein the target support is operable to bias the target in the range of approximately 10 to 1,000 volts.
12. The sputter deposition system of claim 9 wherein the substrate biasing system is operable to bias the substrate in the range of approximately 10 to 5,000 Volts.
13. The sputter deposition system of claim 9 wherein the substrate biasing system includes one of an AC source and a pulsed DC source for biasing the substrate during sputter deposition.
14. The sputter deposition system of claim 13 wherein the biasing source operates between approximately DC and 20 MHz.



**WO 97/41598**

**PCT/IB97/00522**

15. The sputter deposition system of claim 13 wherein the AC or pulsed DC source operates between approximately 100 kHz and 20 MHz.

16. The sputter deposition system of claim 9 wherein the substrate biasing system includes a DC source for biasing the substrate with DC voltage during sputter deposition.



17. A method of sputter depositing a layer of material into substrate contacts having very small dimensions comprising:
- positioning a substrate in a vacuum chamber;
  - exciting a sputtering plasma containing ions within the chamber;
  - positioning a target of deposition material in the chamber opposite the substrate and biasing the target such that ions from the sputtering plasma bombard the target to produce the deposition of sputtered material particles onto a surface of the substrate and into contacts formed in the substrate surface;
  - intercepting sputtered particles of a predetermined angular incidence to the substrate surface to promote uniform deposition into and promote voidless filling of the substrate contacts;
  - biasing the substrate such that ions from the sputtering plasma bombard the substrate surface and effectively etch the surface generally contemporaneously with the sputter deposition and redistribute the deposited particles in the contacts to reduce deposition overhang in the contacts and to further promote uniform deposition into the contacts;



**WO 97/41598**

**PCT/IB97/00522**

whereby substrates with contacts having large aspect ratios may be uniformly coated with a layer of material and filled with material with reduced numbers of voids.



18. The method of claim 17 wherein the intercepting step includes positioning a collimator between the target and substrate to intercept sputtered particles, the method further comprising electrically coupling the substrate and the target to the collimator such that the collimator acts as a common reference potential to both the target and the biased substrate.

19. The method of claim 17 further comprising negatively biasing the substrate to etch the substrate surface with positively biased ions from the plasma.

20. The method of claim 17 further comprising biasing the target in the range of approximately 10 to 1,000 Volts.

21. The method of claim 17 further comprising biasing the substrate in the range of approximately 10 to 5,000 Volts.

22. The method of claim 17 further comprising biasing the substrate with AC voltage during sputter deposition.



**WO 97/41598**

**PCT/IB97/00522**

23. The method of claim 22 further comprising biasing the substrate between approximately DC and 20 MHz.

24. The method of claim 22 further comprising biasing the substrate between approximately 100 kHz and 20 MHz.

25. The method of claim 17 further comprising biasing the substrate with DC voltage during sputter deposition.



26. A method of sputter depositing a layer of material into substrate contacts having very small dimensions comprising:

positioning a target of material inside of a sputter deposition chamber;

positioning a substrate in the chamber opposite the target with a substrate surface having contacts formed therein facing the target;

bombarding the target with particles from an excited gas plasma to sputter deposit a material layer onto the substrate surface and into the contacts;

bombarding the substrate surface with particles to etch the substrate surface and material layer generally contemporaneously with the sputter deposition of the layer to redistribute the deposited material in the contacts to reduce deposition overhang in the contacts and to promote uniform deposition into the contacts;

whereby substrates with contacts having large aspect ratios may be uniformly coated with a layer of material and filled with material with a reduced number of voids.



27. The method of claim 26 further comprising intercepting sputtered particles of a predetermined angular incidence to the substrate surface to further promote uniform deposition into the substrate contacts.

28. The method of claim 26 wherein the intercepting step includes positioning a collimator between the target and substrate to intercept sputtered particles.

29. The method of claim 26 further comprising electrically coupling the substrate and the target to the collimator such that the collimator acts as a common reference potential to both the target and the substrate.

30. The method of claim 26 further comprising biasing the substrate to etch the substrate surface with positively biased ions from the plasma.