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SEMICONDUCTOR PACKAGE LEADFRAME ASSEMBLY AND METHOD OF MANUFACTURE

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to packaged semiconductors, semiconductor packages, leadframe assemblies therefor and a method of manufacture, and more particularly, but not by way of limitation, to a semiconductor leadframe and method incorporating a reverse-down set portion in a region of the tie bar for its securement within the semiconductor package.

HISTORY OF RELATED ART

It is conventional in the electronic industry to encapsulate one or more semiconductor devices, such as integrated circuit dies, or chips, in a semiconductor package. These plastic packages protect a chip from environmental hazards, and provide a method of and apparatus for electrically and mechanically attaching the chip to an intended device. Recently, such semiconductor packages have included metal lead frames for supporting an integrated circuit chip which is bonded to a chip paddle region formed centrally therein. Bond wires which electrically connect pads on the integrated circuit chip to individual leads of the lead frame are then incorporated. A hard plastic encapsulating material, or encapsulant, which covers the bond wire, the integrated circuit chip and other components, forms the exterior of the package. A primary focus in this design is to provide the chip with adequate protection from the external environment in a reliable and effective manner.

As set forth above, the semiconductor package therein described incorporates a lead frame as the central supporting structure of such a package. A portion of the lead frame completely surrounded by the plastic encapsulant is internal to the package. Portions of the lead frame extend internally from the package and are then used to connect the package externally. More information relative to lead frame technology may

be found in Chapter 8 of the book Micro Electronics Packaging Handbook, (1989), edited by R. Tummala and E. Rymaszewski, incorporated by reference herein. This book is published by Van Nostrand Reinhold, 115 Fifth Avenue, New York, New York.

Once the integrated circuit chips have been produced and encapsulated in semiconductor packages described above, they may be used in a wide variety of electronic appliances. The variety of electronic devices utilizing semiconductor packages has grown dramatically in recent years. These devices include cellular phones, portable computers, etc. Each of these devices typically include a motherboard on which a significant number of such semiconductor packages are secured to provide multiple electronic functions. These electronic appliances are typically manufactured in reduced sizes and at reduced costs, which results in increased consumer demand. Accordingly, not only are semiconductor chips highly integrated, but also semiconductor packages are highly miniaturized with an increased level of package mounting density.

According to such miniaturization tendencies, semiconductor packages, which transmit electrical signals from semiconductor chips to motherboards and support the semiconductor chips on the motherboards, have been designed to have a small size. By way of example only, such semiconductor packages may have a size on the order of 1x1mm to 10x10 mm. Examples of such semiconductor packages are referred to as MLF (micro leadframe) type semiconductor packages and MLP (micro leadframe package) type semiconductor packages. Both MLF type semiconductor packages and MLP type semiconductor packages are generally manufactured in the same manner.

In further description of the above-described semiconductor package in Figure 1, the leadframe 10 is therein shown. The leadframe 10 comprises a plate type leadframe body 12 typically formed of metal and constructed with tie bars 14 extending from each of four corners surrounding a chip paddle 16 adapted for supporting an integrated circuit die also referred to as a "chip." The chip is not shown in this particular view for purposes of illustration and will be discussed below. Along and at a distance away from the perimeter of the chip paddle 16, a plurality of internal leads 18 are radially formed on the leadframe body 12. From the internal leads 18, external leads 22 are extended with their terminals being connected to the leadframe body 12. With connection to the leadframe body 12, dam bars 20 are provided between the internal leads 18 and the external leads 22 in order to prevent an encapsulation material from flowing over the external leads 22 upon encapsulating and to firmly fix the internal leads 18 and the external leads 22 to the

leadframe body 12. The dam bars 20, the external leads 22, predetermined areas of the tie bars 14, and the leadframe body 12 are all removed in a subsequent singlulation process. A large number of this type of leadframe 10 may be formed in a larger leadframe body 12 in a matrix form.

Along the periphery of the sides of the chip paddle 16 and at the ends of the internal leads directing to the chip paddle 16, there are formed half-etched parts which will be shown and discussed below.

Referring now to FIG. 2, there is shown a side elevational cross-sectional view, of a semiconductor package 100, taken along the line 2-2 of the leadframe illustrated in FIG. 1, for purposes of reference. It may be seen in this view that a half-etched part 15 is formed in the underneath side of the tie bar 14 along a predetermined area near the internal leads 18 and at the corner of the chip paddle 16. Generally, this and the other half-etched parts discussed herein are formed by a chemical etching process. This chemical etching process is usually conducted after a general design of the leadframe 10 is completed. As well known, areas in which the half-etched parts 15, such as tie bars 14, are to be formed remain uncoated with photoresist while the other areas are coated with photoresist before an etchant is applied to the leadframe 10. In the leadframe body 12 which is formed in a fabrication process later, chip paddle 16 and the internal leads are prevented from seceding from the leadframe body 12 horizontally or vertically or lengthening a passage through which moisture can permeate the chip, so as to restrain the moisture absorption to the semiconductor package. In addition, the half-etched parts 15 formed in the tie bars 14 interlock the chip paddle 16 and the tie bars 14 with the leadframe body 12. When mounting the semiconductor package 100 onto a motherboard, the half-etched parts 15 allow the internal leads 18 to be distant from the tie bars 14 to prevent the internal leads 18 and the tie bars 14 from forming a short circuit through the solder that is applied. This will be described in more detail below.

Still referring to FIG. 2, the semiconductor package 100, as shown herein, includes a semiconductor chip 102 mounted to the chip paddle 16. An encapsulation material 105 is used to coat the semiconductor chip 102 and leadframe 10 to form a semiconductor package body 128. It may also be seen that the encapsulation material 105 is also present within the recesses formed by the half-etched parts 15 formed in the tie bars 14. The semiconductor package 100, as shown herein, comprises the semiconductor chip 102 described above, having a plurality of bond pads 112 (shown in Fig. 3) disposed

around the perimeter of the upward surface of the semiconductor chip 102, and a chip paddle 16 which is bonded to the bottom surface of the semiconductor chip 102 via a conventional adhesive.

Referring now to FIG. 3, there is shown the semiconductor package 100 in a side-elevational cross-sectional view illustrating other aspects of the assembly thereof. In this particular cross-sectional view of the semiconductor package 100 taken along lines 3-3 of the semiconductor package 100 including the conductive wires extending from the semiconductor chip to be discussed below. The chip paddle 16 has a half-etched part 15 along the perimeter of its side. At the corners of the chip paddle 16 are formed tie bars 14 which externally extend and have half-etched parts 15. A plurality of internal leads 18, each of which has a half-etched part 15 at the end facing the chip paddle 16, are radially located along the perimeter of the chip paddle 16. Via conductive wires 116, the bond pads 112 of the semiconductor chip 102 are electrically connected to the internal leads 18. The semiconductor chip 102, the conductive wires 116, the chip paddle 16 and the internal leads 18 are encapsulated by an encapsulation material 105 to create a semiconductor package body 128 whereas the chip paddle 16, the internal leads 18 and the tie bars 14 are externally exposed in the downward direction of the semiconductor package body 128.

As mentioned above, the formation of the half etched parts 15 at the sides and ends of the internal leads 18 and the chip paddle 16 have advantages of preventing the internal leads 18 or the chip paddle 16 from seceding from the body horizontally or vertically as well as allowing the internal leads 18 and the tie bars 14 to be distant from the bottom surface of the semiconductor package body 128, so as to restrain the formation of a short circuit through solder upon mounting the package onto the motherboard. In addition, a half etched part 15 is formed in a predetermined area of the tie bars 14, interlocking with the semiconductor package body 128. Also, the half etched parts make the tie bars 14 spaced away from the internal leads 18 so as to prevent the formation of a circuit between the internal leads 18 and the tie bars 14 via a solder upon the mounting. This aspect may be seen in the footprint of semiconductor package 100 illustrated in FIG. 4, wherein the tie bar 14 is shown adjacent the internal leads 18 outwardly of chip paddle 16.

The leadframe described above is one that is formed by chemical etching. Such a leadframe is advantageous in that it can be fabricated at a small quantity in a short period

of time. Upon mass production, however, it is required that chemical solutions necessary for various chemical treatment processes are accurately controlled as to concentration, treatment period of time, flow rate, etc. In addition, its costs are high because of low productivity, or low Units Per Hour (UPH), and a large area for accommodating facilities.

Much effort is thus being made to adopt mechanical stamping techniques in the mass production of semiconductor packages. In the stamping techniques, the shape of the conventional half etched part can be formed by conducting on a predetermined area of the internal lead a coining process (a technique in which a predetermined area of a leadframe is strongly pressed to widely spread out the area in a ribbon shape and thus, the pressed area is thinner than other areas). However, these techniques are very difficult to apply for the conventional half etched part formed in the tie bars. For example, when a coining process is applied to the four tie bars 14 (Fig. 1), too much stress is placed on the tie bars 14 which support the chip paddle 16, making the chip paddle 16 bent, oblique or deformed. If the shape such as the conventional half etched part is absent in the tie bars 14, the tie bars 14 are externally exposed in the direction of the bottom surface of the semiconductor package. In this condition, the tie bars come into so close contact with the internal leads 18 that the internal leads 18 and the tie bars 14 may readily form a short circuit through the solder upon the soldering of the semiconductor package onto the motherboard.

BRIEF SUMMARY OF THE INVENTION

The present invention relates to semiconductor packages and leadframe assemblies of improved design and reliability. More particularly, one aspect of the present invention comprises a semiconductor package leadframe assembly wherein the leadframe includes a plate type frame body, a plurality of tie bars extending from the body to the central part of the leadframe, a chip paddle connected to the tie bars, and a plurality of internal leads radially formed at regular intervals along the perimeter of the chip paddle. The chip paddle is the type adapted to receive a semiconductor chip thereupon, and the tie bars are formed with reverse-down set portions formed in a predetermined area of each of the tie bars near the chip paddle. In this manner, this region of the tie bar is not exposed externally from the package body. Instead, the reverse-down set portion is present within the insulating body interlocking therewith,

bringing about a prevention effect to prevent the formation of a short circuit between an exposed tie bar region and the internal lead through solder upon the mounting of the semiconductor package onto a motherboard.

In another aspect of the present invention described above, the ends of the internal leads near the chip paddle are also made thinner by forming coining parts or portions at the ends of the internal leads.

In yet another aspect of the present invention, a semiconductor package comprises a semiconductor chip provided with a plurality of input and output pads; a chip paddle bonded to the bottom surface of the semiconductor chip via an adhesive; a plurality of tie bars externally extended from the corners of the chip paddle; a plurality of internal leads located at regular intervals along the perimeter of the chip paddle; conductive wires for electrically connecting the bond pads of the semiconductor chip to the internal leads; and a package body in which the semiconductor chip, the chip paddle, the tie bars, the internal leads and the conductive wires are encapsulated by an encapsulation material while the chip paddle, the tie bars and the internal leads are externally exposed at their bottom surfaces. Each tie bar includes a reverse-down set portion formed in a predetermined area thereof near the chip paddle to afford security of the tie bar within the encapsulation material in preventing the tie bar from being exposed to conductive portions of the semiconductor package that could cause a short therewith.

In yet a further aspect of the present invention, a method of securing a metal leadframe within a semiconductor package is set forth. The method includes the steps of forming a leadframe with a chip paddle generally centrally disposed therein, the chip paddle being connected to outer frame portions by oppositely disposed tie bars extending therebetween. An encapsulation material is provided for encasing a semiconductor chip disposed upon the chip paddle. The tie bars are also formed with reverse-down set portions between the chip paddle and the leadframe for preventing the tie bars from being exposed along the lower region of the semiconductor package. The semiconductor chip is secured to the chip paddle and electrically interconnected to select portions of the lead frame. The semiconductor chip and leadframe is then encapsulated with the reverse-down set portions of the tie bars encapsulated therein so as to prevent lateral movement of the tie bar relative to the encapsulant.

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BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the method and apparatus of the present invention may be obtained by reference to the following detailed description when taken in conjunction with the accompanying drawings wherein:

Fig. 1 is a top plan view of a conventional metal lead frame structure adapted for securement within a semiconductor package;

Fig. 2 is a side elevational, cross-sectional view of a semiconductor package utilizing the lead frame of Fig. 1 and taken along lines 2-2 thereof;

Fig. 3 is a side elevational, cross-sectional view of the semiconductor package of Fig. 2, taken along the lines 3-3 of the leadframe of Fig. 1 illustrating another aspect of the construction of prior art leadframe structures;

Fig. 4 is a bottom plan view of the semiconductor package of Fig. 2 illustrating the footprint thereof;

Fig. 5 is a cutaway perspective view of a semiconductor package incorporating the improved lead frame assembly of the present invention;

Fig. 6 is a top plan view of a metal leadframe structure constructed in accordance with the principles of the present invention and illustrating the reverse-down set portions of the tie bars thereof;

Fig. 7 is a side elevational, cross-sectional view of the tie bar and paddle assembly of Fig. 6 taken along the lines 7-7 thereof;

Fig. 8 is a side elevational, cross-sectional view of a semiconductor package utilizing the leadframe of Fig. 6 and taken along lines 8-8 thereof to illustrate the securement of a semiconductor chip therein and the reverse-down set regions of the tie bar adjacent thereto;

Fig. 9 is a side elevational cross-sectional view of the semiconductor package of Fig. 8 taken along lines 7-7 of the leadframe of Fig. 6;

Fig. 10 is a side elevational, cross-sectional view of the semiconductor package of Fig. 8 taken along lines 8-8 of the leadframe of Fig. 6;

Fig. 11 is a bottom plan view of the semiconductor package of Fig. 8 illustrating the footprint thereof; and

Fig. 12 is a flow diagram illustrating the steps of securing a lead frame within a semiconductor package in accordance with the principles of the present invention.

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DETAILED DESCRIPTION OF THE INVENTION

Referring now to Fig. 5, there is shown a cutaway perspective view of a semiconductor package 210 incorporating a leadframe 200 in accordance with one embodiment of the present invention, within the semiconductor package body 204. Shown by virtue of the cutaway portion of the semiconductor encapsulant forming semiconductor package body 204 is chip paddle 216 disposed adjacent a plurality of internal leads 218. The upper side of each one of the plurality of internal leads 218 may, but does not necessarily have to be, electroplated with an electrically conductive material such as, but not limited to, gold or silver, to enhance electrical conductivity. Conductive wires 201 extend between a semiconductor chip 202 and the internal leads 218. A tie bar 214 is also shown to be formed with a reverse-down set part 215 located adjacent the chip paddle 216. Owing to the presence of the reverse-down set part 215, the tie bar 214, which is exposed from beneath the package body as described below, is further spaced from the internal leads 218 so that the possibilities of short circuits between the tie bar 214 and the internal leads 218 are reduced. Such a short can be formed by solder when mounting the semiconductor package 210 on a motherboard or the like.

Referring now to Fig. 6, there is shown a top plan view of the leadframe 200 constructed in accordance with an embodiment of the present invention. The leadframe 200 is constructed with a plate type leadframe body 212 provided with tie bars 214 as shown and internally extending from each of the four (or two) corners. At least two tie bars 214 are typically used in metal leadframe fabrication, and the present invention is directed to any metal leadframe assembly having tie bars constructed therein. Being in contact with the tie bars 214, a roughly square chip paddle 216 is provided. Along and at a distance away from the perimeter of the chip paddle 216, a plurality of internal leads 218 are radially formed on the leadframe body 212. From the internal leads 218, external leads 213 are extended with their terminals being connected to the leadframe body 212. With connection to the leadframe body 212, dam bars 209 are provided between the internal leads 218 and the external leads 213 in order to prevent an encapsulation material from flowing over the external leads 213 upon encapsulating and to firmly fix the internal leads 218 and the external leads 213 to the leadframe body 212.

Referring now to Figs. 5, 7 and 8 in combination, an embodiment of the present invention is featured in that a predetermined area of each tie bar 214 which extends

externally from a corner of the chip paddle 216, is bent to a predetermined length in an upward direction to form a reverse-down set part 215 (Fig. 7). As shown in detail in Fig. 5, the reverse-down set part 215 is bent more upwardly than the plane of the chip paddle 216, the internal lead 218 and the external lead form together. This reverse-down set part 215 is formed by mechanical stamping. That is, predetermined areas of the tie bars 214 (in the vicinity of the square corners of the chip paddle 216) are punched to form such a reverse-down set part 215.

As seen in Figs. 5 and 8 inside the frame body, coining parts 219 are formed at the internal leads' ends near the perimeter of the chip paddle 216, so that the internal leads 218 are made thinner at their ends. The coining parts 219 may also be formed by a half etching process as in the prior art discussed above.

As shown most clearly in Fig. 5, the reverse-down set part 215 of the tie bar 214 is located inside and thus, is later interlocked with a semiconductor package body 204. In result, owing to the presence of the reverse-down set part 215, the tie bar 214, which is exposed from the semiconductor package body 128, is further spaced from the internal lead 218, so that a short circuit between the tie bar 214 and the internal lead 218 is reduced. Such shorting can be produced by the solder when mounting the semiconductor package on the motherboard. This will be in more detail described below.

With reference to Figs. 9, 10 and 11 in combination, there is shown the semiconductor package 210 using the leadframe 200 in cross sectional views and in a bottom view. As shown therein, the semiconductor package 210 comprises the semiconductor chip 202 provided with a plurality of bond pads 234, and the chip paddle 216 bonded to the bottom surface of the semiconductor chip 202 via an adhesive. At the corners of the chip paddle 216 are formed tie bars 214 which externally extend. A plurality of internal leads 218 are radially located at a distance away from and along the perimeter of the chip paddle 216. Via conductive wires 201, the bond pads 234 of the semiconductor chip 202 are electrically connected to the internal leads 218. An upper surface of each one of internal leads 218 may, but does not necessarily have to be, electroplated with for example, silver or gold, to enhance electrical conductivity. The semiconductor chip 202, the conductive wires 201, the chip paddle 216 and the internal leads 218 are encapsulated by an encapsulation material to create a semiconductor package body 204 whereas the chip paddle 216, the internal leads 218 and the tie bars 214 are externally exposed in the downward direction of the semiconductor package body

128. The encapsulation material may be thermoplastics or thermoset resins, with the thermoset resins including, but not limited to, silicones, phenolics, and epoxies. The exposed portions of chip paddle 216, internal leads 218, and tie bars 214 may, but do not necessarily have to be, electroplated with a corrosion-minimizing material such as, for example, tin lead, tin, gold, nickel palidium, tin bismuth, or similar materials known in the art.

A feature of the various embodiments of the present invention resides in that a predetermined area of each tie bar 214, which extends externally from a corner of the chip paddle 216, is bent to a predetermined length in the upward direction to form a reverse-down set part 215. Thus, the reverse-down set part 215 is located inside and spontaneously interlocks with the semiconductor package body 204. Additionally, the area of the tie bar 214, which is exposed externally in the downward direction of the semiconductor package body 204, is reduced. In result, the tie bars are further spaced away from neighboring internal leads 218.

When the semiconductor package 210 is mounted on a motherboard, solder is plated on the bottom surfaces of the internal leads 218 and tie bars 214, which are externally exposed in the downward direction of the semiconductor package body 204. The presence of the reverse-down set part has the effect of making smaller the probability that the tie bars 214 are connected to the internal leads 218 through the solder.

In addition, coining parts 219 are formed at the ends of internal leads 218 near the chip paddle 216, being inside the semiconductor package body 204. The coining parts 219 are thinner than the remaining areas of internal leads 218, located inside the semiconductor package body 204. Thus, the internal leads 218 interlock with the semiconductor package body 204 and are prevented from seceding from the semiconductor package body 204 horizontally and vertically by virtue of the coining parts 219.

Referring now to Fig. 12, there is shown a flow diagram illustrating the method of securing a leadframe within a semiconductor package of the type wherein a semiconductor chip is secured thereon. The method comprises the steps of providing a leadframe having a chip paddle and a frame region extending around the paddle. The chip paddle is connected to the frame by oppositely disposed tie bars extending therebetween. Either two or four tie bars can be utilized, as set forth above. The next step provides an encapsulant for encasing a semiconductor chip disposed upon and

secured to the chip paddle. The tie bars are formed with reverse-down set portions between the paddle and the frame for preventing the tie bar from being exposed from a lower region of the semiconductor package. A semiconductor chip is then mounted upon and secured to the paddle and is electrically interconnected to select portions of the leadframe. The chip paddle and lead frame assembly is then encapsulated with the semiconductor chip secured therein, and the reverse-down set portions of the tie bars encapsulated therein so as to prevent lateral movement of the tie bar relative to the encapsulant. In a final step, the semiconductor package is singulated from the outer portions of the leadframe as set forth and described in one or more of the copending patent applications referenced and incorporated herein by reference.

The present invention has been described in an illustrative manner, and it is to be understood that the terminology used is intended to be in the nature of description rather than of limitation. Many modifications and variations of the present invention are possible in light of the above teachings. Specifically, the coining can be achieved mechanically, chemically, or a combination thereof, while the material of which the leadframe is made can be a good electrical conductor such as copper, aluminum, or other metals and alloys. The lead frame may also be formed of one material and plated with another material such as, but not limited to, for example gold or silver.

In the leadframe and semiconductor package structure of the present invention, as described hereinbefore, a reverse-down set part is formed in the tie bar supporting the chip paddle by stamping. Each of the reverse-down set parts are located inside and thus, interlock with the package body. In addition, owing to the presence of the reverse-down set part, the tie bar, which is exposed from the package body, is further spaced from the internal lead, so that a short circuit between the tie bar and the internal lead is greatly restrained from being formed by the solder when mounting the semiconductor package on the motherboard. In addition, a coining part is provided to the internal leads, interlocking them with the body spontaneously.

Consequently, the present invention takes advantage of a stamping technique with a reduced probability of forming a short circuit between the internal leads and the tie bars via solder and thus, produces leadframes and semiconductor packages on a large scale.

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The following applications are all being filed on the same date as the present application and all are incorporated by reference as if wholly rewritten entirely herein, including any additional matter incorporated by reference therein:

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Attorney Docket No.	Title of Application	First Named Inventor
09/687,787	Improved Thin and Heat Radiant Semiconductor Package and Method for Manufacturing	Jae Hun Ku
09/687,331	Lead Frame for Semiconductor Package and Mold for Molding the Same	Young Suk Chung
09/687,532	Method for Making a Semiconductor Package Having Improved Defect Testing and Increased Production Yield	Tae Heon Lee
09/687,876	Near Chip Size Semiconductor Package	Sean Timothy Crowley
09/687,536	End Grid Array Semiconductor Package	Jae Hun Ku
09/687,048	Leadframe and Semiconductor Package with Improved Solder Joint Strength	Tae Heon Lee
09/687,585	Semiconductor Package Having Reduced Thickness	Tae Heon Lee
09/687,049	Improved Method for Making Semiconductor Packages	Young Suk Chung

It is thus believed that the operation and construction of the present invention will be apparent from the foregoing description of the preferred exemplary embodiments. It will be obvious to a person of ordinary skill in the art that various changes and modifications may be made herein without departing from the spirit and the scope of the invention.

Claims:

1. A semiconductor package comprising:

a quadrangular chip paddle defining opposed top and bottom surfaces and multiple corners;

at least one tie bar attached to the chip paddle and extending from a respective one of the corners thereof, the tie bar including:

an inner portion extending to a respective one of the corners of the chip paddle and defining opposed top and bottom inner portion surfaces; an outer portion defining opposed top and bottom outer portion surfaces; and

a downset portion extending between the inner and outer portions and defining opposed top and bottom downset surfaces;

the top outer portion surface of the tie bar extending in generally co-planar relation to the top surface of the chip paddle, with the top downset surface and the top surface of the chip paddle extending along respective ones of a spaced, generally parallel pair of planes;

a plurality of internal leads extending at least partially about the chip paddle in spaced relation thereto, each of the internal leads defining opposed top and bottom surfaces;

a semiconductor chip mounted to the top surface of the chip paddle and electrically connected to at least one of the internal leads; and

a package body at least partially encapsulating the semiconductor chip, the chip paddle, the tie bar, and the internal leads such that at least a portion of the bottom surface of each of the internal leads and the bottom outer portion surface of the tie bar are exposed in the package body.

2. The semiconductor package of Claim 1 further comprising a plurality of conductive wires electrically connecting the semiconductor chip to respective ones of the internal leads, the conductive wires being encapsulated by the package body.

3. The semiconductor package of Claim 1 wherein the bottom downset surface of the downset portion of the tie bar and the top surface of the chip paddle extend in generally co-planar relation to each other.

4. The semiconductor package of Claim 1 wherein the bottom surface of the chip paddle is exposed in the package body.

5. The semiconductor package of Claim 4 wherein the bottom surface of the chip paddle, the bottom surfaces of the internal leads, and the bottom outer portion surface of the outer portion of the tie bar extend in generally co-planar relation to each other.

6. The semiconductor package of Claim 1 wherein each of the internal leads defines an inner end disposed proximate to the chip paddle and is configured to include a region of reduced thickness which extends to the inner end thereof.

7. The semiconductor package of Claim 1 comprising a plurality of tie bars which extend to respective ones of the corners of the chip paddle.

8. A leadframe for use in the semiconductor package, the leadframe comprising:
a quadrangular chip paddle defining opposed top and bottom surfaces and multiple corners;
at least one tie bar attached to the chip paddle and extending from a respective one of the corners thereof, the tie bar including:
an inner portion extending to a respective one of the corners of the chip paddle and defining opposed top and bottom inner portion surfaces; an outer portion defining opposed top and bottom outer portion surfaces; and
a downset portion extending between the inner and outer portions and defining opposed top and bottom downset surfaces;

the top outer portion surface of the tie bar extending in generally co-planar relation to the top surface of the chip paddle, with the top downset surface and the top surface of the chip paddle extending along respective ones of the spaced, generally parallel pair of planes;

a plurality of internal leads extending at least partially about the chip paddle in spaced relation thereto, each of the internal leads defining opposed top and bottom surfaces.

9. The leadframe of Claim 8 further comprising a frame body, the internal leads being attached to and extending inwardly from the frame body toward the chip paddle, with the outer portion of the tie bar extending and being attached to the frame body.

10. The leadframe of Claim 8 wherein the bottom downset surface of the downset portion of the tie bar and the top surface of the chip paddle extend in generally co-planar relation to each other.

11. The leadframe of Claim 8 wherein the bottom surface of the chip paddle, the bottom surfaces of the internal leads, and the bottom outer portion surface of the outer portion of the tie bar extend in generally co-planar relation to each other.

12. The leadframe of Claim 8 wherein each of the internal leads defines an inner end disposed proximate to the chip paddle and is configured to include a region of reduced thickness which extends to the inner end thereof.

13. The leadframe of Claim 8 comprising a plurality of tie bars which extend to respective ones of the corners of the chip paddle.

14. A method of fabricating a semiconductor package, comprising the steps of:

a) providing a leadframe which includes:

a quadrangular chip paddle defining opposed top and bottom surfaces and multiple corners, a plurality of internal leads extending at least partially about the chip paddle in spaced relation thereto, each of the internal leads defining opposed top and bottom surfaces, and at least one tie bar attached to the chip paddle and extending from a respective one of the corners thereof, the tie bar including an inner portion extending to a respective one of the corners of the chip paddle and defining opposed top and bottom inner portion surfaces, an outer portion defining opposed top and bottom outer portion surfaces, and a downset portion extending between the inner and outer portions and defining opposed top and bottom downset surfaces, the top outer portion surface extending in generally co-planar relation to the top surface of the chip paddle, with the top downset surface and the top surface of the chip paddle extending along respective ones of the spaced, generally parallel pair of planes;

b) mounting a semiconductor chip to the top surface of the chip paddle;

c) electrically connecting the semiconductor chip to at least one of the internal leads; and

d) at least partially encapsulating the semiconductor chip, the chip paddle, the tie bar, and the internal leads with the package body such that at least a portion of the bottom surface of each of the internal leads and the bottom outer portion surface of the tie bar are exposed in the package body.

15. The method of Claim 14 wherein step (c) comprises electrically connecting the semiconductor chip to respective ones of the internal leads via a plurality of conductive wires.

16. The method of Claim 14 wherein step (d) comprises forming the package body such that the bottom surface of the chip paddle is exposed therein.

17. The method of Claim 14 wherein step (a) comprises forming the leadframe such that the bottom downset surface of the downset portion of the tie bar and the top surface of the chip paddle extend in generally co-planar relation to each other.

18. The method of Claim 14 wherein step (a) comprises forming the leadframe such that the bottom surface of the chip paddle, the bottom surfaces of the internal leads, and the bottom outer portion surface of the outer portion of the tie bar extend in generally co-planar relation to each other.

19. The method of Claim 14 wherein step (a) comprises forming each of the internal leads to define an inner end disposed proximate to the chip paddle and to include a region of reduced thickness which extends to the inner end thereof.

20. The method of Claim 14 wherein step (a) comprises forming the leadframe to include a plurality of tie bars which extend to respective ones of the corners of the chip paddle.

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ABSTRACT

A semiconductor package and the leadframe therefor having a reverse-down set part formed in the tie bar supporting the chip paddle. The reverse-down set part of the tie bar may be formed by a mechanical stamping process in such a way that it is present within the insulating body, interlocking therewith. This feature also facilitates the prevention of a short circuit between the tie bar that is exposed externally from the package body and the exposed internal lead through solder upon the mounting of a semiconductor package onto a motherboard.

FIGURE 5