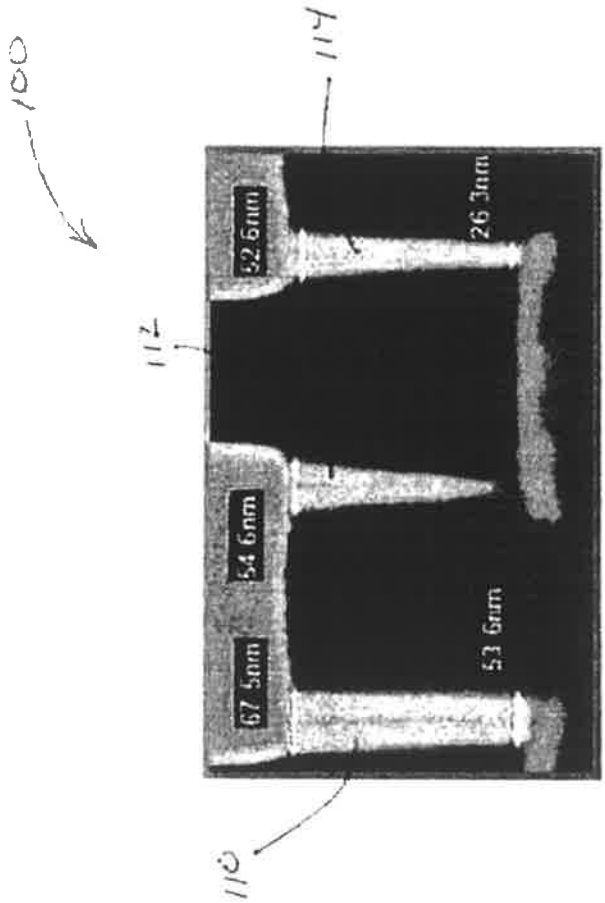


Figure 1

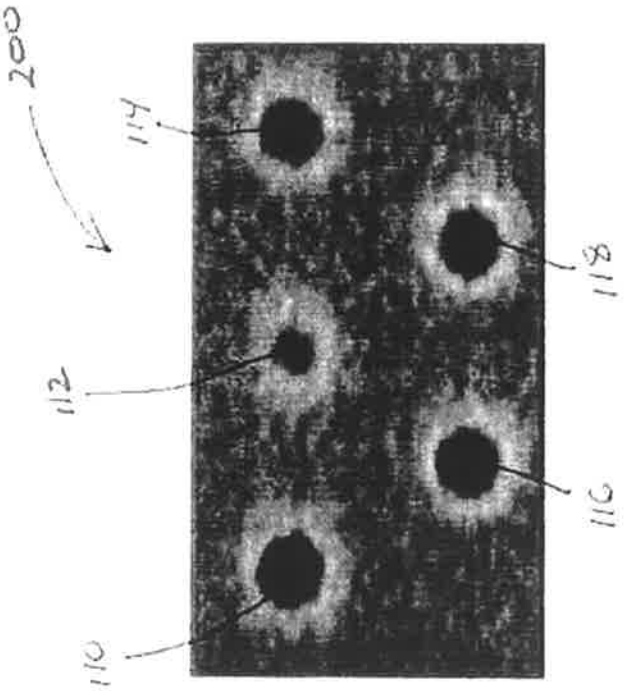


Figure 2

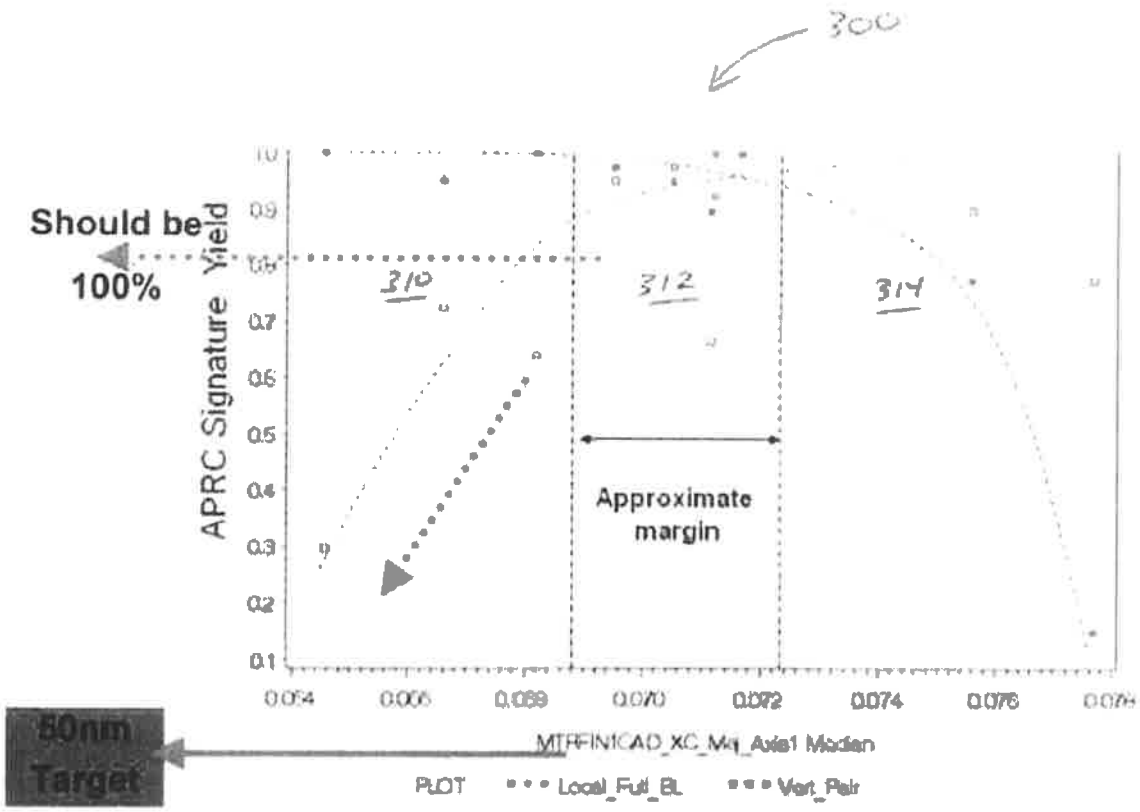

300
Should be
100%
Yield
APRC Signature
310
312
314
Approximate
margin
50nm
Target
MTFINCAD_XC_Mq_Axis1 Median
PLOT
Local_Full_BL
Vert_Pair

Figure 3

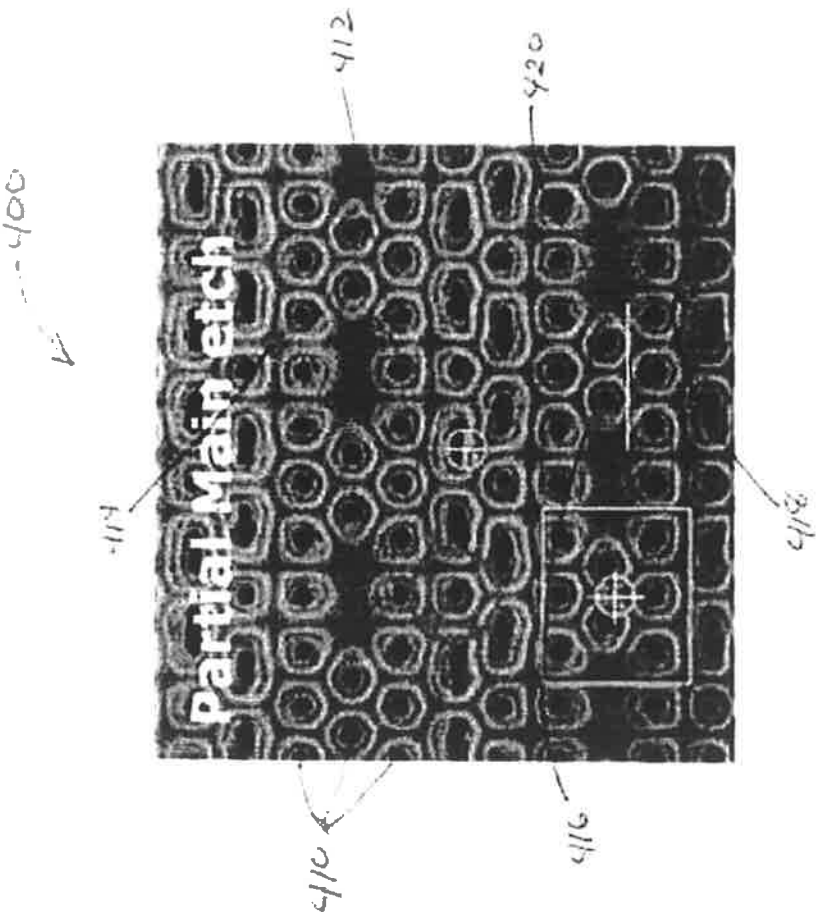


Figure 4

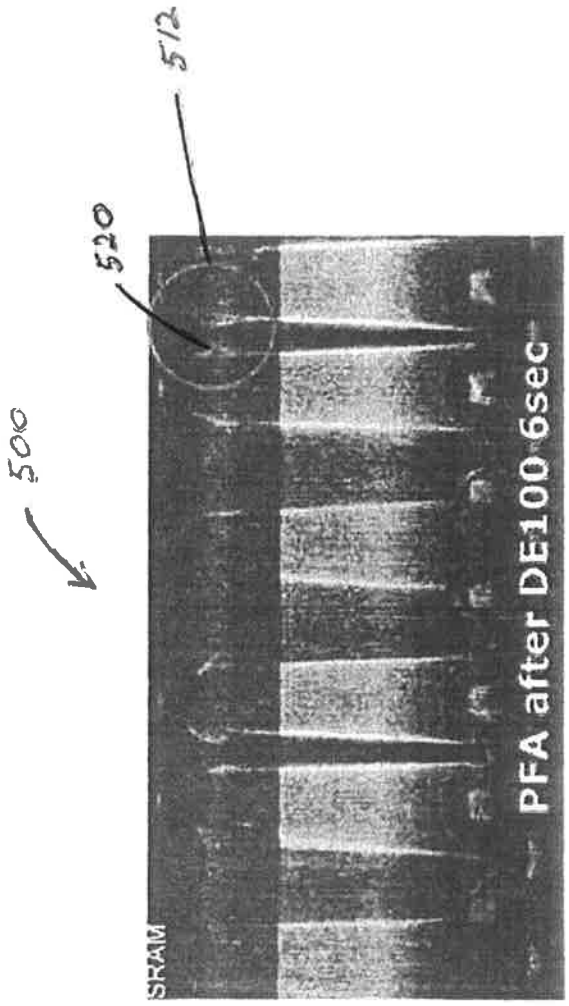


Figure 5

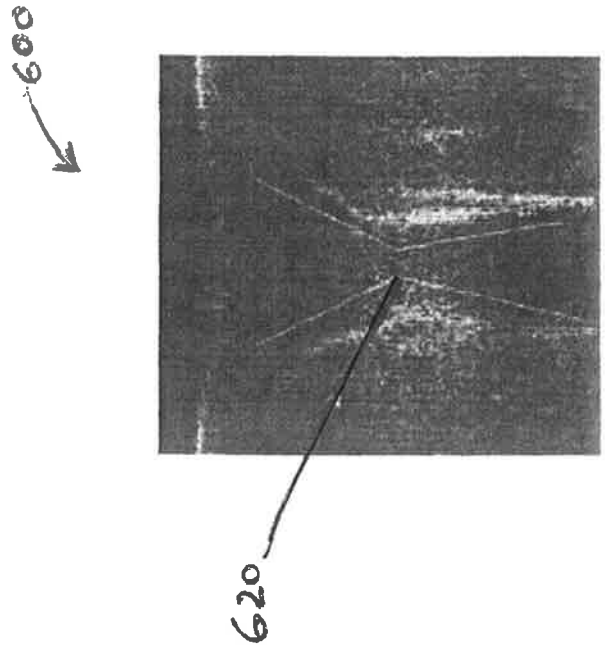


Figure 6

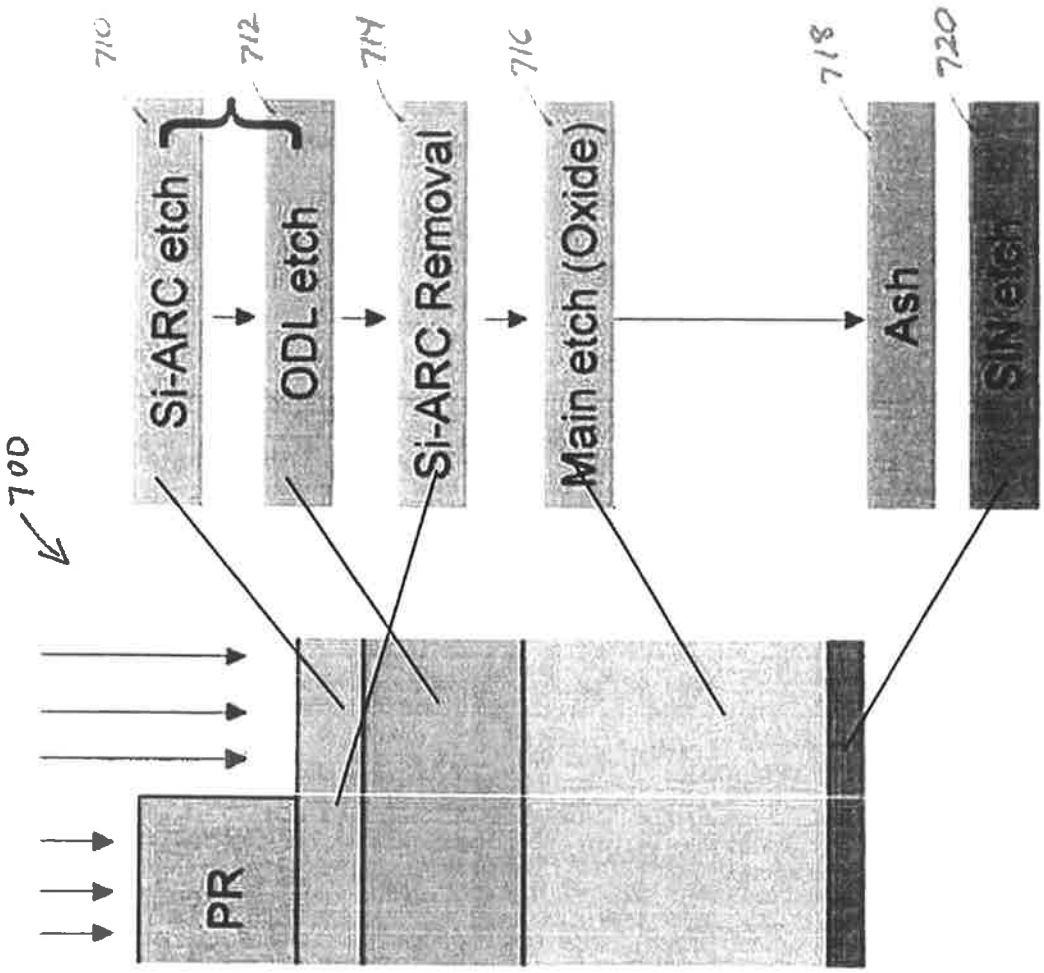

700
710
712
714
716
718
720
Si-ARC etch
ODL etch
Si-ARC Removal
Main etch (Oxide)
Ash
SiN etch
PR

Figure 7

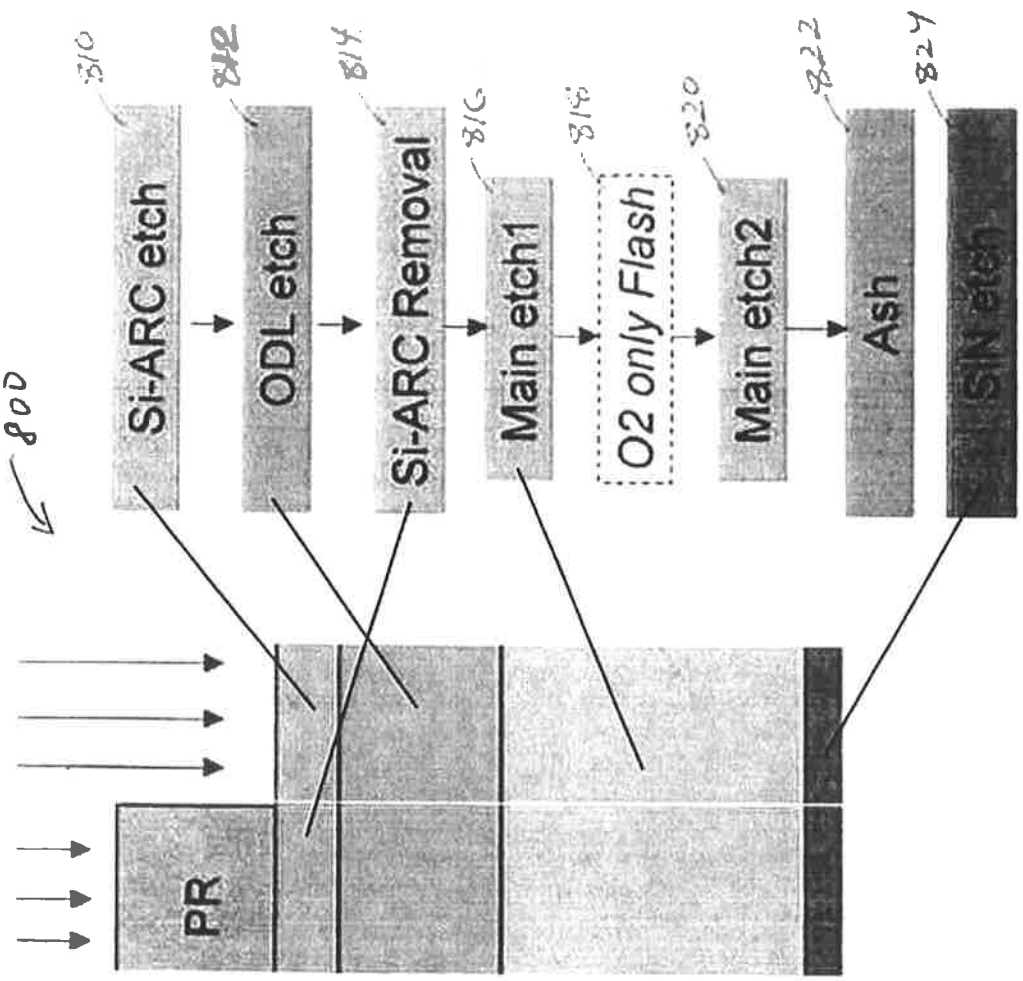

800
Si-ARC etch
ODL etch
Si-ARC Removal
Main etch1
O2 only Flash
Main etch2
Ash
SiN etch
PR

Figure 8

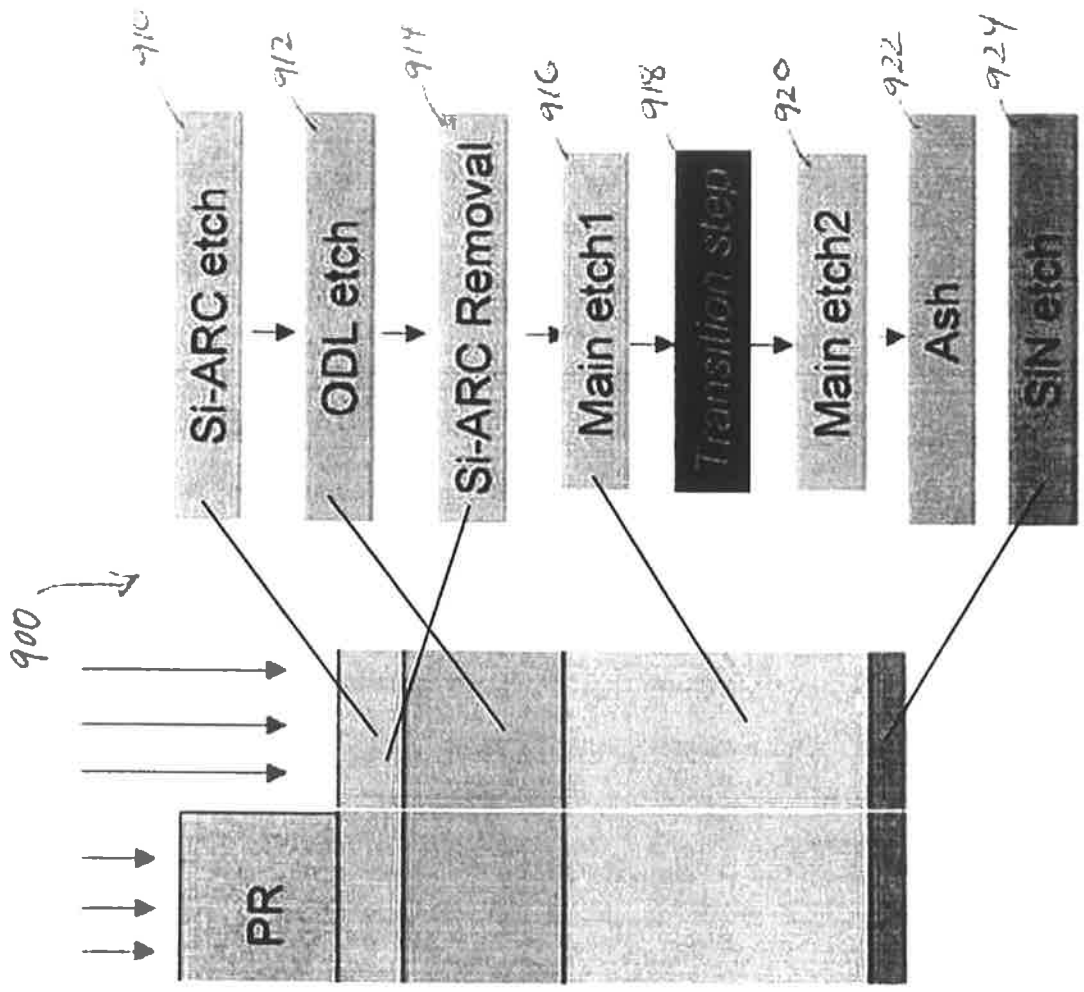

900
PR
Si-ARC etch
ODL etch
Si-ARC Removal
Main etch1
Transition step
Main etch2
Ash
SiN etch

Figure 9

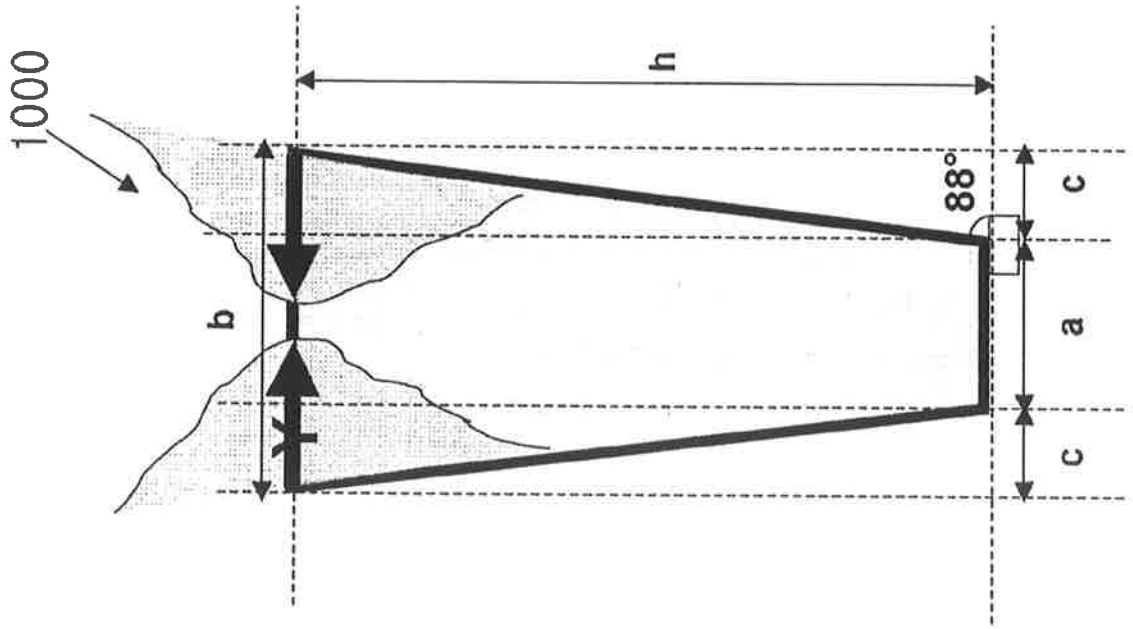


Figure 10

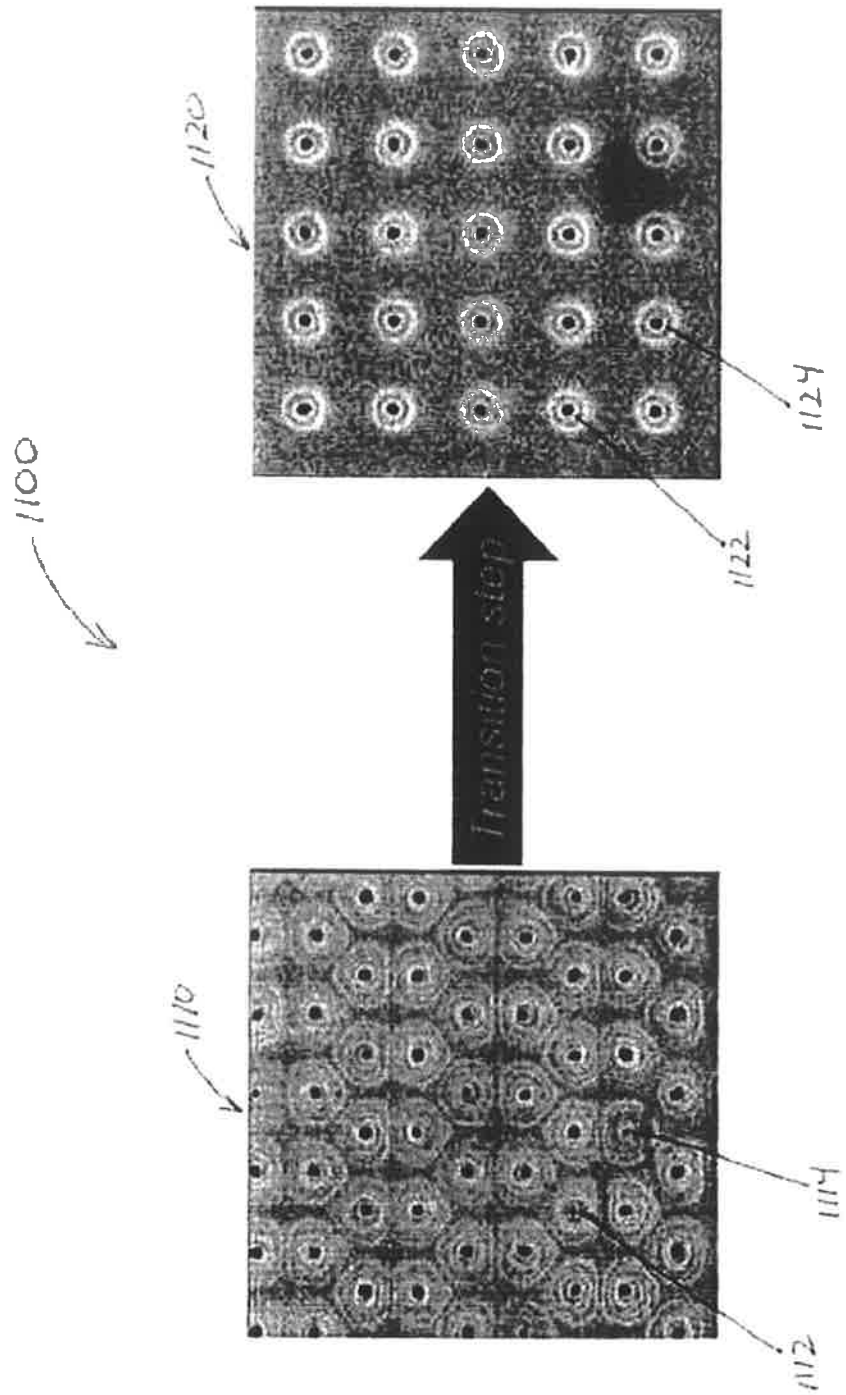


Figure 11

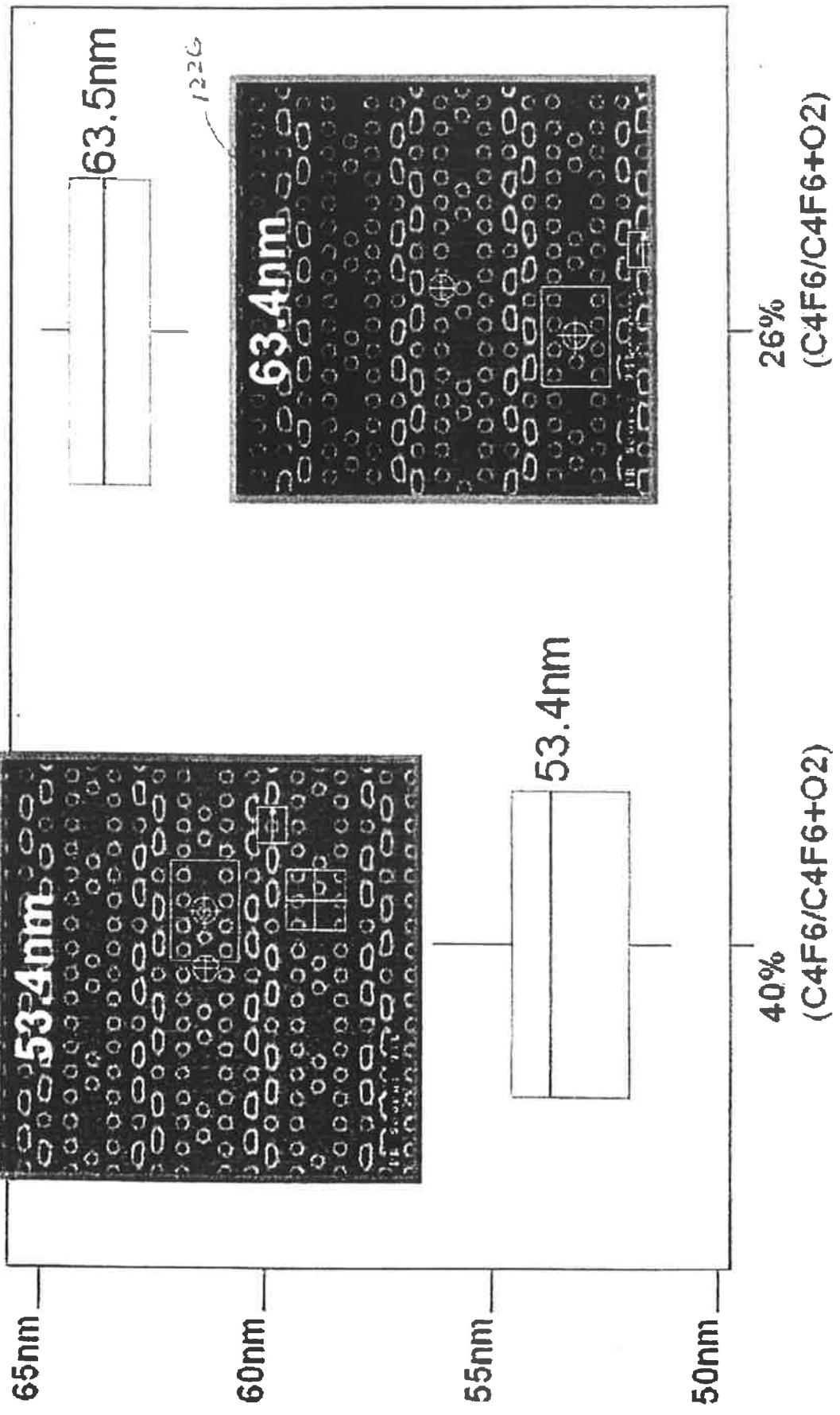

1200
1240
1226
63.5nm
63.4nm
53.4nm
53.4nm
26%
(C4F6/C4F6+O2)
40%
(C4F6/C4F6+O2)
65nm
60nm
55nm
50nm

Figure 12

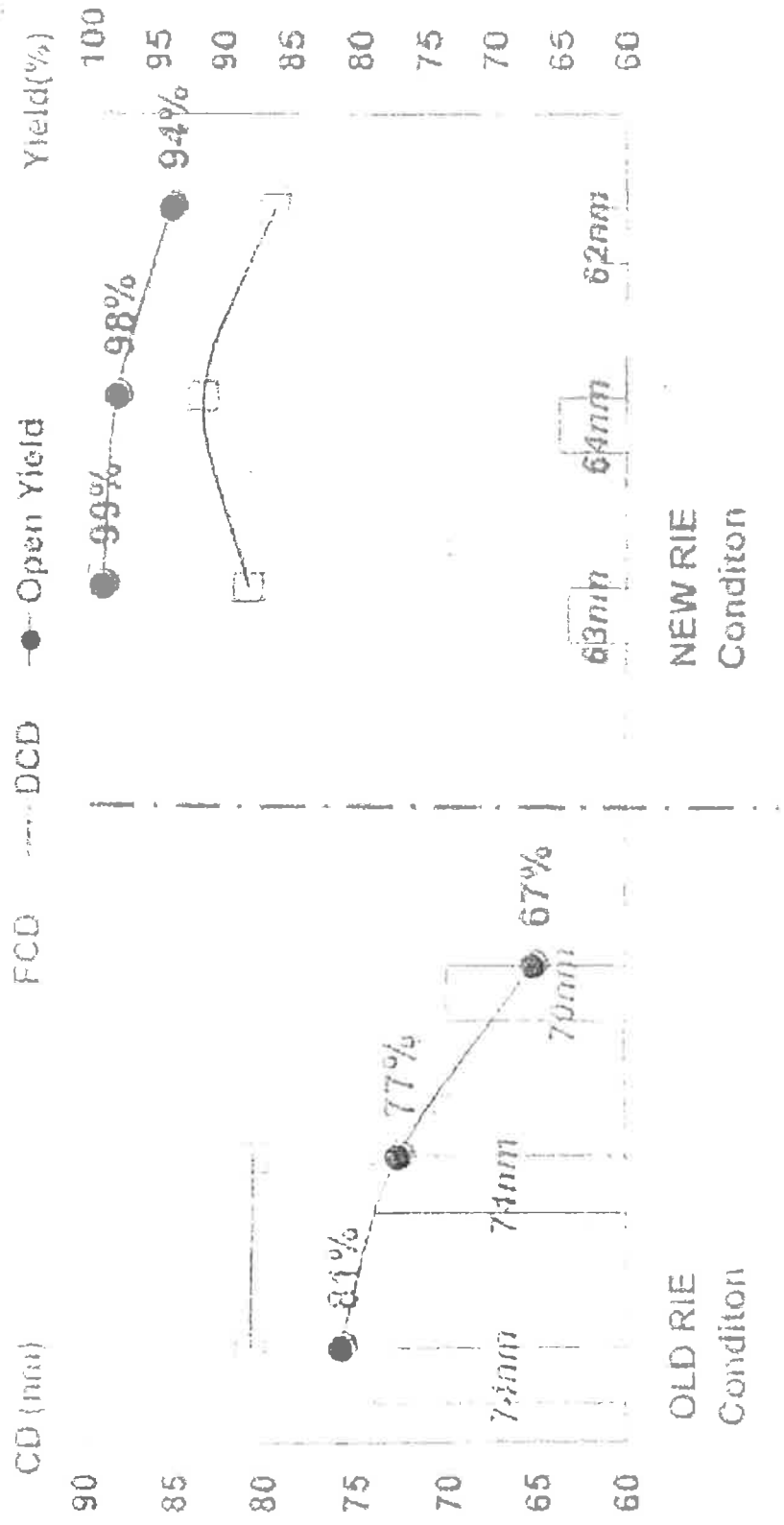

1300
FCD
DCD
Open Yield
Yield(%)
CD (nm)
99%
98%
94%
81%
77%
67%
74nm
70nm
68nm
64nm
62nm
OLD RIE
Condition
NEW RIE
Conditon

Figure 13