

ABSTRACT

A control means 101 is responsive to the shape of data inputted by inputting means 32 to control designating means 102 to switch addresses of a memory 18 designated for accessing means 103a to 103d. The designating means 102 designates to the accessing means 103a to 103d addresses of the memory 18 to be accessed under control by the control means 101. The accessing means 103a to 103d simultaneously access plural addresses of the memory 18 designated by the designating means 102. By switching simultaneously accessible addresses for accessing the memory with a minimum number of accessing operations for performing pre-set data processing operations, data processing may be improved in efficiency.
