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PATENT SPECIFICATION

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COMPLETE SPECIFICATION

DRAWINGS ATTACHED

Semiconductor Networks including F ield-Effect and Junction Transistors

We, TEXAS INSTRUMENTS INCORPORATED, of 13500 North Central Expressway, Dallas, Texas, United States of America, a corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor networks including field-effect and junction transistors and is divided from our co-pending patent application No. 15723/61 (Serial No. 983,252).

The present invention is a semiconductor network comprising a semiconductor wafer having therein or thereon a field-effect transistor including a source, drain and gate and a junction transistor including a collector-base and base-emitter junction, and wherein said source, said drain, said gate, said base-emitter junction and said collector-base junction are all adjacent one and the same major wafer face.

Embodiment of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:—

Fig. 1 shows a unipolar field-effect transistor;

Fig. 2*a* illustrates a semiconductor network according to the present invention;

Figs. 2*b* and 2*c* show the top and cross-sectional views illustrating another semiconductor network according to the present invention;

Fig. 3 shows the circuit diagram of the Fig. 2*a* embodiment;

Fig. 4 shows a characteristic of the Fig. 2*a* embodiment;

Fig. 5 shows a bistable circuit exemplifying the switching properties of the Fig. 2*a* embodiment;

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Fig. 6 is a schematic illustration of a ring counter circuit;

Fig. 7 is the plan view of another semiconductor network according to the present invention providing the circuitry for a single stage of the ring counter circuit;

Fig. 8 is a cross-sectional view through Fig. 7; and

Fig. 9 illustrates a relaxation oscillator circuit.

The semiconductor network of the present invention includes a field-effect and junction transistor which is a modification of a unipolar field-effect transistor such as that illustrated in Fig. 1. The unipolar field-effect transistor in Fig. 1 comprises a block 11 of N-type material on which there is a diffused layer 12 of P-type material forming a PN junction 13 with the N-type material of the block 11. In the middle of the layer 12 of P-type material is a diffused section 14 of N-type material which extends down into the layer 12 of P-type material, dividing it into two main parts 12*a* and 12*b* connected by a narrow conducting channel 15 of P-type material bounded by the N-type material of block 11 and the section 14 of N-type material. The section 14 of N-type material makes a PN junction 16 with the layer 12 of P-type material. An ohmic connection is made to one of the main parts 12*a* of the layer 12 of P-type material. This connection provides the source 17 of the field-effect transistor. An ohmic connection is made to the other main parts 12*b* of the layer 12 of P-type material to provide the drain 18 of the field-effect transistor. Ohmic connections are also made to the section 14 and to the block 11 on the side opposite to the layer 12, which connections are connected together to form the gate 19 of the field-effect transistor.

The width of the channel 15 between the boundaries provided by the PN junctions 13

and 16 is important in determining the characteristics of the field-effect transistor. This width is controlled and determined by the depths of diffusion of the layer 12 and the section 14. With this structure, the conductance in the channel 15 of P-type material btween the source 17 and the drain 18 is controlled by the voltage applied to the gate 19.

Fig. 2*a* illustrates one embodiment of the present invention. As shown in Fig. 2*a*, the semiconductor network, like the unipolar field-effect transistor illustrated in Fig. 1, comprises a block or first region 11 of N-type material on which there is a diffused layer or second region 12 of P-type material. In the layer 12 is a diffused section or third region 14 of N-type material. The N-type material of the block 11 forms a PN junction 13 with the layer 12 of P-type material. The section 14 of N-type material also forms a PN junction 16 with the layer 12 of P-type material. As in the unipolar transistor, the section 14 extends into the layer 12, dividing it into two major parts 12*a* and 12*b* connected by a narrow channel 15 of P-type material. An ohmic contact is made connecting a first terminal electrode with the part 12*a* of the layer 12 to form the source 17 of the field-effect transistor. Ohmic contacts are made to the section 14 and to the block 11 on the side opposite the layer 12, which contacts are connected together to form a third terminal electrode 19. The electrode 19 in Fig. 2*a* is structurally the same as the gate 19 in the unipolar field-effect transistor Fig. 1. In the Fig. 2*a* embodiment, however, this electrode is referred to as the collector. As can be seen in Fig. 2*a*, the semiconductor network differs from the unipolar field-effect transistor in that a diffused section 20 or fourth region of N-type material is provided in the part 12*b* of the layer 12 of P-type material. This section 20 of N-type material extends down into the layer 12 of P-type material not quite as far as the junction 13. An ohmic contact is made connecting a second terminal electrode to the section 20 forming the emitter 21 of the junction transistor. The section 20 forms a PN junction 22 with the P-type material of the layer 12. The PN junctions 22 and 13 will coact to provide junction transistor action wherein 22 and 13 are the emitter-base and base-collector junctions, and, as a result, the semiconductor network embodies a junction transistor and a field-effect transistor connected together in a circuit, which is shown in Fig. 3.

In Fig. 2*a*, 11, 12 and 20 act as the collector, base and emitter of a junction transistor and 14, 15, 12*a* and 12*b* act as the gate, channel, source and drain of a field-effect transistor. It should be noted that the collector-base and base-emitter junctions and the source, drain and gate are all adjacent the top surface or major face of the wafer.

Figs. 2*b* and 2*c* show a particular physical embodiment of the semiconductor network of Fig. 2*a* which has been found to be especially desirable. A specific example of a method of producing this structure will now be described. A wafer 110 of silicon, forming a first region, of a resistivity of 7.5 ohm-centimetres is used as the starting material. Each side of the wafer is lapped to achieve wafer thickness of 10 mils. The upper side of the wafer is then optically polished. After the polishing operation, the wafer is placed in an open tube, and steam of a temperature of approximately 1200°C, is allowed to pass over the wafer. This operation causes a thin oxide film to form on all surfaces of the wafer. The wafer is then subjected to diffusion from a gallium trioxide source in the presence of dry oxygen to form a layer of P-type material approximately 0.7 mils thick in the surface of the wafer. Using photo-resist techniques, the oxide film is then selectively removed from concentric circular portions of the wafer surface. After the selective removal of the oxide film, the wafer is subjected to a second diffusion cycle in which phosphorus is diffused to a depth of approximately 0.3 mils from a phosphorus pentoxide source in the presence of dry nitrogen. The resulting thin layer of P-type material is then removed from the bottom and sides of the wafer, leaving a layer 112 or second region of P-type material on the surface of the wafer, making a PN junction 126 with the N-type material of the wafer. The second step of diffusion from the source of phosphorus pentoxide causes concentric circular sections 114, forming a third region, and 116, forming a fourth region, of N-type material to be formed in the layer 112 making PN junctions with the P-type material of the layer 112. Ohmic contacts 120 and 122 connecting the second and third terminal electrodes to the sections 116 and 114, respectively, are provided. An ohmic contact 124 connecting the first terminal electrode to the layer 112 is provided at the centre about which the circular sections 114 and 116 are positioned. An ohmic contact 118 is provided connecting the third terminal electrode to the bottom of the wafer 110. The contacts 118, 120, 122 and 124 are of aluminium, and are formed by evaporation and sintering techniques. The wafer is then masked with an etch-resistant material such as wax, and the wafer etched in an acid solution to achieve the mesa configuration shown in Fig. 2*c*. The resulting device is a semiconductor network which is equivalent to the device in Fig. 2*a*.

In the device in Figs. 2*b* and 2*c*, the contacts 124 and 120 correspond to the source 17 and the emitter 21, respectively, in Fig.

2a. The contacts 122 and 118 in Figs. 2b and 2c will be connected together and 118 corresponds to the collector 19 in Fig. 2a. The sections 114 and 116 in Figs. 2b and 2c correspond to the sections 14 and 20, respectively, in Fig. 2a. In the completed device, the collector-base junction 126 defines an enclosed area at the top surface or top major face of the wafer 110; and the base-emitter junction (between regions 116 and 112) defines an enclosed area at said top major face which enclosed area is surrounded by the first-mentioned enclosed area.

It is to be noted that, in some instances, it may be desirable that the sections 114 and 116 be diffused to different depths or have different impurity concentrations therein. In such instances, it will be necessary to form the sections by different diffusion cycles. In the embodiment described, however, only one diffusion cycle is used to form both sections 114 and 116.

The circuit in Fig. 3 is the circuit diagram of the Fig. 2a embodiment. As shown in Fig. 3, the circuit comprises a unipolar field-effect transistor 23 and a junction transistor 25, which in the specific embodiment of the present invention is an NPN transistor. In Fig. 3, the source of the unipolar field-effect transistor 23 is designated by the reference number 26, the gate by the reference number 28, and the drain by the reference number 27. The unipolar field-effect transistor 23 has its drain 27 connected directly to the base of the junction transistor 25. The gate 28 of the field-effect transistor 23 is connected directly to the collector of the junction transistor 25. The source of the field-effect transistor in Fig. 2a corresponds in its circuit diagram to the source 26 of the unipolar field-effect transistor 23. The collector of the junction transistor in Fig. 2a corresponds in its circuit diagram to the collector of the junction transistor 25. The emitter of the junction transistor in Fig. 2a corresponds in its circuit diagram to the emitter of the junction transistor 25.

A collector voltage (X axis) versus collector current (Y axis) characteristic for the Fig. 2a embodiment and for its circuit diagram is shown in Fig. 4. This characteristic is for a constant source voltage of 1.7 volts. This characteristic, as seen in Fig. 4, has a positive resistance portion 31 and a negative resistance portion 32. The negative resistance portion of the characteristic arises when the junction transistor 25 is not in saturation. As the collector voltage rises, the voltage applied to the gate of the unipolar field-effect transistor 23 will rise, and this will decrease the drain current flowing from the field-effect transistor 23. In this manner, the base current flowing to the junction transistor 25 is decreased, and this decrease in base current will cause a decrease in the collector current. Thus, as the collector voltage is increased, the collector current of the transistor 25 will decrease, thus providing the negative resistance portion of the characteristic. The positive resistance portion of the characteristic occurs during the time that the junction transistor 25 is saturated. At low values of collector voltage, the drain current of the field-effect transistor 23 will be high, and thus the base current of the transistor 25 will be high enough to cause the transistor 25 to saturate. As the collector voltage is increased, it will decrease the current flowing from the drain of the field-effect transistor 23. However, since the transistor 25 is in saturation, this will have no effect on the collector current of the transistor 25. Therefore, the collector current will increase as the collector voltage increases, thus providing the positive resistance portion 31 of the characteristic shown in Fig. 4. The point at which the characteristic changes from positive resistance to negative resistance is the point at which transistor 25 comes out of saturation.

From Fig. 4, is will be seen that the device has bistable properties. For example, the 1500 ohm load line 34, drawn from the point represented by 5 milliamperes and zero volts to the point represented by zero milliamperes and 7.5 volts, crosses the characteristic three times. One crossing is on the positive resistance portion 31 of the characteristic, another crossing is on the negative resistance portion 32, and the third crossing is on the cut-off line at a current of zero milliamperes. Therefore, two stable points are provided, one being on the positive resistance portion where the transistor 25 is in saturation, and the other being on the cut-off line where the field-effect transistor 23 is pinched off and the junction transistor 25 is cut off.

Fig. 5 exemplifies the switching characteristics of the Fig. 2a embodiment. In Fig. 5, the reference number 35 generally designates the semiconductor network, in order to facilitate the description of the operation of the device, which is represented by its circuit diagram comprising the unipolar field-effect transistor 23 and the junction transistor 25. In Fig. 5, the emitter 21 is grounded and the collector 19 is connected to a source of positive voltage through a 300 ohm resistor 36. The source 17 is connected to the positive terminal of a variable voltage source 38 through the series circuit of a 2 kilohm resistor 40 and a 51 ohm resistor 42. The negative terminal of the source 38 is grounded. A terminal 44 is connected to the junction between resistors 40 and 42 to provide an input to the circuit.

If the circuit is in the condition in which the field-effect transistor is pinched off and the junction transistor is cut off, and a positive pulse is applied to the input 44, the

voltage at the source 17 will rise at a rate depending on the RC time constant associated with the input resistor 40 and the capacitance from the source 17 to ground. When the voltage at the source 17 starts to rise, the gate-to-source voltage of the field-effect transistor 23 will decrease. When this gate-to-source voltage decreases to a value below the pinch-off voltage for the field-effect transistor 23, the field-effect transistor 23 will start to conduct. When the field-effect transistor starts to conduct, it will supply current to the base of the junction transistor 25. The base current flowing in the junction transistor 25 will start collector current to flow in the junction transistor 25 and the collector voltage of the junction transistor 25 will drop. As a result, the voltage at the gate of the field-effect transistor 23 drops, and more current flows through the field-effect transistor 23. The action is regenerative, and the field-effect transistor and the junction transistor are switched quickly to a fully conducting condition. If the field-effect transistor supplies enough current to the base of the junction transistor, it will saturate, the diode present due to the PN junction between the gate and the source of the field-effect transistor 23 will become forward-biased, and the voltage at the source 17 will be clamped to the voltage at the collector 19. The device will remain fully conducting until the voltage at the source 17 is decreased to less than the voltage at the collector 19, at which time the field-effect transistor 23 will start to be pinched off. A regenerative action will come into play to switch the device to a non-conducting condition if the junction transistor acts faster than the field-effect transistor 23. If this were not to happen the field-effect transistor would become non-conducting while the junction transistor is still in storage.

It should be noted that, when the junction transistor 25 is saturated, the voltage from the collector to the base of the junction transistor 25 is about zero volts; therefore, the voltage from the source to the drain of the field-effect transistor 23 will be the same approximately as the voltage from the source to the gate, and the field-effect transistor 23 will be saturated. Therefore, the source-to-drain current of the field-effect transistor may be less than its limiting value. If the junction transistor 25 requires the limiting value of drain current as base current in order to saturate, it will never saturate, and the field-effect transistor 23 will act as a base current clamp to keep the junction transistor 25 unsaturated. Of course, the low-gain junction transistors are the ones that would not saturate. These low-gain devices would be the slowest switching to a fully conducting condition because there would be less loop gain, but they would be cut off faster because of decreased storage time.

The loop gain and the RC circuit of the input resistance 40 and the capacitance from the source 17 to ground determine the rise time of the circuit. The storage and fall time of the circuit depend almost entirely on the storage and fall time of the junction transistor 25.

Reference to Fig. 2*a* will reveal a jumper connecting gate 14 to collector tab 19. Although such an arrangement lends itself advantageously to use in the foregoing embodiments, an alternative connection provides increased versatility in other applications. Thus, if the jumper is broken and a resistor inserted serially therein, relatively low power pulses may be applied to the gate 14 to effect switching from one of the stable states to the other.

Fig. 6 illustrates how semiconductor networks of the present invention may be connected to form a ring counter circuit. In Fig. 6, the semiconductor networks are designated generally by the reference number 35, and, in order to facilitate description of the operation of the invention, they are represented by the circuit diagram shown in Fig. 3. Thus, each semiconductor network 35 is represented by unipolar field-effect transistor 23 and a junction transistor 25 with the drain of the unipolar field-effect transistor 23 connected directly to the base of the junction transistor 25 and with the gate of the unipolar field-effect transistor 23 connected directly to the collector of the junction transistor 25. The connection between the gate of unipolar field-effect transistor 23 and the collector of junction transistor 25 provides the collector 19; the source of the unipolar field-effect transistor 23 provides the source 17; and the emitter of the junction transistor 25 provides the emitter 21.

The ring counter comprises a plurality of identical semiconductor networks or stages which may be of any number. In the specific embodiment of the present invention, only four stages are shown to simplify the showing in the drawings. These are designated generally by the reference numbers 41, 42, 43, and 44. Each stage of the ring counter comprises a semiconductor network 35 which has its collector connected through a 300 ohm resistor 47 to a source of +10 volts common to all three stages applied at a terminal 49. In each stage of the ring counter, the emitter 21 is connected through a 200 ohm resistor 51 to ground. In each stage of the ring counter, a capacitor 53 connects the source 17 of the bipolar field-effect transistor 35 to an input 55 common to all three stages. The input 55 is connected to ground by 51 ohm resistor 57. The col-

lector 19 in each stage is connected through a 1.5 kilohm resistor 59 to the source 17 of the next preceding stage. Thus, a resistor 59 connects the source 17 of the stage 41 to the collector 19 in the stage 42; a resistor 59 connects the source 17 in the stage 42 to the collector 19 in the stage 43; a resistor 59 connects the source 17 in the stage 43 to the collector 19 in the stage 44; and a resistor 59 connects the source 17 in the stage 44 to the collector 19 in the stage 41. Similarly, a 2.2 kilohm resistor 61 in each stage connects the source 17 to the emitter 21 in the preceding stage. Thus, the resistor 61 in the stage 44 connects the source 17 of this stage to the emitter 21 in the stage 43; the resistor 61 in the stage 43 connects the source 17 in this stage to the emitter 21 in the stage 42; the resistor 61 in the stage 42 connects the source 17 in this stage to the emitter 21 in the stage 41; and the resistor 61 in the stage 41 connects the source 17 in this stage to the emitter 21 in the stage 44.

Each of the stages 41, 42, 43, and 44 have two stable states. One stable state will be with the transistor 25 conducting and the field-effect transistor 23 conducting. In this condition, the stage is referred to as being turned on. In the other stable state, the field-effect transistor 23 will be pinched off, and as a result, the junction transistor 25 will be cut off. In this stable state, the stage shall be referred to as being turned off. It shall be assumed for purposes of description that the stage 41 is turned on, and that the stages 42, 43, and 44 are turned off. In the stages which are turned off, the collectors 19 will be substantially at +10 volts. Similarly, the emitters of the stages which are turned off will be substantially at zero volts. The voltage at the sources 17 in each of the turned-off stages 42, 43, and 44 is determined by the voltage-dividing effect of the resistors 61 and 59. Thus, the voltage at each source 17 in the turned-off stages will be six-tenths of the difference between the voltage at the collector of the succeeding stage and the voltage at the emitter of the preceding stage. For example, the voltage at the emitter 21 of the stage 42 is zero volts, and the voltage at the collector 19 of the stage 44 is in +10 volts. Thus, the voltage applied to the source 17 of the stage 43 will be six-tenths of +10 volts, or +6 volts. Since the voltage applied to the collector 19 of the stage 43 is +10 volts, the gate-to-source voltage of the field-effect transistor 23 will be +4 volts, which is sufficient to maintain this field-effect transistor pinched-off, and in this manner, the stage 43 is maintained in its turned-off stable state. Since the stage 41 is turned on, the voltage at the collector 19 of the stage 41 will be considerably less than +10 volts due to the voltage drop through the resistor 47. As a result, the voltage applied to the source 17 of the stage 44 will even be less than +6 volts, and the gate-to-source voltage of the field-effect transistor 23 in the stage 44 will be even greater than +4 volts. Therefore, the stage 44 will also be maintained in its turned-off stable state. Since the stage 41 is turned on, the voltage at the emitter 21 of this stage will be considerably greater than zero, and thus the voltage applied at the source 17 of the stage 42 will be greater than +6 volts. The values of the resistors 59 and 61 are selected so that the voltage applied to the source 17 does not make the gate-to-source voltage of the field-effect transistor 23 in the stage 42 less than the pinch-off voltage. Thus, the field-effect transistor 23 will be maintained pinched-off, and the stage 42 will be maintained in its turned-off stable state. It will be noted, however, that the gate-to-source voltage of the field-effect transistor 23 in the stage 42 will be less than the gate-to-source voltage of the field-effect transistors 23 in the stages 43 and 44. The values of the resistors 59 and 61 are selected so that the gate-to-source voltage in the field-effect transistor 23 in the stage 42 is just greater than the pinch-off voltage for reasons which will be explained below. Since the field-effect transistor 23 in the stage 41 is conducting, the voltage applied to the source 17 of this stage will be considerably less than the +6 volts, since a large amount of the current flowing through the resistor 59 will flow into the source of the field-effect transistor 23. As pointed out above, since the stage 41 is conducting, there will be a large voltage drop through the resistor 47. This voltage drop will be sufficient to bring the voltage between the collector 19 and the source 17 in the stage considerably less than the pinch-off voltage of the field-effect transistor 23. The field-effect transistor 23 will therefore be maintained conducting, and the stage 41 will be maintained in its turn-on stable state.

When a +input is applied to the terminal 55, it will be applied through the capacitors 53 to the sources 17 in each stage. This will have the effect of raising the voltage at the source 17 in each stage and decreasing the gate-to-source voltage in each stage. Since the stage 41 is already turned on, it will not have any effect on this stage. The voltages at the sources 17 in the stages 43 and 44 will be sufficiently low that the input pulse will not raise the potential at the sources 17 in the stages 43 and 44 enough to bring the gate-to-source voltage of the field-effect transistors 23 in these stages below the pinch-off voltage. Therefore, the input pulse will not affect the stages 43 and 44. As pointed out above, the potential at

the source 17 in the stage 42, however, is just above the pinch-off voltage, and thus when the input pulse is applied through the capacitor 53 to the source 17 in the stage 42, it will cause the voltage at the source 17 in this stage to rise sufficiently to bring the gate-to-source voltage of the field-effect transistor 23 in the stage 42 below the pinch-off voltage, and the field-effect transistor 23 in this stage will begin to conduct. When the field-effect transistor 23 in the stage 42 begins to conduct, it will cause current to flow into the base of the junction transistor 25 in this stage and, thus, the junction transistor 25 in stage 42 will begin to conduct. Current will start to flow through the resistor 47 in the stage 42, and this will cause the voltage at the collector 19 in the stage 42 to drop. This drop in voltage at the collector 19 further decreases the gate-to-source voltage of the field-effect transistor 23 in this stage, and thus more current flows through the field-effect transistor 23, allowing more current to flow into the base of the transistor 25. The effect is regenerative, and the field-effect transistor 23 and the junction transistor 25 will become fully conducting. In this manner, the stage 42 is turned on. The drop in voltage at the collector 19 is transmitted to the source 17 in the stage 41 by means of the resistor 59. When the voltage at the source 17 in the stage 41 drops, the gate-to-source voltage of the field-effect transistor 23 in the stage 41 increases. This increase in the gate-to-source voltage of the field-effect transistor 23 in this stage reduces the current flowing through this field-effect transistor, and thus reduces the current flowing through the junction transistor 25. This causes a rise in the potential at the collector 19 in the stage 41, and thus the gate-to-source potential of the field-effect transistor 23 in the stage 41 is further increased. Therefore, the current flowing through the field-effect transistor decreases further. The action in the stage 41 is regenerative, and the stage is turned-off. Thus, after the pulse has been applied to the input 55, the stage 42 is the stage which is turned on, and the stages 41, 43 and 44 are turned-off. Since each stage is identical and is connected with its adjacent stages in exactly the same manner, the stages 41, 43 and 44 will be maintained turned-off in exactly the same manner that the stages 42, 43 and 44, respectively, were maintained turned-off when the stage 41 was conducting. Similarly, the stage 42 will be maintained turned on in the same manner that the stage 41 was maintained turned on. The next pulse applied to the input 55 will cause the stage 43 to turn on which, in turn, will cause the stage 42 to turn-off in the same manner that the stage 42 was turned on and the stage 41 was turned-off. Each succeeding pulse will cause each succeeding stage to turn on, and the preceding stage to turn-off in the same manner. The next pulse applied after the stage 44 has been turned on will cause the stage 41 to turn on again, and the stage 44 will be turned-off. The device will operate in this manner continuously as long as pulses are applied to the input 55.

Semiconductor networks 35 may be interconnected to provide a flip-flop. This flip-flop circuit is provided when the ring counter is built as just two stages. When the ring counter is connected in two stages as a flip-flop circuit, larger input pulses will be required to cause switching from one stage to the other because the source 17 in the stage which is turned-off will be at a lower voltage due to its connection to the collector of the stage which is turned on through the resistor 59 of the stage which is turned on.

Figs. 7 and 8 illustrate the embodiment of the ring counter in semiconductor networks in accordance with the present invention. A semiconductor network is provided for each stage of the ring counter. Since each stage of the ring counter is identical, each semiconductor network providing the circuitry for each stage will be identical. Figs. 7 and 8 illustrate the semiconductor network for one of the stages of the ring counter. As shown in these figures, the semiconductor network comprises an oblong block of N-type material 71 or first region on which there is diffused a layer of P-type material. At one end of the oblong block, a slot 73 is cut through the layer of P-type material, dividing it into two parts 75 and 77, the part 75 forming a second region and being much longer along the oblong block 71 than the part 77 which forms a fifth region. A section 79 of N-type material is formed by diffusion in the layer of P-type material at one end of the part 75. A second section 81 of N-type material is formed by diffusion in the P-type layer close to the section 79, leaving a short path of P-type material joining the two sections 79 and 81. The sections 79, forming a fourth region, and 81, forming a third region, are diffused to a depth not quite as far as the PN junction between the N-type material of block 71 and the P-type material of part 75. Evaporated aluminium contacts 83 and 85, forming the sixth and seventh terminal electrodes respectively, are formed on the part 77 of the P-type layer at opposite sides thereof. An evaporated aluminium contact 87 is formed connecting a second terminal electrode to the section 79 of N-type material. An evaporated aluminium contact 89 is formed connecting a third terminal electrode to the section 81 of N-type material. An evaporated aluminium contact 91 is formed connecting the first terminal electrode to the part 75 of the P-

type layer close to the section 81 and on the opposite side thereof from the section 79. A second evaporated aluminium contact 101 is also formed connecting an eighth terminal electrode to part 75 of the P-type layer at the opposite end from the sections 79 and 81. The aluminium contacts 83, 85, 91 and 101 make ohmic contact with the layer of P-type material and the contacts 87 and 89 make ohmic contact with the sections of 79 and 81, respectively. Ohmic contacts in the form of tabs 103, 105 and 107 are formed connecting the fourth, third and fifth terminal electrodes to the block of N-type material on the opposite side from the layer of P-type material made up of the parts 75 and 77. The ohmic contact 103 is formed directly below the part 77 of the P-type layer. The ohmic contact 105 is formed directly below the section 79 of N-type material and the ohmic contact 107 is formed at the opposite end of the block 71 of N-type material beneath the aluminium contact 101. The semiconductor network shown in Figs. 7 and 8 can be fabricated by the same techniques described for the fabrication of the semiconductor network shown in Figs. 2*b* and 2*c*.

The above-described device shown in Figs. 7 and 8 can be used to provide almost the entire circuitry for a single stage of the ring counter. In order to use this device for the circuitry of a single stage, the contact 85 must be connected directly to the contact 87 and the contact 89 must be connected directly to the contact 105. The capacitor 53 of each stage is not provided as an integral part of the semiconductor network and must be connected externally. This capacitor will be connected to the contact 91. When this semiconductor network is used in the ring counter, the contact 83 will be grounded and +10 volts will be applied to the terminal 103. With the block connected in this manner, the complete circuitry for a single stage of the ring counter is provided. The resistance of the conducting path through the part 77 of the P-type layer between the contacts 83 and 85 provides the resistance 51 for the stage. The resistance of the path through the part 75 of the P-type layer between the contacts 91 and 101 provides the resistor 61. The resistance of the path through the N-type semiconductor material of the block 71 between the contacts 105 and 107 provides the resistor 59. The resistance of the path between the contacts 103 and 105 through the N-type material of the block 71 provides the resistor 47. The sections 79 and 81, the PN junction between the layer of P-type material and the block 71 of N-type material beneath these sections, and the contacts 87, 89, 91, and 105 with the contacts 89 and 105 connected together provide the Fig. 3 circuit the contact 91 providing the source contact the common connection to the contacts 89 and 105 providing the collector to gate interconnection and the contact 87 providing the emitter contact.

Thus, to connect a plurality of these stages formed out of semiconductor networks, as disclosed in Fig. 6, the contact 101 of each succeeding stage should be connected to the contact 87 of the preceding stage and the contact 91 of each preceding stage should be connected to the contact 107 of the succeeding stage. The unconnected terminals of the capacitors 53 connected to the contacts 91, of course, will be connected together to the input terminal 55 and through the resistor 57 to ground, as shown in Fig. 6 . In this manner the ring counter is provided with semiconductor networks.

Fig. 9 illustrates how the semiconductor network according to the present invention may be connected in a relaxation oscillator circuit. In Fig. 9, the reference number 35 generally designates the semiconductor network. The semiconductor network is represented in Fig. 5 by its circuit diagram in order to facilitate the description of the operation. The collector 19 is connected to a source of +10 volts applied at a terminal 132 through a 200 ohm resistor 134. The +10 volts at terminal 132 is also connected through a variable 1 megohm resistor 136 to the source 17. The emitter 21 is connected to ground through a 100 ohm resistor 43. A 0.022 microfarad capacitor 138 is connected between the source 17 and ground.

For purposes of the description of the operation, it is assumed that the capacitor 138 is discharged. The source 17 will therefore be at a low voltage, and as a result, the gate-to-source voltage of the unipolar field-effect transistor 23 will be high. Therefore, the field-effect transistor 23 will be pinched off, and will have no current flowing therethrough. As a result, no base current will flow through the junction transistor 25 and the transistor 25 will thus be cut off. Therefore, no collector current will flow in this transistor, and a high voltage will result at the collector of transistor 25. This high voltage will be applied to the gate of the transistor 23, maintaining it pinched off. Current will then flow from the positive source at terminal 132 through the variable resistor 136, charging the capacitor 138, thus causing the potential at the source 17 of the bipolar field-effect transistor 35 to rise. The capacitor 138 will charge in this manner until the voltage at the source 17 rises to a point at which the voltage between the gate and the source of the field-effect transistor 23 is below pinch-off. At this point, the field-effect transistor 23 will begin to conduct. When the field-effect transistor 23

starts to conduct, base current will start to flow in the transistor 25, thus causing collector current to flow in the transistor 25. This action will cause a drop in the collector voltage of the transistor 25 and in the gate voltage of the field-effect transistor 23. Therefore, current flow in the field-effect transistor 23 will increase. The action is regenerative, and the collector voltage of the transistor 25 will drop so far that the gate of the field-effect transistor 23 becomes forward-biased, the capacitor 138 then discharges through the gate of the transistor 23 and into the collector of the transistor 25. Of course, some of the capacitor current will also go through the base of the transistor 25. The capacitor 138 will continue to discharge in this manner until the voltage at the source 17 drops to a value at which the current in the field-effect transistor starts to pinch off. When the field-effect transistor 23 starts to pinch off, it will reduce the base current flowing through the transistor 25, and thus cause the collector current of the transistor 25 to drop. The gate voltage of the field-effect transistor 23 will therefore rise. This action will further pinch off the current flowing in the field-effect transistor 23. The action is regenerative, and the transistors 23 and 25 will both stop conducting. The capacitor 138 will then again start to charge through the resistor 136, and the cycle will repeat itself ad infinitum.

The frequency of the circuit is determined by the size of the capacitor 138 and the resistor 136, since these two elements determine the charging current to the capacitor 138 and the voltage at the source 17. With the proper choice of values for the capacitor 138 and the resistor 136, the circuit can be made to oscillate at any frequency in the range from less than 1 cycle per second to 600 kilocycles per second. The period and pulse width are directly proportional to the capacitance of the capacitor. The pulse width produced by the circuit can be decreased by decreasing the ratio of the resistance of the resistor 134 to the resistance of the resistor 136. By maintaining this ratio low, the transistor 25 is kept out of hard saturation and, therefore, it is easier to turn the transistor 25 off by the cumulative action.

WHAT WE CLAIM IS:—

1. A semiconductor network comprising a semiconductor wafer having therein or thereon a field-effect transistor including a source, drain and gate and a junction transistor including a collector-base and base-emitter junction, and wherein said source, said drain, said gate, said base-emitter junction and said collector-base junction are all adjacent one and the same major wafer face.

2. A semiconductor network according to claim 1, wherein said base-emitter junction terminates at said one major face and there defines a first enclosed area, and wherein said collector-base junction terminates at said one major wafer face and there defines a second enclosed area surrounding said first enclosed area.

3. A semiconductor network according to either preceding claim, wherein the channel of said field-effect transistor comprises an elongated portion of said wafer lying on said one major wafer face and spaced from the opposite major wafer face.

4. A semiconductor network according to claim 1, or 2, wherein the channel of said field-effect transistor comprises a circular portion of said wafer lying on said one major wafer face and spaced from the opposite major wafer face.

5. A semiconductor network according to claim 3 or 4, wherein the channel overlies the collector-base junction.

6. A semiconductor network according to any preceding claim, wherein the drain and base are contiguous with each other within the semiconductor wafer to provide an ohmic connection therebetween.

7. A semiconductor network according to any preceding claim, wherein said wafer includes one or more elongated portions thereof defining the properties of one or more resistors and wherein each resistor is electrically connected with one of the transistors.

8. A semiconductor network according to any preceding claim, further including an electrical connection between the gate and collector.

9. A semiconductor network substantially as hereinbefore described with reference to Fig. 2*a* of the accompanying drawings.

10. A semiconductor network substantially as hereinbefore described with reference to Figs. 2*b* and 2*c* of the accompanying drawings.

11. A semiconductor network substantially as hereinbefore described with reference to Figs. 7 and 8 of the accompanying drawings.

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10. A semiconductor network substantially as hereinbefore described with reference to Figs. 2*b* and 2*c* of the accompanying drawings.

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