

SYNCHRONIZING SYSTEM CAPABLE OF CERTAINLY EXECUTING SYNCHRONIZING OPERATION

ABSTRACT

In a synchronizing system, a CRC bit end judging circuit (3) judges an end of a CRC bit of the demodulated signal from the demodulating circuit (2) to produce a CRC bit end signal. A RSSI detecting circuit (4) detects a RSSI level of the received signal and produces a RSSI level signal. An edge detecting circuit (5) produces a level compared result signal when the RSSI level is greater than a predetermined threshold level. The edge detecting circuit (5) masks, in a predetermined time interval, the level compared result signal in response to the CRC bit end signal and the level compared result signal. The edge detecting circuit (5) produces a trigger signal after the predetermined time interval. A bit synchronous circuit (6) produces the bit synchronous signal. A bit synchronous correcting circuit (7) corrects the bit synchronous signal to supply a bit synchronous correct signal to the demodulating circuit (2).

Fig 1