

CLAIMS

WHAT IS CLAIMED IS:

1. A thermal conduction structure for an integrated circuit transistor device made using a back-side access process and mounted on a handle wafer such that a gate of the transistor device is oriented towards the handle wafer, including:
 - (a) at least one laterally-extending thermal path having a near portion in close thermal contact with the transistor device, and a far portion sufficiently spaced away from the transistor device in a lateral direction from the transistor device so as to be couplable to a generally orthogonal thermal pathway, each laterally-extending thermal path being substantially electrically isolated from the transistor device; and
 - (b) at least one generally orthogonal thermal pathway thermally coupled to at least one laterally-extending thermal path and configured to convey heat from the at least one laterally-extending thermal path to at least one of (i) at least one externally accessible thermal pad, or (ii) the handle wafer.
2. The invention of claim 1, wherein at least one laterally-extending thermal path is spaced from the transistor device by an electrically isolating structure.
3. The invention of claim 1, wherein at least one laterally-extending thermal path is spaced from the transistor device by an electrically isolating structure formed by a shallow trench isolation process.
4. The invention of claim 1, wherein at least one laterally-extending thermal path is formed at least in part by at least one metallization layer.
5. The invention of claim 1, wherein the handle wafer is spaced from the transistor device by a passivation layer, and the at least one generally orthogonal thermal pathway includes at least one thermal via formed through the passivation layer sufficiently so as to be thermally coupled to the handle wafer.

6. A thermal conduction structure for an integrated circuit transistor device made using a back-side access process and mounted on a handle wafer such that a gate of the transistor device is oriented towards the handle wafer, including:
 - (a) at least one dummy gate electrically isolated from the transistor device by a gate oxide and in thermal contact with the transistor device;
 - (b) at least one thermal path electrically isolated from the transistor device and in thermal contact with at least one dummy gate; and
 - (c) at least one generally orthogonal thermal pathway thermally coupled to at least one thermal path and configured to convey heat from the at least one thermal path to at least one of (i) at least one externally accessible thermal pad, or (ii) the handle wafer.
7. The invention of claim 6, wherein the dummy gate comprises polysilicon.
8. The invention of claim 7, wherein at least one thermal path is formed at least in part by at least one metallization layer overlaying at least a portion of at least one dummy gate and extending laterally from the transistor device.
9. A method of making a thermal conduction structure for an integrated circuit transistor device made using a back-side access process and mounted on a handle wafer such that a gate of the transistor device is oriented towards the handle wafer, including:
 - (a) fabricating at least one laterally-extending thermal path having a near portion in close thermal contact with the transistor device, and a far portion sufficiently spaced away from the transistor device in a lateral direction from the transistor device so as to be couplable to a generally orthogonal thermal pathway, each laterally-extending thermal path being substantially electrically isolated from the transistor device; and
 - (b) fabricating at least one generally orthogonal thermal pathway thermally coupled to at least one laterally-extending thermal path and configured to convey heat from the at least one laterally-extending thermal path to at least one of (i) at least one externally accessible thermal pad, or (ii) the handle wafer.
10. The method of claim 9, further including spacing at least one laterally-extending thermal path from the transistor device by an electrically isolating structure.

11. The method of claim 9, further including spacing at least one laterally-extending thermal path from the transistor device by an electrically isolating structure formed by a shallow trench isolation process.
12. The method of claim 9, further including fabricating at least one laterally-extending thermal path at least in part out of a metallization layer.
13. The method of claim 9, further including spacing the handle wafer from the transistor device by a passivation layer, and forming at least one thermal via through the passivation layer sufficiently so as to be thermally coupled to the handle wafer and to at least one generally orthogonal thermal pathway.
14. A method of making a thermal conduction structure for an integrated circuit transistor device made using a back-side access process and mounted on a handle wafer such that a gate of the transistor device is oriented towards the handle wafer, including:
 - (a) fabricating at least one dummy gate electrically isolated from the transistor device by a gate oxide and in thermal contact with the transistor device;
 - (b) fabricating at least one thermal path electrically isolated from the transistor device and in thermal contact with at least one dummy gate; and
 - (c) fabricating at least one generally orthogonal thermal pathway thermally coupled to at least one thermal path and configured to convey heat from the at least one thermal path to at least one of (i) at least one externally accessible thermal pad, or (ii) the handle wafer.
15. The method of claim 14, wherein the dummy gate comprises polysilicon.
16. The method of claim 15, further including fabricating at least one thermal path at least in part by fabricating at least one metallization layer overlaying at least a portion of at least one dummy gate and extending laterally from the transistor device.
17. The invention of claims 1 or 6, wherein the handle wafer is glass.
18. The method of claims 9 or 14, wherein the handle wafer is glass.