WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a gate stack structure including a plurality of interlayer insulating layers and a plurality of conductive layers, which are alternately stacked in a first direction, the gate stack structure having a stepped structure defined by an end portion of each of the plurality of conductive layers extending to a different length;

a gap fill insulating layer disposed on the gate stack structure to cover the stepped structure;

a tubular insulating layer intersecting the end portion of each of the plurality of conductive layers, the tubular insulating layer extending in the first direction to penetrate the stepped structure of the gate stack structure and the gap fill insulating layer; and

a conductive gate contact disposed in a central region of the tubular insulating layer,

wherein the conductive gate contact includes a protrusion part penetrating a side portion of the tubular insulating layer to be connected to one conductive layer among the plurality of conductive layers,

wherein an interface between the protrusion part of the conductive gate contact and the tubular insulating layer is spaced apart from the interlayer insulating layers.

2. The semiconductor memory device of claim 1, wherein the tubular insulating layer is isolated into a first tubular insulating pattern

penetrating the gate stack structure and a second tubular insulating pattern penetrating the gap fill insulating layer by the protrusion part.

3. The semiconductor memory device of claim 1, wherein the tubular insulating layer continuously extends to penetrate at least one conductive layer among the plurality of conductive layers and at least one interlayer insulating layer among the plurality of interlayer insulating layers.

4. The semiconductor memory device of claim 1, further comprising a blocking insulating layer extending along a surface of each of the plurality of conductive layers,

wherein the protrusion part penetrates the blocking insulating layer.

5. The semiconductor memory device of claim 1, wherein the conductive gate contact includes a pillar part surrounded by the tubular insulating layer, the pillar part being integrated with the protrusion part.

6. The semiconductor memory device of claim 1, wherein the protrusion part of the conductive gate contact is integrated with the one conductive layer among the plurality of conductive layers.

7. A semiconductor memory device comprising:

a first conductive layer;

a second conductive layer disposed to be spaced apart from the first conductive layer in a first direction;

an interlayer insulating layer between the first conductive layer and the second conductive layer;

a first tubular insulating pattern penetrating the first conductive layer, the interlayer insulating layer, and the second conductive layer, the first tubular insulating pattern extending in the first direction;

a second tubular insulating pattern spaced apart from the first tubular insulating pattern in the first direction, the second tubular insulating pattern extending in the first direction; and

a conductive gate contact including a pillar part extending from a central region of the first tubular insulating pattern to a central region of the second tubular insulating pattern and a protrusion part extending between the first tubular insulating pattern and the second tubular insulating pattern from the pillar part, wherein the protrusion part is in contact with a top surface of the second conductive layer.

8. The semiconductor memory device of claim 7, wherein a first interface between the first tubular insulating pattern and the protrusion part and a second interface between the second tubular insulating pattern and the protrusion part overlap with each other in the first direction.

9. The semiconductor memory device of claim 7, wherein the first conductive layer extends farther than the second conductive layer in a

second direction perpendicular to the first direction.

10. The semiconductor memory device of claim 7, further comprising a gap fill insulating layer formed on the protrusion part of the conductive gate contact, the gap fill insulating layer being penetrated by the second tubular insulating pattern.

11. The semiconductor memory device of claim 7, further comprising a blocking insulating layer interposed between the second conductive layer and the interlayer insulating layer, the blocking insulating layer extending between the second conductive layer and the first tubular insulating pattern,

wherein the blocking insulating layer includes an opening facing the protrusion part.

12. A semiconductor memory device comprising:

a first conductive layer;

a second conductive layer disposed to be spaced apart from the first conductive layer in a first direction;

an interlayer insulating layer between the first conductive layer and the second conductive layer;

a first tubular insulating pattern penetrating the first conductive layer, the interlayer insulating layer, and the second conductive layer, the first tubular insulating pattern extending in the first direction; and

a second tubular insulating pattern spaced apart from the first tubular insulating pattern in the first direction, the second tubular insulating pattern extending in the first direction,

wherein the second conductive layer extends along an inner wall of the first tubular insulating pattern and an inner wall of the second tubular insulating pattern while passing between the first tubular insulating pattern and the second tubular insulating pattern.

13. The semiconductor memory device of claim 12, further comprising a core conductive pattern extending toward a central region of the second tubular insulating pattern from a central region of the first tubular insulating pattern.

14. The semiconductor memory device of claim 12, wherein the first conductive layer extends farther than the second conductive layer in a second direction perpendicular to the first direction.