Detachable substrate or detachable structure and method for the production thereof

Field of the invention

The invention relates to the production of components from a thin layer on a substrate and the production of this thin layer/substrate assembly. The substrate can be an original or intermediate substrate and can be demountable, i.e. adapted to be separated from the thin layer.

Description of the prior art

Increasingly, components must be integrated onto supports different from those used to produce them.

Components on plastics material substrates or on flexible substrates may be cited, for example. By component is meant any microelectronic, optoelectronic or sensor (for example chemical, mechanical, thermal, biological or biochemical sensor) device that is completely or partly "processed", i.e. completely or partly produced.

A layer transfer method can be used to integrate the components onto flexible supports.

There are many other examples of applications in which layer transfer techniques can provide a suitable solution for integrating components or layers onto a support that is *a priori* unsuited to their production. In the same line of thinking, layer transfer techniques are also very useful when it is required to isolate a thin layer, with or without components, from its original substrate, for example by demounting or eliminating the latter. Still in the same line of thinking, turning over a thin layer and transferring it onto another support provides engineers with valuable freedom to design structures that would otherwise be impossible. Sampling and turning over thin films can be used to produce buried structures, for example, such as buried capacitors for dynamic random access memory (DRAM) where, in

contradistinction to the usual situation, the capacitors are formed first and then transferred onto another silicon substrate before fabricating the remainder of the circuits on the new substrate. Another example relates to the production of transistor structures referred to as double gate structures. The first gate of the CMOS transistor is produced on a substrate using a conventional technology and then turned over and transferred to a second substrate to produce the second gate and finish the transistor, thereby leaving the first gate buried in the structure (see, for example, K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie and T. Sugii, "High-Speed and Low-Power n+-p+ Double-Gate SOI CMOS", IEICE Trans. Electron., vol. E78-C, 1995, pp. 360-367).

The requirement to isolate a thin layer from its original substrate is encountered in the field of light-emitting diodes (LED), for example, for instance as reported in the documents W.S Wong *et al.*, Journal of Electronic MATERIALS, page 1409, Vol. 28, N° 12, 1999 and I. Pollentier *et al.*, page 1056, SPIE Vol. 1361 Physical Concepts of Materials for Novel Optoelectronic Device Applications I (1990). One of the objects sought here is to improve the control of extraction of the emitted light. Another object relates to the fact that in this particular example the sapphire substrate used to produce the epitaxial stack is *a posteriori* bulky, in particular because it is electrically insulative, which prevents making electrical contacts to its rear face. To be able to remove afterwards the sapphire substrate, which was advantageous for the phase of growing the material, would thus appear to be desirable.

An identical situation is encountered in the field of applications to telecommunications and microwaves, for example. In this situation, it is preferable for the components to be finally integrated onto a support having a

high resistivity, typically at least several kohms.cm. However, a highly resistive substrate is not necessarily available at the same cost and with the same quality as the standard substrates usually employed. In the case of silicon, 200 and 300 mm diameter silicon wafers of standard resistivity are available, whereas for resistivities greater than 1 kohm.cm, there is very little on offer in the 200 mm size and nothing at all in the 300 mm size. One solution consists in producing the components on standard substrates and then, during the final process steps, transferring a thin layer containing the components onto a glass, quartz, sapphire, *etc.* insulative substrate.

From a technical point of view, the major benefit of these transfer operations is to decorrelate the properties of the layer in which the components are formed and those of the final support layer, and they are consequently beneficial in many other situations.

There may also be cited situations in which the substrate that is beneficial for the production of the components is excessively costly. In this case, for example that of silicon carbide, offering improved performance (higher temperatures of use, significantly improved maximum powers and frequencies of use, *etc.*), but whose cost compared to silicon is very high, it would be beneficial to transfer a thin layer of the costly substrate (in this instance silicon carbide) onto the inexpensive substrate (here silicon), and to recover the remainder of the costly substrate for reuse, possibly after a recycling operation. The transfer operation can be carried out before, during or after the production of the components.

The above techniques can also prove beneficial in all fields in which obtaining a thin substrate is important for the final application. Power applications in particular may be cited, whether for reasons associated with the evacuation of heat, which is improved if the substrate is

thin, or because in some cases the current must flow through the thickness of the substrates with losses that are to a first approximation proportional to the thickness through which the current passes. Smart card applications for which a thin substrate is required for reasons of flexibility may also be cited. For these applications, the circuits are produced on thick or standard thickness substrates, which has the advantage, firstly, of good mechanical resistance to the various process steps, and, secondly, of conforming to standards with regard to their use on certain production equipment. The final thinning is achieved by demounting. This demounting can be accompanied by transfer to another support. In some cases the transfer to another support is not indispensable, especially if the final thickness aimed at during thinning is sufficient to produce self-supporting structures.

Various techniques can be used to transfer layers from one support to another. The techniques disclosed in 1985 by T. Hamaguchi *et al.*, Proc. IEDM, 1985, p. 688, may be cited, for example. These techniques are of great benefit since they enable a layer to be transferred from one substrate to another, but they necessarily consume the basic substrate (which is destroyed during the process) and cannot achieve homogeneous transfer of a thin film unless a stop layer is present (i.e. a nonhomogeneous layer in the substrate material).

Of the transfer methods known to the person skilled in the art, it is also possible to use one of transferring thin layers of materials that may contain the whole or part of a microelectronic component. Some of these methods are based on creating a buried weak layer within a material, by introducing one or more gaseous substances. On this subject see the documents US-A-5374564 (or EP-A-533551), US-A-6020252 (or EP-A-807970), FR-A-2767416 (or EP-A-1010198), FR-A-2748850 (or EP-A-902843), and

FR-A-2773261 (or EP-A-963598), which disclose such methods.

These methods are generally used with the objective of demounting the whole of a film from an original substrate to transfer it onto a support. The thin film obtained may then contain a portion of the original substrate. These films can serve as active layers for the production of electronic or optical components. They may contain a part or the whole of a component.

These methods in particular enable reuse of the substrate after demounting, very little of the substrate being consumed on each cycle. This is because the thickness removed is frequently no more than a few micrometers, whereas substrate thicknesses are typically several hundred micrometers. It is therefore possible to obtain substrates that are similar to substrates that are "demountable" (that is to say demountable) by mechanical stress, in particular in the case of the process disclosed in the document US-A-6020252 (or EP-A-807970). This particular process is based on implantation to form a fragile buried region which is cut at the time of final transfer.

Other methods, based on the "lift-off" principle, also demount a thin layer from the remainder of its original support, again without the latter necessarily being consumed. These methods generally use selective chemical etching of a buried intermediate layer, possibly associated with mechanical forces. This type of method is very widely used to transfer III-V elements to different types of support (see C. Camperi *et al.*, IEEE Transactions on photonics technology, vol. 3, 12 (1991), 1123). As explained in the paper by P. Demeester *et al.*, Semicond. Sci. Technol. 8 (1993), 1124-1135, the transfer, which generally takes place after an epitaxial growth step, can be carried out before or after the production of the components (by "post-processing" or "pre-processing", respectively).

Of the methods using a (pre-existing) buried layer of lower mechanical strength than the remainder of the substrate to obtain localized demounting, the ELTRAN® method may be cited (Japanese Patent Publication Number 07302889). In this case, a stack based on monocrystalline silicon is locally weakened by the formation of a porous region. Another similar situation consists in exploiting the presence of a buried oxide in the case of a silicon on insulator (SOI) structure, however standard the latter may otherwise be (i.e. produced without seeking any particular demountability effect). If the structure is bonded sufficiently strongly to another substrate and a high stress is applied to the structure, localized fracture, preferentially achieved in the oxide, can lead to a cutting effect on the scale of the entire substrate. The document "PHILIPS Journal of Research", vol. 49, N° 1/2, 1995, shows an example of this on pages 53 to 55. Unfortunately, the fracture is difficult to control and necessitates high mechanical stresses to bring it about, which is not free of the risk of breaking of the substrate or damaging the components.

The advantage of such buried fragile layer methods is that they can be used to produce layers based on crystalline silicon (or SiC, InP, AsGa, $LiNbO_3$, $LiTaO_3$, *etc.*) in a range of thickness from a few tens of ångström units (Å) to a few micrometers (µm), with very good homogeneity. Greater thicknesses can also be achieved.

To fabricate demountable structures for possible subsequent transfer of a layer onto another support or substrate, it is known to the person skilled in the art to control the energies of the bonds between the layer and the substrate, as indicated in the document EP 0702609 A1.

The inventors of this patent are also aware that, to produce a demountable substrate, it is also possible to use methods involving the control of bonding forces

existing at the "demounting" surface to assemble together temporarily the thin layer and the substrate from which it is subsequently to be demounted. The situation in which the bonding is obtained by molecular adhesion is of particular benefit. Of the categories of assemblies obtained by molecular bonding, silicon on insulator (SOI) substrates produced by these bonding techniques constitute a particularly beneficial category. The category encompasses a number of variants, the principles of which are described in the book "Semiconductor Wafer bonding Science and Technology", Q.-Y. Tong and U. Gösele, a Wiley Interscience publication, Johnson [sic] Wiley & Sons, Inc. Some variants are known as bonded SOI (BSOI) or bond and etch back SOI (BESOI). Apart from bonding involving molecular adhesion, these variants rely on physical removal of the original substrate, by polishing techniques and/or chemical etching techniques. Other variants, described in part heretofore as layer transfer techniques, are additionally based on bonding by molecular adhesion and demounting by "cutting" along a region that has been weakened, for example as in the methods described in the documents US-A-5374564 (or EP-A-533551) and US-A-6020252 (or EP-A-807970) (demounting along an implanted region) or in the document EP 0925888 (demounting by fracture along a buried layer that has been rendered porous). Whatever the exact technique used, the common feature of these variants is their use of molecular bonding, in most of the cases encountered in the literature between two substrates having silicon (Si) or silicon oxide (SiO_2) at the surfaces to be brought into contact. Other materials are sometimes encountered (nitrides, silicides, *etc.*).

If nondemountable SOI structures are to be obtained, the surface preparation operations are intended finally to provide, and often with the aid of annealing carried out after bonding, high bonding energies typically

from 1 to 2 J/m^2. Conventionally, with standard preparation operations, the bonding energy of the structure is of the order of 100 mJ/m^2 at room temperature and 500 mJ/m^2 after annealing at 400°C for 30 minutes, in the case of SiO_2/SiO_2 bonding (bonding energy determined by the blade method developed by Maszara (see: Maszara *et al.*, J Appl. Phys., 64 (10), p. 4943, 1988). When the structure is annealed at a high temperature (1 100°C), the bonding energy can be as high as 2 J/m^2 (C. Maleville *et al.*, Semiconductor wafer bonding, Science Technology and Application IV, PV 97-36, 46, The Electrochemical Society Proceedings Series, Pennington, NJ (1998)). Other forms of preparation prior to bonding exist, for example exposure of the surfaces to be bonded to a plasma (for example an oxygen plasma), and can yield equivalent bonding energies without always necessitating such annealing (YA, Li and R.W. Bower, Jpn. J. Appl. Phys., vol. 37, p. 737, 1998).

In contradistinction to the above, the inventors are interested in demountable SOI structures. It has been shown that different mechanical strengths can be obtained by modifying the hydrophilic properties and the roughness of the surfaces. For example, as indicated in the paper by O. Rayssac *et al.* (Proceedings of the 2nd International Conference on Materials for Microelectronics, IOM Communications, p. 183, 1998), hydrofluoric acid etching increases the roughness of a layer of silicon oxide. The paper describes how an 8 000 Å etch increases the rms roughness from 0.1 nm to 0.625 nm. It has been verified that SiO_2/SiO_2 bonding with rms roughnesses of 0.625 nm and 0.625 nm for the facing surfaces yields a bonding energy value of the order of 500 mJ/m^2 after annealing at 1 100°C, i.e. much lower than in the standard situation previously cited. The inventors have shown that in this case the roughening can be exploited to provide demountable bonding interfaces, even after annealing at high temperature, as

high as 1 100°C. By astutely combining roughness preparation before bonding with suitable thermal annealing treatments, it has been demonstrated that demountable SOI substrates can withstand, without untimely demounting at the assembly interface, most steps of a process for producing CMOS transistors (including in particular heat treatment steps at high temperature, typically 1 100°C, as well as steps of depositing constrained layers, for example layers of nitride), and could *a posteriori* be demounted at the bonding interface by the intentional application of controlled mechanical stresses.

Technical problem and solution in accordance with the invention

Delamination is a well-known problem in the context of multilayer structures, in particular in the field of fabrication techniques for microelectronic components, sensors, *etc.* This is because heat treatment, chemical treatment (hydrofluoric acid etching, *etc.*), mechanical and/or physical operations of removing materials (polishing, *etc.*) necessary for producing components, deposition and/or epitaxial growth steps, and the mechanical stresses generated during the production of nonhomogeneous stacks, often generate cleavages at the layer edge or start lift-off at the edges of the structures. In the case of SOI, for example, the many hydrofluoric acid treatments used to deoxidize the Si surface can in some cases lead to important overetching of the buried oxide and thereby weaken the surface film at the edge of the wafer.

Layer transfer techniques (with or without components) based on the production of demountable substrates by forming an intermediate layer or weakened interface (whether by implantation of substances, by formation of a porous region, by control of the bonding energy, *etc.*) come up against certain problems associated

with untimely delamination if the processing prior to intentional demounting is too aggressive. Cracking can start unintentionally at the edges, during the process of fabrication of the whole or part of the component, and can reduce the yield. Apart from the reduction of the surface area of the active film caused by peeling of the film at the edge, these problems can lead to a high increase in particulate contamination of the wafers, and therefore a high reduction of yield in the fabrication of components and contamination of the plant used (in particular furnaces).

An object of the invention is to alleviate the drawbacks previously cited thanks to a layer/substrate interface that reliably combines the imperative of easy demounting at the right time and the imperative of, where necessary, withstanding the application of heat or mechanical treatment necessary for the production of the whole or part of the microelectronic, optical, or acoustic components or sensors, or epitaxial growth steps, without causing premature demounting or delamination.

More generally, the invention consists in an assembly comprising a thin layer on a substrate, said layer being connected to said substrate by an interface or an intermediate layer having a controlled level of mechanical strength.

To this end it proposes, firstly, a method of preparing a thin layer including a step of producing an interface or an intermediate layer between said thin layer and a substrate, characterized in that said interface is produced so as to have a first region having a first level of mechanical strength and at least one second region having a second level of mechanical strength significantly greater than the first level.

In other words, the invention proposes a method of obtaining a structure having a buried structure (interface

or layer) whose mechanical strength is higher in one region than in another. Thus the interface (or the intermediate layer) can be optimized as a function of requirements, allowing for processing that it is intended to apply to it.

Throughout this document, the expression "mechanical strength" means the mechanical strength in the "strength of materials" sense, but can also refer more generally to the susceptibility to rupture or dissociation of a continuous or discontinuous medium (such as an interface or a stack, which could suffer delamination, for example, *etc.*), whether this is in response to pure mechanical stress (traction, bending, shear, compression, torsion, *etc.*), during heat treatment, or during chemical etching, as well as all feasible combinations.

In the case of the particular problem discussed hereinabove, if it is required to demount the substrate from the layer at the correct time, and not before, the first region having a lower mechanical strength is a region included within the second region.

Especially when the whole of the thin layer is to be transferred, at the wafer scale, the region with the highest mechanical strength is preferably a ring (an annular ring in the case of round substrates), whose width can vary from a few hundred micrometers to a few millimeters, or even be of the order of one centimeter. Thus the ring can constitute the periphery of a round, square, polygonal or other shape plate whose core is of lower mechanical strength.

In a situation corresponding instead to demounting at the level of portions of the thin layer (by die, by component, set or subset of dies, *etc.*), the preparation of said layer preferably includes a step wherein at least one fragment of said layer is isolated on the substrate and said second region extends along the contour of said fragment. Thus the first region can be fragmented, each

fragment being surrounded by a region of greater mechanical strength.

Accordingly, the interface or intermediate layer produced between the thin layer and the substrate is mechanically weaker in its central portion than at its periphery. This greatly reduces the risk of untimely delamination.

Said interface or buried layer can take various forms. It can in particular be defined as:

- a bonding interface (with or without adhesive, for example bonding by molecular adhesion), and with or without an intermediate layer (oxide, nitride),

- a layer of microcavities (and/or gas microbubbles and/or platelets), and more generally a layer of defects, or [sic]

- an intermediate layer having characteristics different from those of the substrate and the layer, for example a porous silicon layer, which can be differentiated in terms of its mechanical strength or its susceptibility to chemical etching (chemical and mechanical), *etc.*,

- an intermediate layer of different chemical composition intended to be selectively chemically etched.

The differentiation between connecting regions of higher or lower mechanical strength or other different kinds of connections can be effected:

- in the case of a bonded interface, by connecting energies obtained, for example, by different preparation before bonding (roughness, different hydrophilic properties, chemical surface connecting states, *etc.*) and/or by heat treatment differences, in particular after bringing into contact for bonding,

- in the case of a layer of microcavities, by reduced implantation dosing in the second region or by preferential growth of microcracks in the first region,

- in the case of a porous layer, by modifying the

percentage porosity so that it is higher in the first region,

- in the case of an intermediate layer of different chemical composition, intended to be selectively chemically etched, by varying the chemical composition, which can be a doping difference or a composition percentage difference for a semiconductor substance, for example, which would have a direct impact on any variation in sensitivity to chemical etching.

To be more precise, in the situation where there are only two regions, in accordance with preferred features of the invention, possibly in combination (in which case the second region surrounds the first region):

• After the step of producing the interface there are effected a step of isolating a fragment of the layer containing said first region and said second region so that said second region runs along the periphery of said fragment, followed by a demounting operation in which the substrate and the thin layer are lifted off; in this case, the lift-off step is sometimes advantageously preceded by a step of physical delimitation of the second region vis à vis the first region, for example after partial or total cutting, by total or partial chemical etching, by total or partial mechanical fracture, *etc.*

• The interface is produced between a surface of the substrate and a surface of the layer, and the step of producing the interface includes a step of preparing at least one of these surfaces and a bonding step during which that surface is bonded to the other surface by molecular adhesion bonding; the step of producing the interface preferably and advantageously includes a preparation step for each of the substrate and layer surfaces. The surface preparation step preferably includes a treatment step during which said surface in said first region is made less hydrophilic or its roughness is locally increased, for

example; this refers, for example, to localized acid etching of the surface in this first region; to be more precise, it is even more preferable if at least one surface includes an oxide layer and the acid etching is effected with hydrofluoric acid, the surface in this second region being protected from said etching by a protection (for example nitride) layer which is eliminated afterwards. In another variant, the surface of at least one of the two wafers is entirely roughened and in some portions the roughness is then modified, essentially improved, to obtain greater bonding forces, for example with the aid of chemical polishing treatment, mechanical or chemical-mechanical or ionic treatment, or by dry etching.

- To prepare the surface and control the roughness, especially if one of the surfaces is an oxide, partial acid etching can be effected using hydrofluoric acid.

- The step of producing the interface includes a step of weakening a buried layer in a starting substrate, whereby at least the first region is made weaker than the second region, said buried layer being disposed between a portion forming the layer and a portion forming the substrate. The weakening step preferably includes a step of implanting at least one element, preferably a gas, this implantation step being conducted in a different way for the first and second regions.

- The step of producing the interface or intermediate layer includes a treatment step adapted to render a surface layer of the substrate porous, this treatment step being conducted in a different manner for the first and second regions, followed by a coverage step in which the layer is produced on top of said porous layer. In the particular case where the substrate is of silicon, this treatment step advantageously includes electrolysis in a hydrofluoric acid medium.

- The mechanical and/or chemical strength of the

interface or connecting layer is modified by nonuniform heat treatment to selectively strengthen or selectively weaken some regions compared to others, according to whether it is a matter of bonding roughened surfaces, porous materials, buried defects, gaseous or other microcavities.

- The step of producing the interface is followed by a step of demounting the layer from the substrate. Between the step of producing the interface and the lifting off step, there is advantageously a bonding step during which the layer is bonded to a second substrate. Said bonding step advantageously consists of molecular adhesion bonding or adhesive bonding, in the latter case using an adhesive hardened by UV, a resin, or a polymer adhesive, for example. In these cases, the demounting step is advantageously effected by acid etching and/or application of mechanical stress.

- The layer is of semiconductor materials (Si, Ge, SiGe, SiC, GaN and other equivalent nitrides, AsGa, InP, Ge, *etc.*) or ferroelectric materials or piezoelectric materials ($LiNbO_3$, $LiTaO_3$), or processed or unprocessed magnetic materials.

- The thin layer on the demountable substrate was obtained by thinning an original semiconductor material substrate.

- The thinning is obtained by machining and/or chemical-mechanical or other polishing and/or chemical etching.

- The thin layer on the demountable substrate was obtained by cutting into the original semiconductor material substrate.

- The cutting is achieved by cutting at the level of a buried weak layer.

- The buried weak layer is obtained by implantation and demounting is obtained by heat and/or mechanical and/or

chemical treatment.

• The substance implanted is a gas (hydrogen, helium, *etc.*).

In terms of product, the invention proposes an assembly comprising a layer on a substrate, said layer being connected to said substrate by an interface of which at least a first chosen region has a first level of mechanical strength and a second chosen region has a level of mechanical strength significantly higher than the first level, and the second region surrounding the first region.

According to preferred features, which may be combined:

• A fragment totally or partially delimited (by cutting, etching, *etc.*) in said layer contains said first region and said second region such that said second region runs along the periphery of said fragment.

• The interface is produced between a surface of the substrate and a surface of the layer that are bonded by molecular adhesion. At least one surface of the interface preferably has a lower roughness in said second region than in the first region.

• The interface is formed by a buried layer in an original substrate, the first region being weakened more than the second region.

• The interface is formed by a porous layer between said layer and said substrate, said layer having differences of porosity between said first and second regions.

• Said layer is further bonded to a second substrate, advantageously by molecular adhesion bonding or adhesive bonding, for example by an adhesive hardened by UV radiation.

• The mechanical and/or chemical strength of the interface or connecting layer is selectively modified with the aid of treatments (heat treatments, UV exposure

treatments, laser irradiation treatments, *etc.*) that are localized or nonuniform to selectively strengthen or selectively weaken some regions more than others, according to whether it is a question of bonding roughened surfaces, porous materials, buried defects, or gaseous or nongaseous microcavities.

• The layer is of semiconductor materials (Si, Ge, SiGe, SiC, GaN and other equivalent nitrides, AsGa, InP, *etc.*) or ferroelectric or piezoelectric materials ($LiNbO_3$, $LiTaO_3$), or processed or unprocessed magnetic materials.

Brief description of the drawings

Objects, features and advantages of the invention will emerge from the following description, which is given by way of nonlimiting illustrative example and with reference to the accompanying drawings, in which:

- figure 1 is a diagrammatic partial plan view of a surface on which two regions are prepared so that they have different molecular bonding characteristics,
- figure 2 is a view in section taken along the line II-II in figure 1,
- figure 3 is a view of an assembly comprising a thin layer on a substrate with an interface of the figure 1 type,
- figure 4 is a diagrammatic view in section of the assembly of a thin layer on a substrate,
- figure 5 is a view in section of a substrate wafer provided with a protective layer,
- figure 6 is a view of the figure 5 wafer after recessing it,
- figure 7 is a view of said wafer after filling the recess with a deposit of oxide,
- figure 8 is a view of said wafer covered with the oxide deposit after polishing,
- figure 9 is a view of said wafer after elimination of surplus oxide coating,

- figure 10 is a view of said wafer after fixing the thin layer or after fixing a thick layer and then thinning it,

- figure 11 is a variant of the assembly [sic] of figure 10, in which the oxide coating penetrates into the substrate and into the thin layer,

- figure 12 is a variant of the assembly [sic] of figure 10, in which the oxide coating is on the thin layer,

- figure 13 is a variant of the assembly [sic] of figure 11, in which the oxide occupies different regions in the substrate and in the thin layer,

- figure 14 shows a variant in which the interface is formed of a layer formed by regions of different materials (in this example SiO_2 and Si_3N_4),

- figure 15 is a variant of figure 10, showing a plurality of regions formed by the oxide,

- figure 16 is a variant of figure 14, showing an intermediate layer formed of a plurality of regions of different materials,

- figure 17 is a variant [sic] showing concentric and alternating rings Z_1 and Z_2,

- figure 18 is a variant [sic] showing an array of regions Z_1 in an overall region Z_2,

- figure 19 is a diagrammatic view of the assembly of figure 4 after depositing a surface layer,

- figure 20 is another view after molecular bonding of a final substrate,

- figure 21 is another view after application of a lift-off operation,

- figure 22 is a diagrammatic view of a wafer obtained after lifting off and polishing,

- figure 23 is a view of a demountable assembly of the figure 4 type,

- figure 24 is a view thereof after production of the whole or part of the components, for example a first

transistor gate,

- figure 25 is a view thereof after deposition of oxide,

- figure 26 is a view thereof after planarization by CMP,

- figure 27 is a view thereof after molecular adhesion bonding (including heat treatment),

- figure 28 is a view thereof after demounting and deoxidization,

- figure 29 is a view of a demountable assembly of the figure 4 type,

- figure 30 is a view thereof after production of components,

- figure 31 is a view thereof after demounting with no transfer to a target substrate, by hydrofluoric etching and/or application of mechanical forces,

- figure 32 is a view thereof after demounting into a final substrate and a substrate that can be recycled,

- figure 33 is a variant of figure 30, after cutting of trenches or notches between components,

- figure 34 is a view thereof showing a component in the process of being lifted off, for example after hydrofluoric etching,

- figure 35 is a view analogous to figure 4,

- figure 36 is a diagrammatic view in section of the figure 35 assembly after adhesive bonding of a transparent substrate,

- figure 37 is a view of the upper portion of this assembly after lifting off and polishing,

- figure 38 is a view of the upper portion of this assembly after lifting off and polishing,

- figure 39 is a view of an assembly analogous to that of figure 4 showing regions [lacuna] are eliminated by chemical and mechanical cutting,

- figure 40 is a view thereof after bonding an

upper substrate,

- figure 41 is a view to a larger scale of an assembly including interleaved regions Z_1 and Z_2,

- figure 42 is a view of an assembly analogous to that of figure 4,

- figure 43 is a view thereof after deposition of an epitaxial stack based on GaN,

- figure 44 is a view thereof after bonding a substrate,

- figure 45 is a view thereof at the time of lifting off,

- figure 46 is a view of the upper portion thereof after polishing,

- figure 47 is a view thereof after removal of the layer under the stack,

- figure 48 is a view of a substrate including a buried weak layer, and

- figure 49 is a view of a substrate including a buried weak layer portion.

Description of the invention

1 - Molecular adhesion bonding interface

The preferred examples selected for the detailed description primarily relate to silicon, which is generally available in the form of round substrates, for example of 200 mm diameter. These methods transfer readily to other systems characterized in particular by materials other than silicon, in a nonlimiting manner and without departing from the scope of the invention.

Some embodiments of the method according to the invention tend to encourage lifting of the layer off its substrate at the overall level, i.e. on the scale of the whole of the substrate, while others tend to delimit fragments.

An assembly to be produced in the former case is shown diagrammatically in figures 1 and 2, the interface or

intermediate layer shown diagrammatically in figure 2 representing the region in which local bonding differences are to be created. In addition to these figures, figure 3 in particular shows one example of the preparation of a surface intended to participate in an interface having, in accordance with the invention, two regions having different mechanical strengths. To be more precise, in the example shown, the object is to obtain a central region Z_1 whose mechanical strength E_{c1} is less than that E_{c2} of a peripheral region Z_2 surrounding the central region.

Different methods can be used to obtain a higher bonding energy in the peripheral region Z_2 than in the central region Z_1. Examples of SiO_2/SiO_2 and Si/SiO_2 bonding are considered. In the case of layers of different kinds (Si_3N_4 is another conventional example, but there are also silicides), and by analogy with what is described hereinafter, it suffices to use appropriate chemical treatment (for example $NH_4OH/H_2O_2/H_2O$ (also known as SC1) for Si and H_3PO_4 or HF for Si_3N_4). Figure 4 shows the option in which the substrate 11 and the thin layer 14 are of monocrystalline silicon and two intermediate layers 12 and 13 are formed prior to bonding on the substrate 11 and the thin layer 14, respectively. Of course, only one of the two intermediate layers 12 or 13 may suffice, and the situation in which neither of them exists (i.e. that of Si/Si bonding) must be considered (i.e. there are two special cases). If the intermediate layers 12 and 13 exist and are both of SiO_2, the system is referred to as SiO_2/SiO_2 bonding. If only one of the two exists, and consists of SiO_2, then the system is referred to as Si/SiO_2 bonding.

A number of techniques can be employed to produce a structure like that shown in figure 4, in addition to technical aspects related to molecular adhesion bonding, including those previously cited, for the production of nondemountable SOI substrates (see Semiconductor Wafer

Bonding, Science and Technology, Q. Y. Tong and U. Gösele, Wiley Interscience Publication [sic]). Hereinafter the layer 14 is referred to as the active layer, being the layer comprising the components, except for certain special cases in which an additional, for example epitaxial, layer is deposited onto the layer 14. In some variants of the invention, the thin layer is obtained by thinning the structure chemically and/or mechanically. These variants are known as bonded SOI (BSOI) and bond and etch back SOI (BESOI). In addition to molecular adhesion bonding, these variants are based on physical removal of the original substrate by polishing techniques and/or chemical etching techniques. Other variants, partially described hereinbefore as layer transfer techniques, are based, in addition to molecular adhesion bonding, on demounting by "cutting" or cleaving along a weakened region, such as the methods described in the documents US-A-5374564 (or EP-A-533551) and US-A-6020252 (or EP-A-807970): demounting along an implanted region, or in the document EP 0925888: demounting by fracture along a buried layer that has been rendered porous.

With reference to specific aspects related to bonding for the production of demountable substrates, in the case of SiO_2/SiO_2 (or even Si/SiO_2) bonding, a temporary mask can first be used to deposit a protection layer, for example a layer of silicon nitride Si_3N_4, onto only the ring of the silicon oxide SiO_2 layer(s) 12 and/or 13. The oxide layer can be prepared in several ways (deposition, thermal oxidation of the silicon) and can have a thickness that varies according to the application. For this example, a 1 µm thick thermal oxide is chosen. The following structure is therefore obtained: the surface of the central disk is formed of oxide only and the surface of the external ring (which is typically a few mm wide) is formed of the oxide covered with an additional protection layer

(for example of nitride).

This is followed by hydrofluoric acid etching to roughen the surface of the oxide, the roughening increasing with the thickness of oxide removed. For each application, the roughness can be optimized, in particular as a function of the conditions of the method of producing the components (or of epitaxial growth), which must be formed without delamination, and the method adopted for the final demounting. Typically, hydrofluoric acid etching to remove a thickness of oxide of the order of a few hundred to a few thousand Å is a good starting compromise. A nitride thickness of the order of 1 000 Å protects the underlying oxide from hydrofluoric acid etching, which increases the roughness of the central region of the oxide layer(s) 12 and/or 13. The nitride is subsequently removed by etching with hot (> 110°C) orthophosphoric acid (H_3PO_4), for example. This can be combined with selective wet or dry cleaning to obtain different hydrophilic properties between the regions Z_1 and Z_2. The resulting effect is one of weaker bonding than the standard bonding at the center and bonding identical to the standard bonding at the location of the ring.

If the oxide removed is thick, in particular because the application requires this (especially in the range of a few thousand Å, knowing that 5 000 Å is a good starting compromise in many cases), it must be noted that in addition to the required effect of locally increased roughness, a difference in level is created between the central region (which has been hydrofluoric acid etched) and the ring (which has been protected from this etching). To obtain bonding of very high quality in the ring, in combination with bonding of satisfactory quality in the central region, it may be necessary to eliminate or reduce the difference in level in some cases. It can be appropriate to use polishing for this (for example

chemical/mechanical polishing). Because of the difference in level, polishing that is *a priori* uniform results, through a planarizing effect that is well known to the person skilled in the art of microelectronics, in preferential polishing of the emergent region, i.e. the region of the ring in the present instance. However, the polishing can also be intentionally localized to the ring. If the substrate is circular, the ring can be preferentially polished by using a polishing cloth with a central opening, for example, thereby reducing the level of the ring to that of the central region that has been hydrofluoric acid etched. Moreover, it is known that polishing leads to higher bonding energies than are obtained by conventional molecular adhesion bonding (with no polishing). This therefore combines two effects tending toward weaker bonding than the standard bonding at the center and stronger bonding at the location of the ring. This combination is another special case of what is shown in figure 3. Another way to reduce the level of the ring to that of the center is localized wet or dry etching.

An alternative to this is to roughen all of the intermediate layer(s) 12 and/or 13, i.e. without protecting the ring, but to add treatment localized to the ring that significantly increases the bonding strength. These treatments include, for example, the use of an oxygen plasma or localized annealing, one aim of which would be, through a flow effect, to reconstruct and reduce the roughness of the surface of the oxide, or any other treatment known to the person skilled in the art to improve the cohesion of the assembly. These treatments have the advantage that they do not create any relief.

Another alternative relates to the use of localized thermal annealing (laser beam, nonuniform furnaces, heating by lamps, *etc.*) after the bonding operation. As reported in C. Maleville *et al.*, Semiconductor wafer bonding, Science

Technology and Application [sic] IV, PV 97-36, 46, The Electrochemical Society Proceedings Series, Pennington, NJ (1998), a 100°C annealing temperature difference after bonding can significantly vary the bonding energy, especially in the range of temperatures beyond 800°C. This alternative can be used alone or in combination with roughening at least one intermediate layer 12 or 13, or alone [sic] (i.e. with no step of roughening at all). One very specific example, that must not in any way be regarded as limiting on the invention, applied to SiO_2/SiO_2 bonding is to anneal the whole of the structure at 1 000°C and to heat the ring selectively to 1 200°C. Another is not to anneal the ring at a temperature of 1 000°C at all. For this selective annealing alternative, it must be understood that, because of thermal conduction phenomena and the difficulty of producing equipment for localized heating with perfect selectivity, localized heating can result in a heat input gradient. In this case, the annealing temperature can be considered to be at a maximum at the edges of the substrate and to fall on approaching the center of the substrate.

Another variant of the method of producing a demountable substrate can be based on a difference in chemical nature between the region Z_1 and the region Z_2. The following pairs may be cited by way of nonexhaustive example: $Z_1=SiO_2$ and $Z_2=Si$; $Z_1=Si_3N_4$ and $Z_2=SiO_2$; $Z_1=Si_3N_4$ and $Z_2=Si$, *etc.* Only the pair $Z_1=SiO_2$ and $Z_2=Si$ is described here.

As shown in figure 5, a protective ring (of resin, deposited PECVD, *etc.*) a few mm wide is deposited onto a silicon substrate to define the dimensions of the region Z_2.

The structure is then etched (wet or dry, by any of the techniques conventionally employed to etch silicon) so that the etching attacks only the unprotected region.

Mechanical etching (milling, polishing, *etc.*) can also be envisaged so that only the center is machined, by virtue of the configuration and/or size of the tool employed. In the above cases, the operation of depositing a protection layer is no longer indispensable. Regardless of the method employed (possibly involving a step of removing the protective ring), a silicon wafer is obtained with a recess at the center, as shown in figure 6.

This defines the location of the region Z_1 (disk with recess) and the region Z_2 (outer ring).

An oxide is deposited by the CVD process on the resulting substrate with a recess. The thickness of the layer of oxide deposited is much greater than the depth of the recess, producing the structure shown in figure 7.

Planarizing by polishing eliminates the difference in level between the ring and the center of the structure as well as the high inherent roughness of this type of deposit (see figure 8). Hydrofluoric acid etching then produces the structure shown in figure 9. In this case, hydrofluoric acid etching is stopped when the silicon is flush with the ring. This produces a "silicon ring and roughened oxide at the center" configuration, which defines an energy difference between the regions Z_1 and Z_2, firstly because these two regions have different roughnesses and secondly because the nature of the materials is different (different molecular adhesion bonding properties).

Depending on the energy difference required between the regions Z_1 and Z_2, the above sequence can be modified to yield a "silicon ring and nonroughened oxide at the center" configuration. To this end, the hydrofluoric acid etching step can be eliminated, for example, and the previous polishing step extended so that polishing the silicon ring results in a flush surface. In this case, the energy difference between the regions Z_1 and Z_2 is essentially caused by the difference in the nature of the

materials. In this case, the difference is smaller.

A recess and an oxide deposit have been cited in the situation where they are produced on the substrate 11 (with the result that the figure 10 configuration is obtained after bonding). A variant consists in carrying out these operations on the side of the thin layer 14 (see figure 11), or even on both sides (see figure 12).

Methods for other pairs of materials that can exhibit a difference in mechanical strength can include a small number of additional steps. For example, if the aim is to obtain the pair Z_1=Si_3N_4 and Z_2=SiO_2, Si_3N_4 must be deposited in addition to the oxide, taking care to define the required ring for the whole of the structure using conventional masking techniques (photolithography, mechanical methods, *etc.*). This structure has the advantage of excellent chemical etching (for example hydrofluoric acid etching) selectivity between the two materials concerned, which could facilitate demounting through easy and selective removal of the ring by chemical etching.

Other configurations are possible, for example:

- figure 13 is a variant of figure 11 in which the central layer does not have the same dimensions in the substrate and in the thin layer,

- figure 14 shows an assembly in which the interface layer between the substrate and the thin layer has a central portion Z_1 and [sic] a material (Si_3N_4) different from that (SiO_2) of the peripheral portion Z_2, these two portions being of different materials (here Si) than those of the substrate and the thin layer,

- figure 15 is a variant of figure 10 in which there is a plurality of regions Z_1 of a material different from that of the support,

- figure 16 is a variant of figure 14 in which there is a plurality of regions Z_1 and a plurality of regions Z_2 of materials (here Si_3N_4 and SiO_2) different from

those (here Si) of the substrate and the thin layer.

Figures 15 and 16 can correspond to a plurality of geometries of which figures 17 and 18 are examples (at the die level or otherwise):

- figure 17 shows a configuration with a plurality of concentric bands Z_1 or Z_2, and
- figure 18 shows a configuration having an array (made up of rows and columns) of regions of one type (here Z_1) in an overall region of the other type (Z_2).

Apart from the production of the demountable substrate itself, using techniques based on molecular bonding, there are several means as to its use and to the means to implement it.

The benefit of the demountable substrate, depending on the thickness of the unprocessed active layer or of the processed active layer (i.e. its thickness when it has been processed to produce the whole or part of a component), is that it allows demounting of the active layer to obtain either a self-supporting layer (a relatively thick layer, whether the thickness is already present in the demountable substrate as manufactured or obtained during deposition steps subsequent to its fabrication, as is the case in an epitaxial growth step) or a surface layer, which is generally thinner, transferred onto a target support, whether the latter is the final support or merely a temporary support which is itself intended to be demounted.

There are various ways to transfer the surface layer to the target substrate.

First of all, transfer can be effected by molecular adhesion bonding of what is to become the thin layer to be transferred to another substrate.

By way of illustration, a demounting method is described next in the context of producing a new SOI structure that is referred to herein as the second SOI structure. This kind of method, *a priori* less direct than

the techniques previously mentioned, nevertheless has a number of benefits. The example chosen here relates to the production of a second SOI substrate with a buried oxide layer 500 Å thick, which thickness is difficult to obtain using this kind of method directly.

The first structure is obtained by one of the methods previously described, yielding a demountable substrate corresponding to figure 4. In this example the monocrystalline silicon layer 14 is to become the active layer. On this demountable substrate, in which the central region of the connecting layer has been roughened before bonding and has not undergone any strengthening heat treatment at very high temperatures (preferably less than 1 100°C and even better less than 1 000°C or even 900°C), a 500 Å oxide layer is formed by thermal oxidation to yield the structure shown in figure 20. This oxide is to become the buried oxide of the second SOI structure. In the present example, the demountable substrate (11+12+13+14+15) is molecular adhesion bonded to a silicon substrate 16 that is to become the final support of the active layer (see figure 2). The stack obtained is preferably stabilized at a high temperature (1 100°C) to consolidate strongly the second bond at the interface of the layers 15 and 16. This second bond is conventional in the sense that there is no differentiation between regions of different mechanical strength. The first bond, if subjected to the same treatment, nevertheless has at least in its central portion, corresponding to the region Z_1, a mechanical strength less than that of the second bond. A chemical and/or mechanical demounting method can be used. For example, the stack obtained as above is first immersed in a hydrofluoric acid bath, one object of which is to overetch the oxide layers 12 and 13, starting from the edges of the assembly, to eliminate the ring corresponding to the region Z_2 and reach the region Z_1. The two interfaces 12/13 and

15/16 are preferentially etched. Moreover, the interface 12/13 of the demountable substrate is advantageously an oxide/oxide interface. It therefore yields more readily than the interface 15/16 between the oxide and the silicon. Accordingly, during this step of lifting off the ring of higher mechanical strength, there is less surface etching at the interface of the second bond than at the interface of the demountable substrate. When the acid reaches the low energy region (the central region, see figure 21), mechanical demounting (by pressurized water jet, as in the document EP 0925888, by compressed air jet, as in the document FR 2796491, by traction, as in the document WO 00/26000, by insertion of a blade, *etc.*) completely frees the final structure 13+14+15+16 (see figure 22). Following removal of the oxide 13, for example by hydrofluoric acid etching, the final SOI structure is obtained. The Si wafer 11 that served as a substrate within the demountable substrate can be recycled and reused, for example to produce another demountable substrate (preferably after eliminating the layer 12).

Other means of eliminating a ring to obtain access to the region Z_1 can at least partially eliminate the ring. Wet or dry chemical etching techniques or other mechanical polishing, laser cutting, *etc.* techniques can be employed for this, localized to the ring (see figures 39 and 40, which correspond to the production of a mechanical or chemical cut (cross-hatched area), before bonding the second substrate).

Note that the 500 Å thick buried oxide layer 15 formed previously on the layer 14 could have been formed on the substrate 16 before bonding rather than on the layer 14. Another variant divides the 500 Å thickness into two portions, with one portion on the substrate 16, for example 250 Å thick, and the other portion on the layer 14, also 250 Å thick in this example.

Note that if the two molecular adhesion bonded interfaces are both of the oxide/oxide type, stabilization of the second bond at high temperature can be carried out in such a way as to guarantee that preferential hydrofluoric acid etching occurs at the first interface. In this method, the creation of a mechanically weak region Z_1 achieves preferential demounting of the complete stack at the first bond interface, and the region Z_2 firstly yields an active layer 14 of good quality and secondly prevents the onset of cracks that can cause losses of yield and a reduction in the surface of the active film caused by peeling of the film at the edge, and thus a strong increase in particulate contamination of the wafers.

Another example of the use of the method according to the invention relates to the production of double-gate transistor structures. The first operations relating to the fabrication of the transistors essentially consist in producing the first CMOS transistor gate (see figure 24) on a demountable substrate using conventional technology (see figure 23), as shown in figure 4, for example, in exactly the same way as previously described for the production of SOI structures with a thin buried oxide layer. The bonding stabilization temperature can be reduced in a temperature range of the order of 900/1 000°C. An oxide layer with a thickness of the order of 1 µm is then deposited onto this substrate (see figure 25) using a conventional deposition technique (for example CVD). The oxide is planarized using a conventional chemical/mechanical polishing technique (see figure 26). This is followed by molecular adhesion bonding to another silicon substrate 16 (see figure 27). The bonding is preferentially stabilized at a temperature from 1 000 to 1 100°C if the structures formed for the first gate can withstand this high a temperature, or at temperatures of the order of 900/1 000°C otherwise. Finally (see figure 28), demounting is carried out in exactly the

same way as previously (insertion of a blade, pressurized water jet, compressed air jet, *etc.*). Before resuming the transistor fabrication process, in particular to produce the second gate (on the new "substrate" shown in figure 28), the remainder of the oxide layer 13 is removed by chemical etching. Because the oxide is etched with a hydrofluoric acid solution of known etching selectivity with respect to silicon, etching stops naturally once the oxide has been entirely etched, revealing a silicon surface. The major advantage of this technique over other fracture techniques, for example obtained by way of implantation, is that it does not necessitate excessively complex finishing sequences that are problematic in terms of their potential to create defects, as for a final polishing operation, for example. The remainder of the double-gate transistor fabrication process will be obvious to the person skilled in the art.

The same method can be used in many other applications. If the first SOI structure (see figure 4) is used to produce transistors, circuits, components, *etc.*, these can be finally transferred onto many types of dedicated support. For example, the substrate 16 can be chosen for its electrical insulation properties (high-resistivity silicon, quartz, sapphire, *etc.*) to provide an ideal support for microwave and telecommunication circuits, thereby limiting losses in the substrate. For applications relating to flat screens, a transparent substrate is chosen for the final support.

Another example of demounting is briefly described here (see figures 29 to 32) in the case of producing circuits on thin substrates. The final thicknesses of interest are typically less than a few hundred µm, even of the order of a few tens of µm. They relate, for example, to power applications or applications to smart cards and other circuits for which some flexibility is required (plastics

material supports, curved supports, *etc.*). One variant relates to a type of demounting necessitating no transfer to a target substrate. Here the object is to achieve demounting without transferring the layer 14 after producing the circuits or components C, when the layer 14 is sufficiently thick to be self-supporting but too thin to withstand without damage a circuit production process (typically less than a few hundred µm thick, and even of the order of a few tens of µm). The method of producing the demountable substrate is identical in every respect to any of those described previously to produce the figure 4 structure, for example. In the case of 200 mm diameter silicon wafers, the standard substrate thickness is 725 µm. If the application requires a final substrate thickness of 80 µm, for example, a silicon substrate 725 - 80 = 645 µm thick is chosen for the support substrate 11. This 645 µm thick substrate is then molecular adhesion bonded, for example, to a 725 µm thick wafer, forming areas of lower mechanical strength. The 725 µm thick wafer is then thinned to the required thickness of 80 µm, for example by planing and chemical/mechanical polishing. The resulting assembly therefore corresponds to the standards and offers sufficient resistance to the processes for fabricating the whole or part of the components. After production of the latter, one of the demounting techniques previously cited may be used (see figure 31, hydrofluoric acid etching and mechanical stresses), except that the substrate 16 can be omitted. Its presence can be beneficial in some cases, however. After demounting, the self-supporting layer 14 alone represents the final substrate of interest, characterized by a substrate thickness of 80 µm, including the components. The remainder of the substrate can be recycled.

If required, the dies can be cut before demounting, as is clear from figures 33 and 34: figure 33 shows notches

between the components, extending to just below the future demounting region, and figure 34 shows a pull-off support SA bonded to one of the fragments and adapted to allow pulling off after hydrofluoric acid etching, if any.

The weakening parameters have to be adapted to the technological operations that have to be carried out on the demountable substrate prior to demounting, in particular thermal and chemical treatments, and according to the nature of the mechanical stresses. For example, if the demountable substrate consists of a surface layer of germanium having an SiO_2-SiO_2 bonding interface that has to withstand an epitaxial growth temperature of 550°C (which is typical in the case of growing GaInAs to constitute a solar cell for use in space), then the rms roughness must advantageously be 0.4 nm for the substrate to be demountable.

Another example of use concerns the production of circuits for smart cards, where the flexibility of the support becomes critical, firstly because of the increase in the size of the circuits, and secondly because the trend is to require cards with ever higher resistance to deformation. A monocrystalline silicon support whose thickness is greater than around 50 µm is too fragile in this context, because its thickness is too high if it is subjected to a bending force, as can happen regularly with a smart card.

Figure 35 shows a starting assembly similar to that shown in figure 4, with a starting substrate 11' covered with a layer 12' of silicon oxide that is molecular adhesion bonded to a second layer 13' of silicon oxide, in turn covered with a silicon layer 14'. The circuits are produced within the silicon layer 14'. Then, for assembly to the second support 16' (see figure 36), an adhesive is preferably chosen that produces a very thin layer 15, whilst having the highest possible mechanical strength at

low temperature, for example < 400°C, so as not to risk damaging the components of the active layer produced before this bonding step. These can advantageously be adhesives hardened by heat or by exposure to UV radiation (in this latter case, it is sufficient to choose a final substrate 16' that is transparent to UV).

When it comes to cutting along the weakened region of the demountable substrate (here the bonding interface 12'/13'), it may appear difficult to produce purely chemical lift-off because adhesives and substrates transparent to UV (in practice made of quartz and glass) are not totally inert to the chemical products (hydrofluoric acid, solvents, *etc.*). On the other hand, a purely mechanical action may be sufficient to lift off the structure at the weak interface 12'/13' if the bonding energy of the ring is lower than the strength of the adhesive and the various layers constituting the integrated circuits (this can be achieved relatively easily). It is then possible to use the substrate of the demountable substrate several times. Apart from limited chemical etching of the ring, it is further possible to eliminate the ring by making a circular cut in the structure after adhesive bonding. The cutting can advantageously be effected by a laser at the boundary between the high bonding energy region and the low bonding energy region. If the ring is only a few mm wide, or even narrower, it is then possible to reuse the substrate.

As a general rule, the residue of the first substrate is obtained, the support of the substrate referred to until now as "demountable" (see figure 37), and is reusable, preferably after polishing the layer 12' and the active layer 14' (figure 38), which is either transferred onto the other support 16' or free and self-supporting if the thickness of the layer 14' is appropriate.

Unlike the preceding examples, the second substrate 16' can instead be merely an intermediate substrate in a much longer process that will continue either with the pure and simple elimination of the intermediate substrate 16' or another layer transfer operation onto a yet further support, generally involving elimination of the substrate 16'. The demountable substrate obtained with the aid of the technique previously described is bonded to the intermediate substrate after it has been "processed". The intermediate substrate can be rigid or flexible (see the above examples). If it is rigid, it can even be a silicon wafer.

The use of adhesive films known to the person skilled in the art can be envisaged for the adhesive bonding, in particular for the operations of cutting silicon wafers and encapsulating integrated circuits or packaging or back-ending ("Blu-Tack®", Teflon® adhesive film, *etc.*). If the adhesive film is double-sided, it may be as well to stick an intermediate substrate to the rear face of the film, to act as a substrate or support for stiffening the assembly at cutting time.

The lift-off techniques that can be envisaged include the application of traction and/or shear and/or bending forces. It may be as well to combine the application of force with chemical etching of the interface, or other means, such as ultrasound. If the interface to be lifted off is of the oxide type, etching of the low energy interface makes it easier for the bonding interface to yield and therefore facilitates the transfer of the processed layer to the intermediate substrate. Under these conditions, it is advantageous for the processed layers to be protected (for example by an additional deposit of nitride in the case of hydrofluoric acid etching).

Stresses can be applied directly to the thin film

or to the intermediate substrate (known as a handle). They can be mechanical stresses (in particular applied by inserting a blade at the bonding interface), and/or use a lift-off tool (see WO 00/26000), and/or a jet, or involve inserting a gas flow, as described in the document FR 2796491, and/or a liquid (see EP 0925888, EP 0989593). In the case of a gas flow (or even a liquid flow, for example a flow of hydrofluoric acid if the interface is of oxide), the demountable substrate can advantageously be prepared beforehand (for example by chemical etching) to feed the fluid locally to the bonding interface. This facilitates preferential lifting off at the multilayer structure bonding interface, where the lifting off must take place, while protecting the various layers of the structure incorporating the components. Thus it is possible to lift off the bonding interface even when the adhesion between the internal component layers is weak. In this regard, see figures 39 and 40.

The intermediate substrate, which is sometimes referred to as a "handle", can then be cut, totally or in part (to form notches or cutting precursors), into elements corresponding to the electronic components, and which can be transferred to different supports. The transfer can be collective, in which case all of the components, even if they are interconnected only by a support, are transferred at the same time in the same technological operation, or component by component (or die by die), if the latter are transferred one after the other. The supports can be of plastics material, as in the case of a smart card, and in this case an adhesive is advantageously used for the transfer. The elements can also be transferred onto a wafer incorporating other electronic or optoelectronic devices, in which case the transfer can again use a molecular adhesion technique (see figures 4 and 19 to 22, imagining the additional presence of components formed in the layer

14). The elements can be transferred by conventional means such as pick and place means. The elements can also be transferred onto another support to improve the thermal properties, for example.

Then, by applying stress or localized heating (for example using a laser), the thin layer, previously bonded to its final support, can be demounted (element by element, or globally) from its handle by means of mechanical forces.

As indicated with reference to figures 17 and 18, the regions Z_1 and Z_2 may not define a system comprising a central circular region Z_1 surrounded by an outer ring Z_2. A multitude of other structures can be envisaged. The array of squares in figure 18 can be replaced by arrays of other shapes (rows, columns, concentric circles, *etc.*) whose pitch and other geometrical dimensions can vary as a function of the application and the demounting technique employed. The benefit of adopting an array may prove to be preferable if the structure to be produced imposes high mechanical stresses that are transmitted to the connecting interface (in this case short-range repetition of areas of good mechanical strength is preferable), or if the layer 14 may feature holes, whether intentional or otherwise, locally uncovering the connecting region, which may in turn be subject to untimely delamination whose epicenter is the hole, or to simplify the method (for example for cutting into individual dies) in the case of producing dies. In principle, dimensions of the order of 1 µm are preferred for structures having to withstand high stresses (for example hetero-epitaxy or any other deposition or technological step applying significant tension or compression to the structure), or in the case of small circuits, or of circuits produced with submicron photolithographic resolution. In the contrary situation, scales of the order of 1 mm or even 1 cm are preferable. Many combinations of more than two regions can of course be

envisaged (Z_1; Z_2, Z_3, *etc.*). Rather than a discrete number of types of regions of particular mechanical strength, a continuum of regions characterized by a continuous variation of the mechanical strength can be envisaged. For example, the mechanical strength decreasing continuously from a maximum value in the vicinity of the edge to a minimum value at its center can be envisaged. The variation can optionally be axisymmetrical about an axis perpendicular to the plane of the substrate. Production processes yielding this type of substrate and their use in demounting are in all respects similar to those described with reference to figures 1 to 8, provided that the geometrical shapes employed are suitable (mask shapes for formation of protection layers for selective roughness, mask shapes for selective deposition, shape of polishing tissues for preferentially polishing eccentric rings, *etc.*).

The above geometrical shapes are compatible with the transfer of a layer 14 as a whole from the demountable original substrate 11+12+13+14 to the target substrate 16.

As opposed to embodiments of the method according to the invention that tend to encourage demounting of the layer from its substrate at the global level, i.e. on the scale of the whole of the substrate, others tend to delimit fragments, the shape of which is clearly related to the dies or components to be produced from the active layer. Figure 41 shows one example of this, with enlargement of the region that subsequently accommodates the die (or any other component). This structure can be repeated as many times as there are components to be demounted on the original substrate. Ideally, each region Z_2 surrounds or simply extends along the contour of each fragment of the region Z_1. The surface area of the component (or die, *etc.*) can correspond exactly to the region Z_1, or be greater than or less than the latter, in configurations where one of the

surfaces of the component and of the region Z_1 encompasses the other. The configuration adopted depends on the demounting technique to be used, which can be the same as those previously described for demounting a substrate having only a ring Z_2 around a central disk Z_1. One interesting variant consists in using conventional component cutting techniques (sawing, laser cutting, *etc.*) to cut or delimit trenches, at least partially around dies, fragments, *etc.* Another beneficial variant is based on the use of chemical etching associated with a photolithography operation to produce identical trenches and/or to remove the connecting region corresponding to the region Z_2. As figure 41 shows in the case of one particular example, the vertical dashed lines indicate the contour of the required fragments. For example, after preparing molecular adhesion bonding over a large area, only layers 3 and 4 are cut to the contour shown, after which each fragment is lifted off the substrate, which amounts to considering that the substrate is lifted off each fragment (as an alternative, all the layers or all of the fragments can be cut at one and the same time). To the extent that, after cutting, the high mechanical strength region is at the periphery, the risk of delamination during treatment steps, for example to produce electronic, optical or other components on the layer 3 or 4, is reduced, whereas, when lifting off is required, it propagates without difficulty, in a controlled manner, in the central region (it may have been initiated at the periphery).

Combining the distribution of the regions Z_1 and Z_2 with the aim of forming an outer ring at the level of the substrate, as shown in figure 4, with a distribution intended to protect each of the dies, as shown in figure 13, is one beneficial combination.

Of course, the embodiments previously described are not limited to the single case of monocrystalline silicon,

and can be extended to many materials, such as other semiconductor materials (Ge, SiGe, SiC, GaN and other equivalent nitrides, AsGa, InP, *etc.*), ferroelectric and piezoelectric materials ($LiNbO_3$, $LiTaO_3$), and "processed" magnetic materials, whether components are produced before demounting or not.

As already mentioned, for the situation of a demountable substrate consisting of a surface layer of germanium having an SiO_2-SiO_2 bonding interface that has to be subjected to an epitaxial growth temperature of 550°C (as is typical in the case of growing GaInAs to constitute a solar cell for use in space), the rms roughness should advantageously be 0.4 nm for the substrate to be demountable.

Another example is that of epitaxially growing an epitaxial stack on a demountable substrate. This applies in particular to the production of blue and white LEDs and thin layer laser diodes (for example, for improved extraction of the light emitted or improved evacuation of heat, thanks to transfer onto a substrate that is a good conductor of heat, such as copper or diamond). In this case, the epitaxial stack concerned is based on composite semiconductors derived from GaN (AlN, GaAlN, GaAlInN, *etc.*). One method consists of using one of the processes previously described to form a demountable structure equivalent to that of figure 4 (or figure 26 or figure 35) in which the layer 14 is of SiC_6H (the transferred Si face is at the top in the figures), the layers 12 and 13 are of silicon oxides, as in the figure 4 example, and the substrate 11 is of polycrystalline SiC (or sapphire). The stack 15" based on nitrides (figure 43) is grown epitaxially on this structure (figure 42). The epitaxial techniques used can be those well known to the person skilled in the art such as molecular beam epitaxy (MBE) for one category, and metallo-organic chemical vapor deposition

(MOCVD) for another category. In the former case, the epitaxial growth temperatures rarely exceed 600°C, whereas the typical temperatures for the second category are of the order of 1 050 to 1 100°C. For each of the above two techniques, the choice of the pairs or sets of mechanical strength regions Z_1, Z_2, etc. must be optimized. In the second case, one of the processes previously described based on roughening of the two oxide layers 12 and 13 by hydrofluoric acid etching is chosen, for example, and another variant consists in forming a 5 mm wide ring from the edge of the substrate. Subsequent MOCVD epitaxial growth at 1 100°C produces, on this structure, a stack whose thickness is of the order of 1 μm. The structure is optionally annealed before the epitaxial growth stage, typically in the temperature range from 900 to 1 200°C, in order to consolidate strongly the mechanical strength of the ring. After the growth step, the assembly is subjected to deposition of oxide, planarization by CMP, molecular adhesion bonding (for example onto a silicon substrate), and annealing at 1 100°C to strength this latter bonding. The layer 16 is produced (figure 44). Finally, there is demounting at the bonding interface (figure 45). A few hours in a 50% hydrofluoric acid bath are sufficient to etch the oxide layer laterally to a depth of a few mm where this interface corresponds to the region Z_2, thereby uncovering the region Z_1. This is followed by demounting by means of mechanical forces, for example by inserting a blade, applying a pressurized water jet, or applying a compressed air jet, using the techniques previously described, for example. A final deoxidation step removes the residue of the oxide layer 13 (figure 46). At least the SiC layer 14 that served as a nucleation layer for the epitaxial stack can optionally be eliminated by etching (figure 41). Diodes can be produced before or after the final transfer.

2 - Weak buried layer incorporating microcavities, microbubbles or platelets

The interface between the substrate and what is to form the "active" layer can instead take the form of a buried weak layer, formed of microcavities, microbubbles, or platelets, for example. This process can be used with many semiconductor and other materials.

The difference between regions with different mechanical strengths is obtained by different levels of weakening; in the case where, as in figures 1 to 3, a central region is required to be surrounded by a peripheral region of greater mechanical strength, it is sufficient to weaken the structure less at the periphery than at the center, for example, by introducing at the periphery smaller amounts of the substances for weakening the region (for example by hydrogen implantation); this can be obtained by masking a portion of the layer during a portion of the implantation operation, for example, or by modifying the sweep during implantation; it can also be achieved by carrying out successive implantations, under different conditions, in the various regions whose properties are to be different. Regions can also be weakened differently by applying different heat treatments to them to obtain different levels of weakening.

With regard to the distribution of the regions Z_1 and Z_2 (a single ring, fragments, array of regions, multitude of regions, etc.), the techniques for demounting these structures (by means of mechanical stresses, chemical treatments, heat treatments, selective removal of rings and regions Z_2, etc.) and how they are put into practice, the elements and examples given in section 1 relating to an interface or intermediate layer produced by molecular adhesion remain valid.

3 - Interface formed of a porous layer

The person skilled in the art knows, in particular

from the document EP 0843346A2, that a porous layer can be obtained from the following materials in particular: Si, GaAs, InP, GaAsP, GaAlAs, InAs, AlGaSb, ZnS, CdTe and SiGe, in monocrystalline, polycrystalline or amorphous forms.

Thus it is only by way of example that the remainder of this description refers to silicon.

It is possible to obtain porous silicon by electrolysis in hydrofluoric acid. The person skilled in the art knows how to vary the porosity of the Si by modifying the concentration of the hydrofluoric acid or by varying the current. For example, reducing the hydrofluoric acid concentration from 50% to 20% changes the porosity from 2.1 g/cm^3 to 0.6 g/cm^3.

Thus by protecting the outer ring of the Si wafer with a thick deposit (of nitride, oxide or polycrystalline silicon, for example), it is possible to make a central region of the silicon layer porous while keeping the periphery intact. It then suffices to eliminate the layer deposited at the periphery and to electrolyze the entire wafer. The consequence of these two electrolysis operations is to produce a higher porosity at the center of the wafer than at the periphery.

A monocrystalline layer of Si is then produced on this porous layer by epitaxial growth (see figure 48, which represents an assembly comprising a substrate 21, the porous layer 22, having controlled differences in porosity between the regions Z_1' and Z_2', and a thin layer 23). Smoothing annealing of the hydrogen annealing type is advantageously employed before the epitaxial growth step to stop up the surface of the pores at least in part.

There can be crystal lattice continuity between the various layers if they have the same constituent.

The thickness of this monocrystalline layer, which thus becomes the active layer, depends on the intended applications.

Depending on the thickness of the active layer, after demounting it can become a self-supporting layer (if it is relatively thick) or it can be transferred to a target substrate (for example by molecular adhesion), especially if the layer is thin. The active layer can be lifted off its substrate by chemical means or by introducing a fluid locally into the porous layer.

An alternative is to render the periphery porous only to a distance of a few mm (as in figure 49, with a substrate 21', a layer 22', some regions of which are porous, and a monocrystalline layer 23'). It then becomes appropriate to eliminate this ring by cutting (by mechanical or laser cutting or by chemical processing using HF/HNO_3 or TMAH).

With regard to the distribution of the regions Z_1 and Z_2 (a single ring, fragments, array of regions, multitude of regions, etc.), the techniques for demounting these structures (by mechanical stresses, chemical treatments, heat treatments, selective removal of rings and regions Z_2, etc.) and how they are put into practice, the elements and examples given in section 1 relating to an interface or intermediate layer produced by molecular adhesion remain valid.

Note that:

- the interface can be a simple contact surface or a connecting layer,
- the fragments can be distributed in an array of squares, lines, concentric circles, etc.,
- the geometrical definition of the fragments is preferably related to the location and the size of the dies (to the nearest region Z_2 or the nearest sawing line, etc.),
- the surface preparation step before bonding can include roughening of the oxide layer,
- the preparation before bonding can affect the

roughness but also the hydrophilic properties,

- to obtain a greater roughness of the first region relative to that of the second region, both regions can be roughened and the roughness of only the second region reduced,

- the difference between Z_1, Z_2 can result from heat treatment after localized molecular bonding; alternatively, localized thermal annealing can be used after the bonding operation (laser beam, nonuniform furnace, heating by lamps, *etc.*),

- when the interface is a buried layer weakened by implanting a gaseous element, the latter preferably remains gaseous,

- to obtain lift-off, portions of material corresponding to the region Z_2 can advantageously be eliminated by chemical etching and/or by mechanical removal of material (machining),

- the lift-off step can be effected by etching in a vacuum and/or application of stresses; a jet of water, air or pressurized fluid can be used,

- the preceding description has emphasized a silicon layer, but SiC, GaN, GaAs, InP, SiGe and semiconductors derived therefrom are also relevant,

- there can be a step of epitaxial growth on the layer before demounting; likewise components can be produced completely or in part before demounting,

- there can be regions Z_3, and even Z_4, having levels of mechanical strength different from those of the regions Z_1 and Z_2,

- there can be a continuous evolution of the mechanical strength between extreme values, rather than in plateaux linked by discrete steps,

- the difference in mechanical strength between the regions can result from a difference of composition (interface formed of a layer with one region of one

material and the other region of another material, or an interface formed in part by the material of the substrate or the layer and in part by a transferred layer).

CLAIMS

1. A method of preparing a thin layer including a step of producing an interface between a layer intended to form part of said thin layer and a substrate, characterized in that said interface is produced so as to have at least a first region (Z_1, Z_1') having a first level of mechanical strength and a second region (Z_2, Z_2') having a second level of mechanical strength significantly greater than the first level of mechanical strength, the first region being included within the second.

2. A method according to claim 1, characterized in that the second region constitutes the periphery of a wafer of which the first region constitutes the core.

3. A method according to claim 1, characterized in that the first region is divided into fragments, each fragment being surrounded by a second region.

4. A method according to any one of claims 1 to 3, characterized in that the interface is produced between a surface of the substrate and a surface of the layer and the step of producing the interface includes a step of preparing at least one of said surfaces and a bonding step during which said surface is bonded to the other surface by molecular adhesion bonding.

5. A method according to claim 4, characterized in that the step of producing the interface includes a step of preparing the surface of the substrate and the surface of the layer.

6. A method according to claim 4 or claim 5, characterized in that the surface preparation step includes a treatment step for locally increasing the roughness of said surface in said first region.

7. A method according to claim 6, characterized in that the treatment step includes localized acid etching of the surface in said first region.

8. A method according to claim 7, characterized in

that the acid etching is effected with hydrofluoric acid, the surface in said second region being protected from said etching by a layer, for example of nitride, that is eliminated after etching.

9. A method according to claim 4 or claim 5, characterized in that the surface preparation step includes a step in which the surface is roughened entirely and a step in which the roughness of some portions is enhanced to obtain greater bonding forces.

10. A method according to claim 9, characterized in that the roughness of some portions is reduced by chemical polishing, mechanical treatment or chemical-mechanical treatment, or dry etching.

11. A method according to any one of claims 1 to 3, characterized in that the step of producing the interface includes a step of weakening a buried layer in a starting substrate, whereby at least the first region is made weaker than the second region, said buried layer being disposed between a portion forming the layer and a portion forming the substrate.

12. A method according to claim 11, characterized in that the weakening step includes a step of implanting at least one gaseous element, said implantation step being carried out differently for the first and second regions.

13. A method according to any one of claims 1 to 3, characterized in that the step of producing the interface includes a treatment step adapted to render a surface layer of the substrate porous, said treatment step being carried out in such a way as to render the first region more porous than the second region, and being followed by a covering step during which the layer is produced on top of said porous layer.

14. A method according to claim 13, characterized in that the substrate is of silicon and said treatment step includes electrolysis in a hydrofluoric acid medium.

15. A method according to any one of claims 1 to 14, characterized in that the step of producing the interface is followed by a step of demounting the layer from the substrate.

16. A method according to claim 15, characterized in that, after the step of producing the interface, there follows a step of cutting at least one fragment of the layer containing said first region (Z_1') and said second region (Z_2') so that said second region (Z_2') extends along the periphery of said fragment, possibly followed by a demounting operation during which the substrate and the thin layer are lifted off.

17. A method according to claim 15 or claim 16, characterized in that, between the step of producing the interface and the demounting step, there is a step of cutting the second region relative to the first region.

18. A method according to any one of claims 15 to 17, characterized in that it includes, between the step of producing the interface and the lift-off step, a step of producing in the layer the whole or part of microelectronic, optical or mechanical components.

19. A method according to claim 18, characterized in that each component is produced facing the first region of low mechanical strength surrounded by the second region of higher mechanical strength.

20. A method according to any one of claims 15 to 19, characterized in that, between the step of producing the interface and the demounting step, there is a bonding step during which the layer is bonded to a second substrate (16, 16').

21. A method according to claim 15, characterized in that said bonding step includes molecular adhesion bonding.

22. A method according to claim 15, characterized in that said bonding step includes adhesive bonding.

23. A method according to claim 17, characterized in that said adhesive bonding uses an adhesive that is hardened by UV radiation.

24. A method according to any one of claims 15 to 18, characterized in that the lift-off step is carried out by acid etching and application of mechanical stresses.

25. A method according to any one of claims 1 to 19, characterized in that the layer is of silicon.

26. An assembly including a layer on a substrate, said layer (13+14, 13'+14', 23) being connected to said substrate (11+12, 11'+12', 21) at an interface of which at least a selected first region (Z_1, Z_1') has a first level of mechanical strength and a selected second region (Z_2, Z_2') has a second level of mechanical strength significantly greater than the first level, and the first region (Z_1, Z_1') is included in the second region (Z_2, Z_2').

27. An assembly according to claim 26, characterized in that the second region constitutes the periphery of a wafer of which the first region constitutes the core.

28. An assembly according to claim 26, characterized in that the first region is divided into fragments, each fragment being surrounded by a second region.

29. An assembly according to claim 26, characterized in that a fragment cut out in said layer contains said first region and said second region so that said second region extends along the periphery of said fragment.

30. An assembly according to any one of claims 26 to 29, characterized in that the layer includes the whole or part of a microelectronic, optical or mechanical component.

31. An assembly according to claim 30, characterized in that said component faces the first region

of low mechanical strength surrounded by the second region of higher mechanical strength.

32. An assembly according to any one of claims 26 to 31, characterized in that the interface is produced between a surface of the substrate and a surface of the layer that are molecular adhesion bonded.

33. An assembly according to any one of claims 26 to 32, characterized in that at least one surface of the interface has greater roughness in said first region than in the second region.

34. An assembly according to any one of claims 26 to 31, characterized in that the interface is formed by a buried layer in a starting substrate, the first region being weakened more than the second region.

35. An assembly according to any one of claims 26 to 31, characterized in that the interface is formed by a porous layer between said layer and said substrate, said layer having different porosities in said first and second regions.

36. Assemblies [sic] according to any one of claims 26 to 35, characterized in that the layer is additionally bonded to a second substrate (16, 16').

37. An assembly according to claim 36, characterized in that said second substrate is molecular adhesion bonded.

38. An assembly according to claim 36, characterized in that said second substrate is adhesive bonded.

39. An assembly according to claim 38, characterized in that said adhesive bonding uses an adhesive that is hardened by UV radiation.

40. An assembly according to any one of claims 26 to 39, characterized in that the layer is of silicon.