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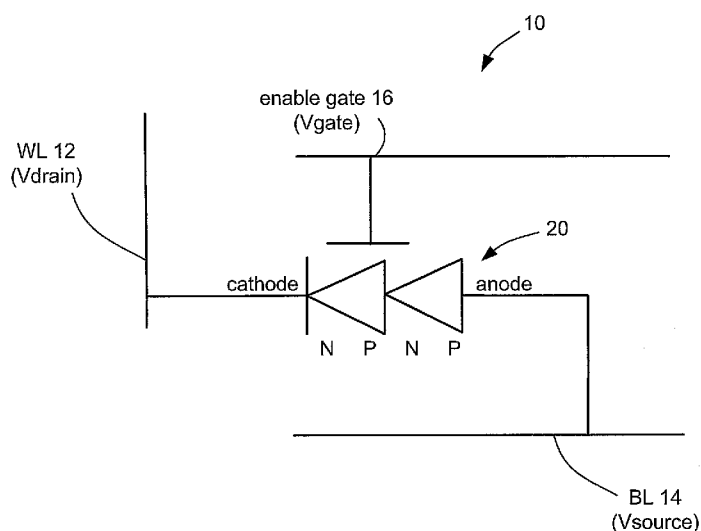
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(54) Title: RECESSED CHANNEL NEGATIVE DIFFERENTIAL RESISTANCE-BASED MEMORY CELL



(57) Abstract: Disclosed herein is an improved recessed thyristor-based memory cell. The disclosed cell comprises in one embodiment a conductive plug recessed into the bulk of the substrate, which is coupled to or comprises the enable gate of the cell. Vertically disposed around this recessed gate is a thyristor, whose anode (source; p-type region) is connected to the bit line and cathode (drain; n-type region) is connected to the word line. Aside from the recessed enable gate, the disclosed cell comprises no other gate, such as an access transistor, and hence is essentially a one-transistor device. As a result, and as facilitated by the vertical disposition of the thyristor, the disclosed cell takes up a small amount of area on an integrated circuit when compared to a traditional DRAM cell. Moreover, the disclosed cell is simple to manufacture in its various embodiments, and is easy to configure into an array of cells. Isolation underneath the cell, while not required in all useful embodiments, assists in improving the data retention of the cell and extends the time needed between cell refresh.

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