Description

The present invention relates to a protection circuit for protecting against high voltages applied to a semiconductor integrated circuit device having an active element formed in a semiconductor body of a first conductivity type, said protection circuit comprising an input-protecting bipolar transistor including a collector comprising a first semiconductor region of a second conductivity type formed in a major surface of said semiconductor body and connected to an exteral terminal or applied with a first potential, respectively; and emitter comprising a second semiconductor region of said second conductivity type formed in said major surface of said semiconductor body and kept at a predetermined potential level, or applied with a second potential, respectively; and a base region comprising a portion of said semiconductor body which is located between said collector and emitter.

Such a circuit is known from JP-A-55-72081 and Patent Abstracts of Japan, Vol.4, Nr.117(E-22) [599] and is intended to protect circuit elements from destruction by electrostatic discharge (hereinafter referred to as ESD).

If the input pin of the semiconductor device is applied with a high voltage arising from ESD (e.g., the discharge of static electricity from the human body, etc.), it may happen that internal elements of a semiconductor device will be electyrostatically destroyed. In order to prevent such electrostatic destruction, the semiconductor device is provided with a protection circuit located between the signal input pad of a semiconductor integrated circuit and the input circuit of internal elements.

The protection circuit is obtained by parasitically producing a bipolar transistor in the semiconductor device. An example of a conventional parasitic bipolar transistor of this type will be described. Let it be assumed that a signal input pad is connected to the input terminal of the input buffer of an internal circuit, by way of a first resistor for protection (e.g., a diffusion layer formed in the surface region of a semiconductor substrate) and a second resistor which is parasitically produced by provision of wiring layers on the semiconductor substrate. In this case, a parasitic bipolar transistor is produced such that it electrically connects the first and second resistors to either a power supply terminal or a grounded terminal.

In this conventional parasitic bipolar transistor, the substrate of the semiconductor integrated circuit functions as a base, a first diffusion region connected to the protective resistor functions as a collector, and a second diffusion region which is formed in the major-surface region of the substrate and is connected to either the power supply terminal or the grounded terminal functions as an emitter. With this structure, even if positive static charge is abruptly applied to the signal input pad, it is guided to either the power supply terminal VCC or the grounded terminal VSS through the parasitic bipolar transistor.

However, with the recent trend toward both high integration of semiconductor devices and use of smaller-size chips, it has become difficult to ensure a sufficiently large pattern area for the above parasitic bipolar transistor. In addition, since the resistance of the power supply lines provided inside a chip tends to increase in accordance with a decrease in the size of the chip, it may happen that the above-mentioned bipolar transistor will fail to reliably guide an excessive current to the outside of the semiconductor device. In particular, if the excessive current is produced by ESD and is therefore large in amount, it cannot be guided to the outside of the semiconductor device. As a result, the gates of the circuit elements formed on the neighboring substrate surface portion and the junctions inside the substrate are likely to be destroyed.

From US-A-4757363 it is known to provide a protective bipolar transistor with a pair of concentric guard rings. A guard ring having the same conductivity type as the substrate also forms the collector contact region.

Accordingly, an object of the present invention is to provide a protection circuit which is adapted for use in a semiconductor integrated circuit device and is capable of reliably preventing electrostatic destruction of circuit elements.

According to the invention, the protection circuit initially defined is characterized by a third semiconductor region of said first conductivity type formed between said active circuit element and the closer of said first and second semiconductor regions to said active element, said third semiconductor region having a high impurity concentration and being connected to the potential of said semiconductor body in order to absorb an excess current produced as a result of a voltage applied to said first semiconductor region beyond the protective capabilities of said input-protecting bipolar transistor.

In the protection circuit mentioned above, the third semiconductor region is located outside of the region of the bipolar transistor and serves to trap electrons. Even if a large amount of excessive current uncontrollable by the parasitic bipolar transistor is produced as a result of an excessive voltage applied due to ESD or the like, such excessive current is guided to the outside of the semiconductor device by way of the third semiconductor region. The third semiconductor region is particularly effective in protecting the neighboring circuit elements from electrostatic destruction, where the current-carrying capacity of the parasitic bipolar transistor is small.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Figs. 1A and 1B are sectional views of a protec-

tion circuit according to the first embodiment of the present invention, Fig. 1A illustrating a parasitic bipolar transistor located on the side of a grounded terminal, together with its neighboring structure, and Fig. 1B illustrating a parasitic bipolar transistor located on the side of a power supply terminal, together with the neighboring structure;

Fig. 2 is a sectional view showing the structure of the second embodiment of the present invention;

Fig. 3 is a sectional view showing the structure of the third embodiment of the present invention;

Fig. 4 is a planar pattern view of the structure shown in Fig. 3;

Figs. 5A and 5B are sectional views of a protection circuit according to the fourth embodiment of the present invention, Fig. 5A illustrating a parasitic bipolar transistor located on the side of a grounded terminal, together with its neighboring structure, and Fig. 5B illustrating a parasitic bipolar transistor located on the side of a power supply terminal, together with the neighboring structure; and

Fig. 6 is a sectional view showing the structure of the fifth embodiment of the present invention.

Embodiments of the present invention will now be described, with reference to the accompanying drawings.

Figs. 1A and 1B show the structure of a protection circuit according to one embodiment of the present invention, the protection circuit being formed between the signal input pad of a semiconductor integrated circuit device and an internal circuit thereof. The signal input pad IN is connected to the input terminal of the internal circuit (e.g., an input buffer which is not shown), with resistors R1 and R2 inserted therebetween. Resistor R1 is a protective resistor and is constituted by a diffusion layer or the like which is formed in a surface region of a semiconductor substrate, while resistor R2 is a parasitic resistor and is produced as a result of the formation of wiring layers on the semiconductor substrate. Between these resistors, a protection circuit is inserted. This protection circuit includes a parasitic bipolar transistor having such a structure as is shown in Figs. 1A and 1B.

Fig. 1A is a sectional view of the element structure of the parasitic bipolar transistor which is included in the protection circuit and is located on the side of a grounded terminal VSS. Referring to Fig. 1A, n^+-type semiconductor regions 102, 103 and 104 are formed in the surface region of a p-type semiconductor substrate 101. The semiconductor regions 102, 103 and 104 are isolated from each other. Of the three semiconductor regions, semiconductor region 103 functions as the collector region of the parasitic bipolar transistor and is connected to the input pad IN. The remaining semiconductor regions 102 and 104 each function as an emitter region, and are connected to the grounded terminal VSS. The substrate portion located between semiconductor regions 102 and 103 and the semiconductor portion located between semiconductor regions 103 and 104 each function as a base region of the parasitic bipolar transistor. As may be understood, a group of small bipolar transistor units 105 are formed such that they jointly constitute the bipolar transistor 106 mentioned above.

In that surface region of the semiconductor substrate 101 which is located in the neighborhood of the parasitic bipolar transistor 106, n^+-type semiconductor regions 107 and 108 are formed while being isolated from each other. These semiconductor regions 107 and 108 respectively function as a source and a drain region of a MOSFET to be mentioned later. A gate electrode 109 is formed on the substrate 101 in such a manner that it is located between the semiconductor regions 107 and 108. A gate oxide film 110 is interposed between the gate electrode 109 and the substrate 101. The semiconductor regions 107 and 108, the gate oxide film 110, and the gate electrode 109 jointly constitute the MOSFET 111, and this MOSFET 111 is part of a large number of circuit elements formed on the substrate 101. The semiconductor region 108 is connected to a circuit made up of a large number of elements.

Fig. 1B is a sectional view of the element structure of the parasitic bipolar transistor which is included in the protection circuit and is located on the side of a power supply terminal VCC. The parasitic bipolar transistor is paired with the above-mentioned parasitic bipolar transistor located on the side of the grounded terminal VSS, and is formed adjacent thereto. The parasitic bipolar transistor located on the side of the power supply terminal VCC has a similar structure to that of the parasitic bipolar transistor located on the side of the grounded terminal VSS. Specifically, the emitter regions 112 and 114 are connected to the power supply terminal VCC, and a plurality of small bipolar transistor units 115 are formed in such a manner as to jointly constitute a parasitic bipolar transistor 116.

The MOSFET 111 mentioned above is located at a position which is very liable to be affected if an excessive voltage caused by ESD or the like is applied to the input pad IN. In this embodiment, therefore, a p^+-type semiconductor region 117 having a high impurity concentration is formed between the parasitic bipolar transistors 106, 116 and the MOSFET 111. This high-impurity concentration semiconductor region 117 is formed by doping impurities into the substrate 101 with dose of $1 \times 10^{15}/cm^{-2}$, for example.

The bases of the two parasitic bipolar transistors 106 and 116 are maintained at the same potential as the substrate potential. If the static electricity applied to the pad IN is negative, it is guided to the power supply terminal VCC through transistor 116. If the static electricity applied to the pad IN is positive, it is guided

to the grounded terminal VSS through transistor 106. However, if an excessive voltage applied to the pad IN is too high and is uncontrollable by the parasitic bipolar transistors 106 and 116, such an excessive voltage is absorbed by the semiconductor region 117. Thus, the circuit elements formed on the substrate are protected from such a high voltage.

Let it be assumed that the substrate potential applied to the bases of the parasitic bipolar transistors 106 and 116 is expressed by VBB. In this case, the potential VBB applied to the locations indicated by arrow A differs from that applied to the locations indicated by arrow B, since the semiconductor region 117 is formed therebetween. More specifically, if an excessive voltage produced due to ESD or the like is applied to the input pad IN, those electrons which cannot be guided to the outside of the device by the parasitic bipolar transistors 106 and 116 are captured by the positive holes existing in the p^+-type semiconductor region 117. After captured or trapped in the p^+-type semiconductor region 117, the electrons are gradually discharged into the substrate 101 which is of the same conductivity type as the semiconductor region 117.

In the manner mentioned above, the MOSFET 111, which is most likely to be electrostatically destroyed due to the location thereof, is protected.

Fig. 2 is a sectional view showing the structure of a protection circuit according to the second embodiment of the present invention. In this embodiment, the present invention is embodied as a protection circuit located between a high-potential power supply terminal VCC and a low-potential grounded terminal VSS. In the second embodiment, n^+-type semiconductor regions 202, 203, and 204 are formed in the surface regions of a p-type semiconductor substrate 101 while being isolated from each other. The n^+-type semiconductor regions 202, 203 and 204 and the p-type substrate 101 jointly constitute a parasitic bipolar transistor, as in the embodiment shown in Figs. 1A and 1B.

The second embodiment shown in Fig. 2 differs from that shown in Figs. 1A and 1B, in that the semiconductor region 203 is connected to the power supply terminal VCC. With this structure, a plurality of bipolar transistor units 205 are formed between the two power supply terminals in such a manner as to constitute a parasitic bipolar transistor 206. In order to prevent electrostatic destruction of a MOSFET 111 located in the neighborhood of the parasitic bipolar transistor 206, a p^+-type semiconductor region 217 having a high concentration of p-type impurities is formed between the parasitic bipolar transistor 206 and the MOSFET 111. The semiconductor region 217 is maintained at the same potential as the substrate 101.

Fig. 3 is a sectional view showing the structure of a protection circuit according to the third embodiment of the present invention. In this embodiment, the protection circuit is formed by a bipolar transistor 316 which is similar to the parasitic bipolar transistor shown in Fig. 2, and a p^+-type semiconductor region 317 is formed in such a manner as to surround the protection circuit. The semiconductor region 317 is maintained at the same potential level as the substrate 101.

Fig. 4 is a planar pattern view of the structure shown in Fig. 3. As is clearly shown in Fig. 4, regions 312 and 314 which function as the collectors of parasitic bipolar transistors located between the two power supply terminals, and regions 311, 313 and 315 which function as the emitters of the parasitic bipolar transistors are formed in the surface region of the substrate 101. Regions 312 and 314 are connected to the power supply terminal VCC, while regions 311, 313 and 315 are connected to the grounded terminal VSS. The p^+-type semiconductor region 317 completely surrounds these parasitic bipolar transistors, to thereby obtain the protection circuit according to the third embodiment.

The protection circuit mentioned above is arranged in the neighborhood of each of the power supply terminal VCC and the grounded terminal VSS. With this arrangement, even if an excessive voltage applied to the power supply terminal VCC or grounded terminal VSS cannot be guided to the outside of the device by the parasitic bipolar transistor, it is uniformly suppressed by semiconductor region 317. Accordingly, the circuit elements located around the semiconductor region 317 can be protected from the excessive voltage. Needless to say, the circuit elements (e.g., MOSFET 111) located in the vicinity of the parasitic bipolar transistor can be protected from electrostatic destruction in a more reliable manner.

In the foregoing embodiments, the protection circuit is obtained by forming semiconductor regions in the major-surface region of the p-type semiconductor substrate. However, the protection circuit may be formed by providing a p-type well region in the major-surface region of an n-type semiconductor substrate and forming semiconductor regions in the p-type well region. An example of such an alternative structure is shown in Figs. 5A-5B and Fig. 6. In principle, the structure shown in Figs. 5A-5B and Fig. 6 is similar to the structure described above with reference to Figs. 1A-1B and Fig. 2.

As mentioned above, the protection circuits of the foregoing embodiments enable the size of a parasitic bipolar transistor for input protection to be reduced, thus enabling miniaturization of a semiconductor chip. Moreover, the protection circuits reliably suppress an excessive voltage produced due to ESD or the like.

Reference numerals added in the claims are for reference purposes only and do not alter the scope.

Claims

1. A protection circuit for protecting against high voltages applied to a semiconductor integrated circuit device having an active circuit element (111, 510) formed in a semiconductor body (101, 501, 502) of a first conductivity type, said protection circuit comprising:

an input-protecting bipolar transistor (106, 206, 116, 316) including:

a collector comprising a first semiconductor region (103, 203, 312, 314, 504, 613) of a second conductivity type formed in a major surface of said semiconductor body (101, 501, 502) and connected to an external terminal or applied with a first potential, respectively;

an emitter comprising a second semiconductor region (102, 104, 202, 204, 112, 114, 311, 313, 315, 503, 505, 513, 515, 602, 604) of said second conductivity type formed in said major surface of said semiconductor body (101, 501, 502) and kept at a predetermined potential level, or applied with a second potential, respectively; and

a base region comprising a portion of said semiconductor body (101, 501, 502) which is located between said collector and emitter;

characterized by:

a third semiconductor region (117, 217, 317, 511, 611) of said first conductivity type formed between said active circuit element (111, 510) and the closer of said first and second semiconductor regions (103, 203, 312, 504, 603, 102, 104, 202, 204, 112, 114, 202, 204, 311, 313, 315, 503, 505, 513, 515, 602, 604) to said active element (111, 510), said third semiconductor region (117, 217, 317, 511, 611) having a high impurity concentration and being connected to the potential of said semiconductor body (101, 501, 502) in order to absorb an excess current produced as a result of a voltage applied to said first semiconductor region beyond the protective capabilities of said input-protecting bipolar transistor (106, 116, 206, 316).

2. A protection circuit according to claim 1, characterized in that said semiconductor body is a p-type semiconductor substrate (101), and said first and second semiconductor regions are n-type impurity regions (103, 203, 312, 314, 311, 315, 102, 104, 112, 114, 202, 204) having a high-impurity concentration.

3. A protection circuit according to claim 1, characterized in that said semiconductor body (101, 501, 502) is a p-type well region (502) formed in a major surface of a semiconductor substrate of said second conductivity type, and said first and second semiconductor regions (504, 503, 505, 513, 515, 602, 603, 604) are n-type impurity regions having a high impurity concentration.

4. A protection circuit according to claim 1, characterized in that said second semiconductor region (102, 104, 112, 114, 503, 505, 513, 515) includes a plurality of second semiconductor portions, which are selectively connected to a power supply terminal or a grounded terminal.

5. A protection circuit according to claim 1, characterized in that said semiconductor body is p-type and said third semiconductor region (117, 217, 511, 611) is a p-type impurity region which has a high impurity concentration and which functions as an electron-trapping region.

6. A protection circuit according to claim 1, characterized in that said third semiconductor region (117, 217, 511, 611) surrounds said input-protecting bipolar transistor (106, 206, 116, 316).

7. A protection circuit according to any preceding claim wherein said collector (103, 504) is connected to an external terminal, and said emitter (102, 104, 112, 114, 503, 505, 513, 515) is biased to a predetermined potential.

8. A protection circuit according to claim 7, characterized in that said external terminal is an input pad (IN) to which an external signal is applied.

9. A protection circuit according to any of claims 1 to 6 wherein said collector (203, 312, 314, 603) is biased to a first potential, and said emitter (202, 204, 311, 313, 315, 602, 604) is biased to a second potential.

10. A protection circuit according to claim 9, characterized in that said first potential is a power supply potential, and said second potential is a ground potential.

11. A protection circuit according to claim 10, characterized in that said first semiconductor region (203, 312, 214, 603) includes a plurality of first semiconductor portions and said second semiconductor region (202, 204, 311, 313, 315, 602, 604) includes a plurality of second semiconductor portions, said first and second semiconductor portions being alternately arranged on said semiconductor body (101, 501, 502) and separated from each other by a predetermined distance.

Patentansprüche

1. Schutzschaltung zum Schützen gegen Hochspannungen, welche angelegt werden an eine integrierte Halbleiterschaltungsvorrichtung mit einem aktiven Schaltungselement (111, 510), gebildet in einem Halbleiterkörper (101, 501, 502) eines ersten Leitungstyps, wobei die Schutzschaltung umfaßt:
einen Eingangschutz-Bipolartransistor (106, 206, 116, 316) einschließlich:
eines Kollektors mit einem ersten Halbleiterbereich (103, 203, 312, 314, 504, 613) eines zweiten Leitungstyps, gebildet in einer Hauptoberfläche des Halbleiterkörpers (101, 501, 502) und verbunden mit einem externen Anschluß oder versorgt mit einem ersten Potential;
eines Emitters mit einem zweiten Halbleiterbereich (102, 104, 202, 204, 112, 114, 311, 313, 315, 503, 505, 513, 515, 602, 604) des zweiten Leitungstyps, gebildet in der Hauptoberfläche des Halbleiterkörpers (101, 501, 502) und gehalten auf einem bestimmten Potentialpegel oder versorgt mit einem zweiten Potential; und
eines Basisbereichs mit einem Abschnitt des Halbleiterkörpers (101, 501, 502) welcher angesiedelt ist zwischen dem Kollektor und dem Emitter;
gekennzeichnet durch
einen dritten Halbleiterbereich (117, 217, 317, 511, 611) des ersten Leitungstyps, gebildet zwischen dem aktiven Schaltungselement (111, 510) und dem näheren des ersten und zweiten Halbleiterbereichs (103, 203, 312, 504, 603, 102, 104, 202, 204, 112, 114, 202, 204, 311, 313, 315, 503, 505, 513, 515, 602, 604) zum aktiven Element (111, 510), wobei der dritte Halbleiterbereich (117, 217, 317, 511, 611) eine hohe Verunreinigungskonzentration hat und verbunden ist mit dem Potential des Halbleiterkörpers (101, 501, 502) zum Absorbieren eines übermäßigen Stroms, der erzeugt wird als ein Resultat einer Spannung, welche angelegt ist an den ersten Halbleiterbereich, oberhalb der Schutzfähigkeiten des Eingangsschutz-Bipolartransistors (106, 116, 206, 316).

2. Schutzschaltung nach Anspruch 1, dadurch gekennzeichnet, daß der Halbleiterkörper ein p-Typ Halbleitersubstrat (101) ist und der erste und zweite Halbleiterbereich n-Typ Verunreinigungsbereiche (103, 203, 312, 314, 311, 315, 102, 104, 112, 114, 202, 204) mit einer hohen Verunreinigungskonzentration sind.

3. Schutzschaltung nach Anspruch 1, dadurch gekennzeichnet, daß der Halbleiterkörper (101, 501, 502) ein p-Typ Wallbereich (502) ist, gebildet in einer Hauptoberfläche eines Halbleitersubstrats des zweiten Leitungstyps, und der erste und zweite Halbleiterbereich (504, 503, 505, 513, 515, 602, 603, 604) n-Typ Verunreinigungsbereich mit einer hohen Verunreinigungskonzentration sind.

4. Schutzschaltung nach Anspruch 1, dadurch gekennzeichnet, daß der Halbleiterbereich (102, 104, 112, 114, 503, 505, 513, 515) eine Vielzahl zweiter Halbleiterbereiche beinhaltet, welche selektiv verbunden sind mit einem Leistungsversorgungsanschluß oder einem Masseanschluß.

5. Schutzschaltung nach Anspruch 1, dadurch gekennzeichnet, daß der Halbleiterkörper vom p-Typ ist und der dritte Halbleiterbereich (117, 217, 511, 611) ein p-Typ Verunreinigungsbereich ist, welcher eine hohe Verunreinigungskonzentration hat und welcher als ein Elektroneneinfangbereich dient.

6. Schutzschaltung nach Anspruch 1, dadurch gekennzeichnet, daß der dritte Halbleiterbereich (117, 217, 511, 611) den Eingangschutz-Bipolartransistor (106, 206, 116, 316) umgibt.

7. Schutzschaltung nach einem der vorhergehenden Ansprüche dadurch gekennzeichnet, daß der Kollektor (103, 504) verbunden ist mit einem externen Anschluß und der Emitter (102, 104, 112, 114, 503, 505, 513, 515) auf ein vorbestimmtes Potential vorgespannt ist.

8. Schutzschaltung nach Anspruch 7, dadurch gekennzeichnet, daß der externe Anschluß ein Eingangskissen (IN) ist, an das ein externes Signal angelegt ist.

9. Schutzschaltung nach einem der Ansprüche 1 bis 6, dadurch gekennzeichnet, daß der Kollektor (203, 212, 314, 603) auf ein erstes Potential vorgespannt ist und der Emitter (202, 204, 311, 313, 315, 602, 604) auf ein zweites Potential vorgespannt ist.

10. Schutzschaltung nach Anspruch 9, dadurch gekennzeichnet, daß das erste Potential ein Leistungsversorgungspotential ist und das zweite Potential ein Massepotential ist.

11. Schutzschaltung nach Anspruch 10, dadurch gekennzeichnet, daß der erste Halbleiterbereich (203, 312, 214, 603) eine Vielzahl erster Halbleiterabschnitte beinhaltet und der zweite Halbleiterbereich (202, 204, 311, 313, 315, 602, 604) eine Vielzahl zweiter Halbleiterbereiche beinhaltet, wobei die ersten und zweiten Halbleiterbereiche

alternierend angeordnet sind auf dem Halbleiterkörper (101, 501, 502) und voneinander getrennt sind durch einen vorbestimmten Abstand.

Revendications

1. Circuit de protection permettant d'assurer une protection vis-à-vis de hautes tensions appliquées à un dispositif de circuit intégré à semiconducteur comportant un élément de circuit actif (111, 510) formé dans un corps semiconducteur (101, 501, 502) d'un premier type de conductivité, ledit circuit de protection comprenant :

un transistor bipolaire de protection d'entrée (106, 206, 116, 316) incluant :

un collecteur comprenant une première région semiconductrice (103, 203, 312, 314, 504, 613) d'un second type de conductivité formée dans une surface principale dudit corps semiconducteur (101, 501, 502) et connectée à une borne externe ou qui se voit appliquer respectivement un premier potentiel ;

un émetteur comprenant une seconde région semiconductrice (102, 104, 202, 204, 112, 114, 311, 313, 315, 503, 505, 513, 515, 602, 604) dudit second type de conductivité formée dans ladite surface principale dudit corps semiconducteur (101, 501, 502) et maintenue à un niveau de potentiel prédéterminé ou qui se voit appliquer un deuxième potentiel, respectivement ; et

une région de base comprenant une partie dudit corps semiconducteur (101, 501, 502) qui est située entre ledit collecteur et ledit émetteur,

caractérisé par :

une troisième région semiconductrice (117, 217, 317, 511, 611) dudit premier type de conductivité formée entre ledit élément de circuit actif (111, 510) et la plus proche desdites première et seconde régions semiconductrices (103, 203, 312, 504, 603, 102, 104, 202, 204, 112, 114, 202, 204, 311, 313, 315, 503, 505, 513, 515, 602, 604) par rapport audit élément actif (111, 510), ladite troisième région semiconductrice (117, 217, 317, 511, 611) présentant une concentration en impuretés semiconducteur (101, 501, 502) afin d'absorber un courant en excès produit en tant que résultat d'une tension appliquée à ladite première région semiconductrice au-delà des capacités de protection dudit transistor bipolaire de protection d'entrée (106, 116, 206, 316).

2. Circuit de protection selon la revendication 1, caractérisé en ce que ledit corps semiconducteur est un substrat semiconducteur de type P (101) et lesdites première et seconde régions semiconductrices sont des régions d'impuretés de type N (103, 203, 312, 314, 311, 315, 102, 104, 112, 114, 202, 204) présentant une concentration en impuretés élevée.

3. Circuit de protection selon la revendication 1, caractérisé en ce que ledit corps semiconducteur (101, 501, 502) est une région de puits de type P (502) formée dans une surface principale d'un substrat semiconducteur dudit second type de conductivité et lesdites première et seconde régions semiconductrices (504, 503, 505, 513, 515, 602, 603, 604) sont des régions d'impuretés de type N présentant une concentration en impuretés élevée

4. Circuit de protection selon la revendication 1, caractérisé en ce que ladite seconde région semiconductrice (102, 104, 112, 114, 503, 505, 513, 515) inclut une pluralité de secondes parties semiconductrices qui sont connectées sélectivement à une borne d'alimentation ou à une borne de mise à la masse.

5. Circuit de protection selon la revendication 1, caractérisé en ce que ledit corps semiconducteur est du type P et ladite troisième région semiconductrice (117, 217, 511, 611) est une région d'impuretés de type P qui présente une concentration en impuretés élevée et qui joue le rôle de région de piégeage d'électrons.

6. Circuit de protection selon la revendication 1, caractérisé en ce que ladite troisième région semiconductrice (117, 217, 511, 611) entoure ledit transistor bipolaire de protection d'entrée (106, 206, 116, 316).

7. Circuit de protection selon l'une quelconque des revendications précédentes, dans lequel ledit collecteur (103, 504) est connecté à une borne externe et ledit émetteur (102, 104, 112, 114, 503, 505, 513, 515) est polarisé à un potentiel prédéterminé.

8. Circuit de protection selon la revendication 7, caractérisé en ce que ladite borne externe est un plot d'entrée (IN) sur lequel un signal externe est appliqué.

9. Circuit de protection selon l'une quelconque des revendications 1 à 6, dans lequel ledit collecteur (203, 312, 314, 603) est polarisé à un premier potentiel et ledit émetteur (202, 204, 311, 313, 315, 602, 604) est polarisé à un second potentiel.

10. Circuit de protection selon la revendication 9, caractérisé en ce que ledit premier potentiel est un potentiel d'alimentation et ledit second potentiel est un potentiel de masse.

* C L M S *

11. Circuit de protection selon la revendication 10, caractérisé en ce que ladite première région semiconductrice (203, 312, 214, 603) inclut une pluralité de premières parties semiconductrices et ladite seconde région semiconductrice (202, 204, 311, 313, 315, 602, 604) inclut une pluralité de secondes parties semiconductrices, lesdites premières et secondes parties semiconductrices étant agencées en alternance sur ledit corps semiconducteur (101, 501, 502) et étant séparées les unes des autres d'une distance prédéterminée.