WHAT IS CLAIMED IS:

1. A memory device comprising:

a path state check circuit configured to check states of signal transmission paths, each signal transmission path including a data transmission path and a clock transmission path of the memory device,

wherein the path state check circuit includes,

a sampling circuit configured to perform a sampling operation by using pattern data that has passed through the data transmission path and a clock signal that has passed through the clock transmission path, and generate sample data, and

a management circuit configured to generate a comparison of the sample data with the pattern data to obtain path state information, and

wherein the management circuit is configured to compare reference state information with the path state information and configured to manage check result information indicating whether a re-training operation for the memory device is to be performed, based on a result of the comparison between the reference state information with the path state information.

2. The memory device of claim 1, wherein the sampling circuit is configured to generate the sample data by sampling a value of the pattern data at both a rising edge and a falling edge of the clock signal.

3. The memory device of claim 1, wherein, in response to receiving a command related to a check operation on the states of the signal transmission paths from outside of the memory device, or in response to completion of a training operation of the memory device, the path state check circuit is configured to perform the check operation every specific period.

4. The memory device of claim 1, wherein at least one of the pattern data and the clock signal is received from outside of the memory device.

5. The memory device of claim 1, wherein the path state check circuit further comprises:

a pattern data generation circuit configured to generate the pattern data; and

a clock signal generation circuit configured to generate the clock signal.

6. The memory device of claim 1, wherein the management circuit is configured to store the check result information in a status register of the memory device,

wherein the memory device is configured to transmit the check result information to outside of the memory device in response to a status read request received from the outside.

7. The memory device of claim 1, wherein the data transmission path comprises a first data transmission path and a second data transmission path,

wherein the pattern data comprises first pattern data passing through the first data transmission path and second pattern data that passing through the second data transmission path,

wherein the sampling circuit is configured to perform the sampling operation by using the first pattern data and the second pattern data which have passed through the data transmission path and the clock signal that has passed through the clock transmission path, and generate first sample data and second sample data,

wherein the management circuit is configured to generate a first comparison result by comparing the first sample data with the first pattern data and generate a second comparison result by comparing the second sample data with the second pattern data.

8. The memory device of claim 1, wherein, in response to the memory device receiving a write command from outside of the memory device, the path state check circuit is configured to perform a check operation on the states of the signal transmission paths at at least one of

i.) a timing before the memory device performs a write operation on a plurality of memory cells of the memory device in response to the write command,

ii.) a timing during which the memory device performs the write operation, and

iii.) a timing after the memory device completes the write operation.

9. The memory device of claim 1, wherein, in response to the memory device receiving data comprising pattern data and write data from outside of the memory device, the path state check circuit is configured to perform a check operation on the states of the signal transmission paths based on an arrangement position between the pattern data and the write data at at least one of

i.) a timing before the memory device performs a write operation on a plurality of memory cells of the memory device,

ii.) a timing during which the memory device performs the write operation, and

iii.) a timing after the memory device completes the write operation.

10. The memory device of claim 1, wherein the memory device is configured to determine whether to perform a write operation for a plurality of memory cells of the memory device by referring to the check result information.

11. The memory device of claim 1, wherein, in response to the memory device being in a latency mode, the path state check circuit is configured to perform an operation of checking the states of the signal transmission paths by using a clock signal in the latency mode.

12. A memory device comprising:

a path state check circuit configured to check states of signal transmission paths, each signal transmission path including a data transmission path and a clock transmission path of the memory device,

wherein the path state check circuit includes,

a sampling circuit configured to perform a plurality of sampling operations by using pattern data that has passed through the data transmission path and a plurality of clock signals that have passed through the clock transmission path, each of the plurality of clock signals having different phases, the sampling circuit configured to generate a plurality of pieces of sample data,

a management circuit configured to generate a comparison of the pattern data with the plurality of pieces of sample data, and configured to manage path state information indicating degree of alignment between the pattern data and a reference clock signal among the plurality of clock signals, based on results of the comparison, the path state information being used for re-training,

wherein the management circuit is configured to compare reference state information with the path state information and manage check result information indicating whether to perform a re-training operation for the memory device, based on a result of the comparison.

13. The memory device of claim 12, further comprising:

a phase shift circuit configured to shift a phase of the reference clock signal to generate the plurality of clock signals having different phases.

14. The memory device of claim 12, wherein the reference state information is the path state information generated as a result of a check operation of the path state check circuit within a specific time after a training operation for the memory device is completed.

15. A memory system comprises:

a memory device; and

a memory controller configured to control a memory operation of the memory device,

wherein the memory device comprises a sampling circuit configured to perform an operation of checking a state of a signal transmission path by using pattern data and a clock signal which have respectively passed through the signal transmission path to obtain sample data,

wherein the memory device comprises a management circuit configured to generate a comparison of the sample data with the pattern data to obtain path state information, the management circuit configured to compare reference state information with the path state information and to generate check result information indicating whether a re-training operation for the memory device is to be performed, as a result of performing the comparison between the reference state information with the path state information,

wherein the memory controller is configured to control the re-training operation for the memory device based on the check result information.

16. The memory system of claim 15, wherein the memory controller is configured to request the check result information from the memory device to determine whether to control the re-training operation for the memory device,

and the memory device is configured to provide the check result information to the memory controller in response to the request.

17. The memory system of claim 15, wherein the memory controller is configured to provide the memory device with a command for controlling the operation of checking the state of the signal transmission path of the memory device,

and the memory device is configured to perform the check operation in response to the command and provide the check result information to the memory controller.

18. The memory system of claim 15, wherein the memory controller is configured to provide at least one of the pattern data and the clock signal to the memory device.