

The invention is based on a method according to the preamble of Claim 1.

In the transmission of digital signals, reliable information as to whether a binary input signal is a useful signal or consists merely of amplified and limited interference signals is often required. Here it is assumed that the input signal occurs in binary form, i.e. is available in binary form at the output of input amplifier, equalizer and level detector.

Such a recognition circuit for a useful signal can be applied advantageously for example in a PLL circuit with a counting phase discriminator according to DE-OS 36 34 751. In this circuit it must be ensured that during the periods with no useful signal the setting of a forwards/backwards counter is not changed as this would give rise to a change in the centre frequency of the VCO oscillator of the PLL circuit and thus an extended running-in time of the PLL at the start of the next useful signal period.

In a PLL circuit according to the earlier PCT Application WO 90/13121 it is likewise necessary to differentiate between useful signal periods and dead periods. Here the switch-over takes place with the aid of a switching voltage derived from the head wheel rotation. As in the case of the known circuit referred to in the introduction, this solution can also lead to undesired detuning of the VCO oscillator, specifically when, at the time of the tape-head contact, instead of the useful signal only interference signals are supplied. This situation can occur, for example, when a non-prerecorded part of the tape is read, when during recording or playback there is temporarily dirt on one of the heads, or in the case of tracking faults.

The aim of the invention is to provide a simple method, which can be implemented using digital modules, for the reliable recognition of a useful signal in a binary signal.

This aim is fulfilled by the invention as described in Claim 1. A circuit for the implementation of the method is described in Claim 2. The number of directly consecutive, equivalent bits referred to in Claim 1 will be termed "run length" in the following.

The invention is based on the recognition that in the case of a binary signal generated from interference signals, the run length range of the useful signal is exceeded at relatively short intervals of time. This fact is exploited, in accordance with the invention, in order to generate a control quantity which indicates the useful signal or the interference signal. A circuit corresponding to the method according to the invention operates particularly reliably and rapidly and can easily be integrated as a pure digital circuit. A fundamental advantage of recognising the useful signal directly from the input signal also consists in that the supply line for an external useful signal marker signal, for example from the head switch-over device, the channel decoder or the drop-out recognition device, is not required.

The invention will be explained in detail making reference to the drawing. In the drawing:

Fig. 1 shows an exemplary embodiment of a circuit for the method according to the invention and

Fig. 2 shows the application of the circuit according to Fig. 1 in the known circuit described in the introduction with a counting phase discriminator.

The circuit illustrated in Fig. 1 is particularly suitable for binary signals in 8/10 modulation with a maximum run

length of 6 in the case of bit rates of up to approximately 50 mbit/s. The counter 24 monitors the run length of the incoming binary signal B'. The counter 24 is reset with every level transition of the input signal. A 1 can occur at the output QD, and thus the output QD can reset the counter 26 which forms the second stage, only when at least 8 clock pulses C occur between two level transitions of the input signal B'. Here the clock signal does not require to be synchronized with the input signal.

The counter 26 monitors the interval between the overshootings of the run length which are determined in the counter 24. The counting range of the counter 26 is adapted to the maximum value of this interval in the dead times of the signal. A 1 occurs at the output of the counter 26 in each case after 128 pulses from the output of the NOR gate 25 unless a resetting occurs in the meantime due to the overshooting of a run length. These resettings occur at sufficiently short intervals during the dead times of the signal so that the control quantity G, which is produced at the output 30 and indicates the useful signal or the interference signal, remains at zero. As also explained with reference to Fig. 2, the control quantity G can effect a desired switch-over between operation for a useful signal and operation for a pure interference signal. The maximum number of clock pulses C allowed between two run length overshootings here amounts to approximately $4 \times 128 = 512$ as the counting pulse for the counter 26 is obtained from the second flip-flop of the counter 24.

In the case of a useful signal which is substantially free of interference, the run length can no longer attain the value 8. Then a 1 occurs at the output 30 of the counter 26 and the gate 25 is disabled so that this state is maintained and can be ended only by the resetting of the counter 26 as a result of the overshooting of a run length. The signal

G=1 ensures that the forwards/backwards counter 16 in Fig. 2 operates and the centre frequency of the oscillator 1 is continuously set at the optimum value.

Each overshooting of the run length signifies that the instantaneous signal is unsuitable for adjusting the frequency of an oscillator. Therefore the adjustment is immediately interrupted by the resetting of the counter 26 and continued again only when satisfactory signal conditions have been established as described.

Fig. 2 illustrates an application of the circuit 23 illustrated in Fig. 1 for a known PLL circuit with counting phase discriminator in accordance with DE-OS 36 34 751. With the aid of the exclusive-OR gate 5 and the delay element 4 a narrow pulse B' is produced from each level transition of the binary input signal A. The flip-flop 15 likewise generates pulses B' of a specific breadth. It serves merely as delay time compensation for the flip-flop 6 which itself serves to generate a switch-over voltage Q. The switch-over voltage causes the pulses B to be fed either to the output of the gate 8 or 9. It is dependent upon whether the pulse B commences before or after the falling flank of the output voltage C of the VCO oscillator 1.

The output voltage E of the gate 8 and the inverted output voltage F of the gate 9 are added with the aid of the resistors 12 and 13 in order to produce the control voltage UR. The network 3 effects a low-pass filtering of UR. Via the amplifier 14, UR is fed to the oscillator 1 as control voltage UR'. The level of the control voltage, and thus the centre frequency of the oscillator 1, are determined by the output voltage Uo of the D/A converter 17. The input signal for the D/A converter 17 is supplied by the forwards/backwards counter 16. The latter obtains its counting pulses via the frequency dividers 18 and 19 unless

the gates 21, 22 are disabled. The circuit 23 for the recognition of the useful signal causes the gates 21 and 22 to be open only when the binary input signal A is a useful signal.

In the case of a binary useful signal A, the level transitions occur more frequently at intervals of whole-number multiples of the bit duration. When the frequency dividers 18 and 19 are identical, U_0 changes until the numbers of pulses at the outputs of the gates 8 and 9 are on average identical. This means, however, that the increases in level transitions, indicated for example by the eye pattern, are disposed symmetrically around a respective level transition of the output voltage C of the oscillator 1.

In the case of equal-length half-waves of the voltage C, the other level transition must then be located at the centre of the eye and thus be suitable for the fault-free reading of the binary input signal. The reading of the signal A here takes place with the aid of the positive flank of C in the flip-flop 20.

Claims

1. A method of generating a control quantity (G), which indicates a useful signal, from a binary signal sequence with alternating useful signals and disturbance signals, wherein the control quantity (G) indicates with a first value (1) that a binary useful signal is present and indicates with a second value (0) that a binary disturbance signal, generated during a signal drop-out as a result of amplification and delimitation, is present, wherein in the case of the useful signal the number of directly consecutive equivalent bits falls within a given range, characterised in that the number of directly consecutive, equivalent bits of the signal sequence (A) is measured and following an overshooting of the upper limit of the given range the control quantity (G) is generated with the second value (0), and that the control quantity (G) is reset to the first value as soon as the interval of time between two overshootings of the given range exceeds a predetermined value.

2. A circuit for the implementation of the method claimed in Claim 1, characterised in that a first counter (24) is provided for consecutive equivalent bits of the signal and a second counter (26) is provided for the interval of time between the overshootings determined in the first counter (24), that an output (QB) of the first counter (24) is connected to the first input of a NOR-gate (25), the output of which is connected to the input of the second counter (26) and the output (30) of which is connected to the second input of the NOR-gate (25), and that the first counter (24) is reset with each level transition of the binary signal or is preset at a specific state, and the second counter (26) is reset as soon as the first counter (24) reaches a predetermined state.