

Description

This invention relates to a power factor input control for an induction motor incorporating a reduced voltage starting capability.

Applicant's U.S. Patent No. 4 052 648 discloses a power reduction system for induction motors in which the operating power factor of a motor is monitored, and the effective voltage input to the motor is controlled as a function of the difference between a commanded power factor signal and the operating power factor. That document shows a power factor control system for an A.C. induction motor including current sampling means in circuit with at least one phase winding of said motor for providing an A.C. output signal representative of the timing of alternating current through said winding; voltage sampling means adapted to sense the voltage of an electrical input applied to said winding for providing an output signal representative of the timing of alternating current voltage across said winding; and phase detection means responsive to the outputs of said current sampling means and said voltage sampling means for providing an output which varies in accordance with the difference in phase between said current and voltage. Applicant's European patent application published in Bulletin 82/20 under No. 0051903 (Art. 54(3)) discloses a power factor type control system particularly adapted for three-phase induction motors. From EP-A-51903 it is also known to combine the outputs of the phase detection means.

In addition to minimizing motor power consumption during normal running conditions, a second area of concern is that of current surges which occur when a motor is first turned on. These surges can amount to five to eight times the normal operating current, and are both wasteful of electrical power and can contribute to excessive load surcharges being borne by electrical users. While discrete starting circuits have been employed which ideally gradually apply a starting voltage, it has been found that in some instances these circuits fail to provide a smooth start-up, and not infrequently there may occur significant motor vibrations during at least a portion of the start-up interval.

It is the object of this invention to provide a single control system which both regulates power usage during normal running of a motor and provides for a graduated turn-on of motor voltage without the attendant problem of motor vibration. It is a particular object of the invention to provide a system of this category for a three-phase motor where graduated voltage starting circuits are most frequently used.

According to the present invention signal means provide a control signal comprising an increasing signal followed by a fixed level signal, the latter comprising a power factor command signal and there is provided control means with elements connected in series with said motor winding, and responsive to the combined outputs of said phase detection means and signal means

for varying the duration of "on" time of each cycle of input power to said winding as an inverse function of the output of said phase detection means and as a direct function of the output of said signal means; whereby a gradually increasing power input is applied to said motor during a selected starting interval and thereafter the motor is controlled by said fixed level power factor command signal.

The motor to be controlled may be a three-phase motor with three windings each with a series connected thyristor as the element of the control means.

In a preferred embodiment the signal means initially block the application of the normal or "run" power factor command signal, and a ramp signal generator provides the increasing, with time, voltage in place of that command signal. This increase in voltage is of an amplitude and rate which will effect a graduated turn-on of the thyristor(s) of the motor circuit, effecting a full turn-on in a selected period of typically 5 to 30 seconds. A comparator examines the ramp voltage, and when the ramp voltage has risen sufficiently to effect a full turn-on of the thyristors and full motor operating speed, the comparator provides a signal which unblocks the normal power factor command signal, enabling the turn-on of a thyristor or thyristors to thereafter be determined by motor loading in a conventional manner for a power factor type controller.

Brief Description of the Drawings

Figure 1 is an electrical schematic diagram of an embodiment of the invention;

Figure 2 is an electrical schematic diagram of the phase detectors employed in the embodiment of the invention shown in Figure 1;

Figure 3 consists of a series of waveforms illustrative of the operation of the phase detector shown in Figure 2;

Figure 4 consists of series of waveforms illustrating the generation of triggering pulses in accordance with the circuitry shown in Figure 1.

Detailed Description of the Preferred Embodiment

Referring initially to Figure 1, a three phase induction motor 10 is powered through thyristor or SCR (silicon control rectifier) devices 12, 14, and 16 from a three phase power line, typically providing 220 or 440 volts, 60 cycle, alternating current to terminals A, B, and C. One phase of such a signal is illustrated by voltage waveform a of Figure 3. As the SCR devices provide for conduction only in one direction, a diode 18 is connected across each SCR and poled for opposite direction conduction. Current is sampled by current sampling transformers 26, 28, and 30, shunted by resistors 20, 22, and 24, each of these resistors being connected in series with an input to motor 10. Transformers 26, 28, and 30 are individually connected across one of these resistors (via a primary winding, as shown), and with one secondary terminal grounded, the other

secondary terminal provides a discretely phased current signal output (as shown in waveform c of Figure 3). Terminal X is associated with phase A, terminal Z is associated with phase C, and terminal Y is associated with phase B. A powder factor signal inversely proportional to the current-voltage phase differential of each of the three phase inputs is obtained, separately, by phase detectors 32, 34, and 36. Phase detector 32 receives a current responsive signal sample from terminal Z representative of the C phase current, and a voltage signal from transformer 38 representative of the A—C phase voltage, and provides a first phase detected output at terminal 40. Phase detector 34 receives a sample from terminal Y representative of the B phase current and a C—B phase voltage sample from transformer 42, and provides a second phase detected output at terminal 40. Phase detector 36 receives a phase A current signal sample from terminal X and a B—A phase voltage sample from transformer 44, and provides a third phase detection signal at terminal 40. The three signals, designated P_1 , P_2 , and P_3 , respectively, from the three phase detectors are shown in waveforms f and g of Figure 3.

The phase detectors are identical; one is shown in Figure 2. It includes two conventional squaring circuits. One is voltage square wave shaper 50, which provides through resistor 52 a rectangular wave (waveform b of Figure 3) responsive to the input voltage (waveform a of Figure 3). The second one is current square wave shaper 56, which provides through resistor 54 a rectangular wave (waveform d of Figure 3) representative of the negative half cycle of input current (waveform c of Figure 3). The outputs of the two wave shaping circuits are combined through resistors 52 and 54. Diode 60 passes only the positive portion of each output to terminal 40, which is common to the outputs of all three phase detectors. Waveform e illustrates the combination process showing the waveform of a single phase detector as it would appear without diode 60, which diode eliminates the negative portions of the waveforms. Significantly, in the detection process, each phase detector produces a pulse (e.g., P_1 from detector 32, P_2 from detector 34, and P_3 from detector 36) which is, in effect, turned "on" by the leading or rising edge of voltage waveform b and turned "off" by the trailing edge of waveform d. Thus, the width of pulse P_1 (it has a constant amplitude) tends to increase with an increase phase angle between current and voltage (thus decreased power factor) and decrease in width with decreased phase angle (and thus increased power factor).

Assuming as indicated that pulse P_1 represents the output of phase detector 32, waveforms f and g illustrate the relative time presence of output pulses P_2 and P_3 from phase detectors 34 and 36, respectively. As the outputs are brought together at terminal 40, waveform g of Figure 3 illustrates the combined signals at this point. This composite becomes the basic feedback control signal, and as will be noted, this is a signal of pulses of a

repetition rate of 180 Hz. This is in contrast to previous circuit approaches wherein a single phase detected output (from one of the three phases) is employed, which would, of course, have been either at 60 Hz or 120 Hz rate, depending upon whether a half or full wave detection was employed.

The next step in accordance with this invention is to effect a conditioning of the control signal wherein its direct current characteristic must be compatible with the SCR trigger circuitry and still have a frequency response up to on the order of 20 Hz. The control signal is applied to the inverting input of operational amplifier 64 of signal conditioner or integrating circuit 66, together with a power factor command signal supplied through resistor 68 and 69 from potentiometer 70. Potentiometer 70 is biased negatively to provide a difference or subtraction signal with respect to the positive signal as developed at the outputs of the phase detectors. Signal conditioning is effected by an inverse feedback network consisting of two circuits, one being capacitor 72 connected between the output and inverting input of operational amplifier 64, and the other consisting of a series combination of capacitor 74 and resistor 76 connected between these two points. The feedback network is basically an integrative or lag one. The combination of resistor 76 (approximately 15,000 ohms) and capacitor 74 (approximately 5 MFD) is initially effective (at 0 frequency) to commence providing a lag effect. At about 2 Hz, the lag state commences to diminish as the value of resistor 76 commences to have a dominant effect over capacitor 74. Then at about 20 Hz, capacitor 72 (approximately .68 MFD) commences to be effective to again impose a pronounced lag effect. The resulting signal is a relatively smooth signal representing the integral of the composite outputs of the phase detectors less the command signal. The signal, as used, is represented by the sample signal waveforms S_1 and S_2 as shown in Figure 4. It is important that while the signals have a relatively smooth and constant level, approximating the average signal value present, the signal must be responsive to signal changes incident to changes in motor loading, typically calling for a signal response upward to approximately 20 Hz. This is achieved by the circuitry as shown.

The circuitry thus far described was designed to develop a control signal for regulating the input power to motor 10 once the motor was started. The present invention is particularly directed to developing a signal for controlling the application of power to motor 10 during the period from the instant when power is turned "on" for a discrete selected interval of typically 5 to 30 seconds, during which the motor will have increased to operating speed. The purpose of this invention, as described above, is to prevent abrupt surges in input current which are not necessary for starting the motor, without accompanying instabilities. To accomplish this, circuitry is added which provides a substitute command signal to that provided by

potentiometer 70 during the start-up interval.

In order to insure that the substitute signal will be in place before any control signal is utilized, operational amplifier 64, which processes control signals, is initially disabled for approximately 100 milliseconds. As operational control signals are applied to the inverting input of operational amplifier 64, and are negative going to provide turn-on signals for the thyristors, a counter or disabling signal is applied to its non-inverting input. This is accomplished by applying a -15 volts to capacitor 77, which is in series with resistor 78, in turn connected between the non-inverting input of amplifier 64 and ground. The time constant of this circuit is adjusted to effect signal blocking for the period described.

As a means of preventing a possible turn-on signal from getting to the thyristors until operational amplifier 64 is disabled, the output of thyristor trigger oscillator 102 is initially blocked by NPN transistor 150 connected through output resistor 152 across the output of oscillator 102. Transistor 150 is initially turned "on", shorting the output of oscillator 102, by a declining ramp signal appearing across resistor 154 in series with capacitor 156 and a +15 volts source. Typically, the time constant provided by resistor 154 and capacitor 156 is such that transistor 150 would be essentially discharged in approximately 10 milliseconds, after which the blocking action would cease and transistor 150 would be turned "off", enabling a normal output from oscillator 102.

In addition to the precautions described above to insure that motor 10 will not turn "on" before the starting circuitry is operative, means are provided to prevent the application of a normal "run" command signal from potentiometer 70 during the entire starting interval. This is accomplished by connecting PNP transistor 158, collector-to-emitter across the output of potentiometer 70, between resistors 68 and 69. Transistor 158 is turned "on" by the application of power to the circuitry by a negative voltage applied to its base through resistor 160 from the output of operational amplifier 162. In this manner, the output of potentiometer 70 is effectively shorted out. The negative output state of operational amplifier 162 is effected by applying a greater negative bias on its non-inverting input than on its inverting input. The bias to the non-inverting input is a fixed bias, being a selected fraction of -15 volts as provided by a voltage divider comprising resistors 164 and 166 and connected across the -15 volts as shown. Initially, the voltage applied to the inverting input of operational amplifier 162 is zero, the initial output of operational amplifier 182, and thus the potential on the non-inverting input of operational amplifier 162 prevails.

Potentiometer 168, through resistor 170, provides an initial starting level negative signal to terminal 172 where it is added to a negative going, start-up, ramp signal supplied from the output of starting ramp generator 174 through resistor 176.

NPN transistor 178 is connected emitter-to-collector between terminal 172 and ground and

blocks an interfering effect from a starting signal after the starting sequence. Transistor 178 is controlled by an output through resistor 180 from operational amplifier 162, and is initially held "off" during the starting sequence by the negative output of operational amplifier 162.

Starting ramp generator 174 is a conventional integrator comprising operational amplifier 182 and a capacitor 184 connected from its output to its inverting input. A selected positive bias is obtained from potentiometer 186, connected between the +15 volts terminal and ground. This bias is fed through input resistor 192 to the inverting input of operational amplifier 182. The result is that, upon the application of voltages to the circuit, there will initially occur at the output of operational amplifier 182 an essentially zero voltage which ramps down negatively at a selected rate determined by this bias and the time constant of capacitor 184 and input resistor 192 to achieve a desired rate of motor turn "on" signal. The negative going signal at the output of operational amplifier 182 is fed through resistor 176 to terminal 172 and there added to a voltage from potentiometer 168, fed through resistor 170. This signal is then applied through resistor 183 to terminal 40 and there summed with the operating power factor (or current-voltage phase angle) signal and applied to operational amplifier 64 to effect an increasing (negatively) control signal which gradually, over a typical period of 5 to 30 seconds, results in effective motor voltage to be raised to full voltage. The actual operational control effected by the control signal on the thyristors is discussed below.

The output of operational amplifier 182 is also applied, in this case, to the inverting input of operational amplifier 162; and when the output rises to a level which exceeds the level applied to the non-inverting input of operational amplifier 162, the output of the latter switches from a negative state to a positive state. This changed state is fed as a switching potential to transistors 178 and 158 to turn transistor 178 "on" and transistor 158 "off". The result is that transistor 178 prevents any further starting signal from appearing at terminal 172, and transistor 158 unblocks the output of potentiometer 70 to restore normal power factor control for "run" operation of motor 10.

It is significant that during the start-up cycle, although the normal power factor command signal from potentiometer 70 is disabled, the effective power factor signal, summed from phase detectors 32, 34, and 36, continues to be an effective control input. This combination overcomes the tendency of motor instabilities to occur, which is common with certain other types of motor start-up circuitry.

Actual thyristor triggering signals, whether during the start of run modes, are developed by the comparison of the control signal (e.g., S_1 and S_2 of Figure 4) output of operational amplifier 64 and ramp shaped signals r . A ramp signal for each phase is developed by one of conventional ramp generators 84, 86, and 88, responsive to A-C,

C—B, and B—A phase voltages from transformers 38, 42, and 44, respectively. The ramp outputs *r* of these generators are illustrated by solid line in waveforms *a*, *b*, and *c*, respectively, of Figure 4 and are separately applied to conventional comparators 90, 92, and 94, together with a control signal from operational amplifier 64. In operation, a comparator provides a pulse output when the level of the control signal, e.g., dashed line *S*₁ of Figure 4, intersects the leading edge of a ramp signal. Thus, with a control signal *S*₁ applied to the comparators, output pulses are produced as shown in waveforms *d*, *e*, and *f* of Figure 4. These pulses, which result in the triggering of the thyristors, occur one per cycle, and are thus representative of a half wave mode of operation. The relatively narrow triggering pulses shown as waveforms *d*, *e*, and *f* produce relatively short turn-on times for SCR devices 12, 14, and 16, and thus produce a relatively low RMS input voltage to motor 10. This state of operation will initially have been brought about by phase detectors detecting a downward shift in power factor (by an upward shift in current-voltage phase angle) occurring when motor loading is reduced. The resulting output signal of operational amplifier 64 will produce a motor RMS input voltage which brings about an equilibrium between the commanded power factors determined by the bias output of potentiometer 70 and integrated output of the phase detectors.

The actual control of the current turn-on periods for the thyristors is effected by gates 96, 98, and 100, which pass high frequency signals responsive to the outputs of the comparators. These gates are electronic switches and function to gate the high frequency signal (e.g., 10 KHz) from oscillator 102 through the primary windings of transformers 104, 106, and 108 to the thyristors. Resistor 110 and diode 112 are connected in series across the primary of each transformer to suppress inductive voltages to a safe level consistent with the semi-conductive circuitry employed. The secondaries of transformers 104, 106, and 108 are connected in series with diode 114 between the gate and cathode of SCR devices 12, 14, and 16. The turn-on periods for the thyristors follow the periods of the pulse outputs of the comparators (as shown in waveforms *d—i*). The waveforms *g—i*, which are produced by control signal *S*₂, are illustrative of the turn-on periods for a moderately to heavily loaded motor in contrast to waveforms *d—f* which are indicative of a slightly loaded or unloaded motor.

During start-up, there would initially be provided a triggering output as illustrated by the narrow width pulses shown in waveforms *d—f*, and these would gradually widen until they were of a complete half cycle width as represented by waveforms *j—l* as the output of ramp generator 174 increases negatively. After the start-up period, and assuming there is a lightly loaded or unloaded motor, the system would adjust to a control as dictated by potentiometer 70 to provide, again, minimum length pulses as shown in

waveforms *d—f*. Alternately, if the motor were moderately loaded, the "after" pulse widths would be as shown by waveforms *g—i*.

While the invention is illustrated for a three-phase system, it is equally applicable in the manner described to a single-phase system. Further, while Figure 1 illustrates a three-phase system employing SCR devices as thyristors in a basically half wave control system, the invention is also applicable to full wave three-phase systems employing either triacs or SCR devices connected in anti-parallel.

Claims

1. A power factor control system for an A.C. induction motor (10) including current sampling means (26, 28, 30) in circuit with at least one phase winding of a said motor (10) for providing an A.C. output signal representative of the timing of alternating current through said winding; voltage sampling means (38, 42, 44) adapted to sense the voltage of an electrical input applied to said winding for providing an output signal representative of the timing of alternating current voltage across said winding; and phase detection means (32, 34, 36) responsive to the outputs of said current sampling means (26, 28, 30) and said voltage sampling means (38, 42, 44) for providing an output which varies in accordance with the difference in phase between said current and voltage; characterised by:

signal means (66, 174) for providing a control signal comprising an increasing signal followed by a fixed level signal, the latter comprising a power factor command signal; and

control means with elements (12, 14, 16) connected in series with said motor winding, and responsive to the combined outputs of said phase detection means and signal means for varying the duration of "on" time of each cycle of input power to said winding as an inverse function of the output of said phase detection means and as a direct function of the output of said signal means;

whereby a gradually increasing power input is applied to said motor during a selected starting interval and thereafter the motor is controlled by said fixed level power factor command signal.

2. A system as set forth in claim 1 wherein said motor (10) is a three-phase motor having three said windings, and there is a thyristor (12, 14, 16) in series with each said winding.

3. A system as set forth in claims 1 or 2, wherein said signal means includes means (705, 158, 162) for separately generating said power factor command signal in response to an initial turn-on of power to said system for initially, and for a selected period, blocking the supplying of said power factor command signal to said control means, and for that period supplying said increasing signal to said control means.

4. A system as set forth in claim 3 wherein said means for separately generating said power factor command signal includes means (70) for manually adjusting said last-named signal, and

C—B, and B—A phase voltages from transformers 38, 42, and 44, respectively. The ramp outputs *r* of these generators are illustrated by solid line in waveforms *a*, *b*, and *c*, respectively, of Figure 4 and are separately applied to conventional comparators 90, 92, and 94, together with a control signal from operational amplifier 64. In operation, a comparator provides a pulse output when the level of the control signal, e.g., dashed line *S*₁ of Figure 4, intersects the leading edge of a ramp signal. Thus, with a control signal *S*₁ applied to the comparators, output pulses are produced as shown in waveforms *d*, *e*, and *f* of Figure 4. These pulses, which result in the triggering of the thyristors, occur one per cycle, and are thus representative of a half wave mode of operation. The relatively narrow triggering pulses shown as waveforms *d*, *e*, and *f* produce relatively short turn-on times for SCR devices 12, 14, and 16, and thus produce a relatively low RMS input voltage to motor 10. This state of operation will initially have been brought about by phase detectors detecting a downward shift in power factor (by an upward shift in current-voltage phase angle) occurring when motor loading is reduced. The resulting output signal of operational amplifier 64 will produce a motor RMS input voltage which brings about an equilibrium between the commanded power factors determined by the bias output of potentiometer 70 and integrated output of the phase detectors.

The actual control of the current turn-on periods for the thyristors is effected by gates 96, 98, and 100, which pass high frequency signals responsive to the outputs of the comparators. These gates are electronic switches and function to gate the high frequency signal (e.g., 10 KHz) from oscillator 102 through the primary windings of transformers 104, 106, and 108 to the thyristors. Resistor 110 and diode 112 are connected in series across the primary of each transformer to suppress inductive voltages to a safe level consistent with the semi-conductive circuitry employed. The secondaries of transformers 104, 106, and 108 are connected in series with diode 114 between the gate and cathode of SCR devices 12, 14, and 16. The turn-on periods for the thyristors follow the periods of the pulse outputs of the comparators (as shown in waveforms *d—i*). The waveforms *g—i*, which are produced by control signal *S*₂, are illustrative of the turn-on periods for a moderately to heavily loaded motor in contrast to waveforms *d—f* which are indicative of a slightly loaded or unloaded motor.

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waveforms *d—f*. Alternately, if the motor were moderately loaded, the "after" pulse widths would be as shown by waveforms *g—i*.

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signal means (66, 174) for providing a control signal comprising an increasing signal followed by a fixed level signal, the latter comprising a power factor command signal; and

control means with elements (12, 14, 16) connected in series with said motor winding, and responsive to the combined outputs of said phase detection means and signal means for varying the duration of "on" time of each cycle of input power to said winding as an inverse function of the output of said phase detection means and as a direct function of the output of said signal means;

whereby a gradually increasing power input is applied to said motor during a selected starting interval and thereafter the motor is controlled by said fixed level power factor command signal.

2. A system as set forth in claim 1 wherein said motor (10) is a three-phase motor having three said windings, and there is a thyristor (12, 14, 16) in series with each said winding.

3. A system as set forth in claims 1 or 2, wherein said signal means includes means (705, 158, 162) for separately generating said power factor command signal in response to an initial turn-on of power to said system for initially, and for a selected period, blocking the supplying of said power factor command signal to said control means, and for that period supplying said increasing signal to said control means.

4. A system as set forth in claim 3 wherein said means for separately generating said power factor command signal includes means (70) for manually adjusting said last-named signal, and



said signal means includes ramp signal generating means (174) for providing said increasing signal to said control means.

5. A system as set forth in claim 4 wherein said means for initially blocking the supplying of said power factor command signal includes means (162) responsive to said ramp generating means (174) for unblocking the supplying of said power factor command signal to said control means upon said increasing signal increasing to a selected value.

6. A system as set forth in claim 5 wherein said signal means includes means (168) for providing a selected initial minimum level for said increasing signal, whereby at least a minimum starting control signal is applied to said control means.

7. A system as set forth in claim 2 and wherein the control means includes means (150) for blocking an operating signal to one of the thyristors until said signal means provides a signal to said control means.

Revendications

1. Système de commande de facteur de puissance pour moteur à induction en courant alternatif (10) comportant un moyen d'échantillonnage de courant (26, 28, 30) dans un circuit avec au moins un enroulement de phase du moteur (10) pour fournir un signal de sortie en courant alternatif représentatif du minutage du courant alternatif dans l'enroulement; un moyen d'échantillonnage de tension (38, 42, 44) destiné à détecter la tension d'une entrée électrique appliquée à l'enroulement afin de fournir un signal de sortie représentatif du minutage de la tension du courant alternatif aux bornes de l'enroulement; et un moyen de détection de phase (32, 34, 36) répondant aux sorties du moyen d'échantillonnage de courant (26, 28, 30) et au moyen d'échantillonnage de tension (38, 42, 44) pour fournir une sortie qui varie en conformité avec la différence de phase entre le courant et la tension, caractérisé par:

— un moyen de signal (66, 174) pour fournir un signal de commande comprenant un signal croissant suivi d'un signal de niveau fixe, ce dernier comprenant un signal d'ordre pour facteur de puissance; et

— un moyen de commande avec des éléments (12, 14, 16) connectés en série avec l'enroulement du moteur, et répondant aux sorties combinées du moyen de détection de phase et du moyen de signal pour faire varier la durée du temps "d'application" de chaque cycle de la puissance d'entrée à l'enroulement en fonction inverse de la sortie du moyen de détection de phase et en fonction directe de la sortie du moyen de signal;

— d'où il résulte qu'une entrée de puissance augmentant progressivement est appliquée au moteur pendant un intervalle de démarrage sélectionné, et ensuite le moteur est commandé par le signal d'ordre pour facteur de puissance de niveau fixe.

2. Système selon la revendication 1, où le

moteur (10) est un moteur triphasé ayant trois desdits enroulements, et un thyristor (12, 14, 16) est monté en série avec chaque enroulement.

3. Système selon la revendication 1 ou la revendication 2, où le moyen de signal comprend un moyen (105, 158, 162) pour générer séparément le signal d'ordre pour facteur de puissance en réponse à une application initiale de puissance au système, pour initialement, et pendant une période sélectionnée, bloquer la fourniture du signal de commande pour facteur de puissance au moyen de commande, et pendant cette période, fournir le signal croissant au moyen de commande.

4. Système selon la revendication 3, où le moyen pour générer séparément le signal de commande pour facteur de puissance comprend un moyen (70) pour régler manuellement le signal cité en dernier, et le moyen de signal comprend un moyen générateur (174) de signal de rampe pour fournir le signal croissant au moyen de commande.

5. Système selon la revendication 4, où le moyen pour bloquer initialement la fourniture du signal d'ordre pour facteur de puissance comprend un moyen (162) répondant au moyen générateur de rampe (174) pour débloquer la fourniture du signal d'ordre pour facteur de puissance au moyen de commande lors de l'augmentation du signal croissant à une valeur sélectionnée.

6. Système selon la revendication 5, où le moyen de signal comprend un moyen (168) pour fournir un niveau minimum initial sélectionné pour le signal croissant, d'où il résulte qu'au moins un signal de commande de démarrage minimum est appliqué au moyen de commande.

7. Système selon la revendication 2, où le moyen de commande comprend un moyen (150) pour bloquer un signal de fonctionnement appliqué à l'un des thyristors jusqu'à ce que le moyen de signal fournisse un signal au moyen de commande.

Patentansprüche

1. Leistungsfaktor-Regelsystem für einen Wechselstrom-Induktionsmotor (10) mit einer Stromabtasteinrichtung (26, 28, 30) in einer Schaltung mit zumindestens einer Phasenwicklung des Motors (10) zur Lieferung eines Wechselstrom-Ausgangssignales, welches für die zeitlich richtige Abstimmung (timing) des Wechselstromes durch diese Wicklung kennzeichnend ist, mit einer Spannungsabtasteinrichtung (38, 42, 44), welche die Spannung eines elektrischen Eingangssignales fühlen oder abtasten kann, welches an die Wicklung angelegt ist, um ein Ausgangssignal zu liefern, welches für die zeitlich richtige Abstimmung (timing) der Wechselstromspannung an der Wicklung kennzeichnend ist und mit einer Phasendetektoreinrichtung (32, 34, 36), welche ansprechbar ist auf die Ausgangssignale der Stromabtasteinrichtung (26, 28, 30) und der Spannungsabtasteinrichtung (38, 42, 44) um ein Aus-



(16)

gangssignal zu liefern, welches in Übereinstimmung mit der Differenz in der Phase zwischen dem Strom und der Spannung variiert gekennzeichnet durch:

eine Signaleinrichtung (66, 174) zur Lieferung eines Regelsignales, umfassend ein ansteigendes Signal, welches durch ein festes Pegelsignal erfolgt wird, wobei das letztere ein Leistungsfaktor-Befehlssignal aufweist und

eine Regeleinrichtung mit Elementen (12, 14, 16) die in Serie mit der Motorwicklung angeordnet sind und auf die kombinierten Ausgangssignale der Phasendetektoreinrichtung und der Signaleinrichtung ansprechbar sind, um die Dauer der "Ein"-Zeit jedes Zyklus der Eingangsleistung für die Wicklung als eine inverse Funktion des Ausgangssignals der Phasendetektoreinrichtung und als eine direkte Funktion des Ausgangssignals der Signaleinrichtung zu ändern, wodurch ein graduell ansteigendes Leistungseingangssignal an den Motor während eines ausgewählten Startintervalles angelegt wird, wonach der Motor durch das feste Pegelleistungsfaktor-Befehlssignal geregelt wird.

2. System nach Anspruch 1, dadurch gekennzeichnet, daß der Motor (10) ein Drei-Phasen-Motor ist mit drei Wicklungen und daß ein Thyristor (12, 14, 16) in Serie mit jeder Wicklung vorgesehen ist.

3. System nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die Signaleinrichtung eine Einrichtung (705, 158, 162) aufweist, um getrennt das Leistungsfaktor-Befehlssignal auf ein Anfangseinschalten der Leistung an das System zu erzeugen, um am Anfang und für eine ausgewählte Periode die Lieferung des Leistungsfaktor-

Befehlssignals an die Regeleinrichtung zu blockieren und um für diese Periode das ansteigende Signal zur Regeleinrichtung zu liefern.

4. System nach Anspruch 3, dadurch gekennzeichnet, daß die Einrichtung zum getrennten Erzeugen des Leistungsfaktor-Befehlssignals eine Einrichtung (70) zum manuellen Einstellen des letztgenannten Signales umfaßt und daß die Signaleinrichtung eine Rampensignal-Erzeugungseinrichtung (174) zur Lieferung des ansteigenden Signales an die Regeleinrichtung aufweist.

5. System nach Anspruch 4, dadurch gekennzeichnet, daß die Einrichtung zum anfänglichen Blockieren der Lieferung des Leistungsfaktor-Befehlssignales eine Einrichtung (162) aufweist, die auf die Rampenerzeugungseinrichtung (174) anspricht, um die Lieferung des Leistungsfaktor-Befehlssignales an die Regeleinrichtung zu entblocken bzw. freizugeben, und zwar wenn das ansteigende Signal auf einen ausgewählten Wert ansteigt.

6. System nach Anspruch 5, dadurch gekennzeichnet, daß die Signaleinrichtung eine Einrichtung (168) zur Lieferung eines ausgewählten Anfangs-Minimum-Pegels für das ansteigende Signal aufweist, wodurch zumindest ein Minimum-Start-Regelsignal an die Regeleinrichtung angelegt wird.

7. System nach Anspruch 2, dadurch gekennzeichnet, daß die Regeleinrichtung eine Einrichtung (150) zum Blockieren eines Betriebssignales für eine der Thyristoren aufweist, bis die Signaleinrichtung ein Signal an die Regeleinrichtung liefert.

