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MEANS AND METHOD FOR STABILIZING POLYCRYSTALLINE SEMICONDUCTOR SURFACES

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates in general to means and methods for stabilizing the properties of polycrystalline semiconductor layers and, more particularly, to means and method for controlling surface hillock growth in polycrystalline semiconductor layers during high temperature processing.

Background Art

Electronic devices using polycrystalline semiconductors often exhibit problems associated with the formation of surface roughness in the poly. For example, when un-capped layers of polysilicon are heated, such as during activation or redistribution of a dopant, it is observed that bumps, hillocks, and/or spikes form on the surface of the poly. These uneven surface features, collectively referred to herein as hillocks, can degrade the integrity of any subsequent layers placed on top of the poly, as for example dielectrics used for passivation or multi-layer interconnections.

It is known that hillock formation may be avoided in polysilicon, for example, by capping the poly layer prior to heating. Capping consists of applying a covering layer of another material such as silicon dioxide or silicon nitride. However, under certain circumstances it is not practical to use a cap layer over the poly, and in these situations hillock formation has heretofore been unavoidable. Examples of such situations are when a high temperature processing step must be used prior to

providing the cap layer, or when the insulating cap layer would interfere with making good electrical contact to the poly layer, or where the cap layer would interfere with subsequent processing steps. Thus, a need continues to exist for improved means and methods for overcoming hillock formation and other problems arising in connection with polycrystalline semiconductor layers.

Accordingly, it is an objective of the present invention to provide improved means and methods for preventing hillock formation in the surface of polycrystalline semiconductor layers during heat treatment.

It is an additional object of the present invention to prevent hillock formation in polycrystalline semiconductor layers without using a cap layer.

It is a further object of the present invention to prevent hillock formation in polycrystalline semiconductor layers without using a surface insulating layer.

As used herein the words "dopant" or "doping" are intended to refer to the class of impurities which provide substantial number of shallow donor or acceptor levels in the semiconductor so as to substantially alter the conductivity of the material. In the case of silicon materials, examples of this class of dopants are arsenic, boron, phosphorous, antimony, aluminum, gallium, and indium, but not oxygen or nitrogen. Those of skill in the art will understand that other such dopant elements exist for use in silicon and other semiconductor materials. As used herein the words "high temperature" are intended to refer to temperatures where the phenomena of interest are proceeding at a rate significant compared to the time periods of interest. For example, for dopant migration or oxidation of silicon, this is generally above about 1000 degrees C. Those of skill in the art will understand that

different temperatures apply for different phenomena and materials.

According to the present invention in one aspect thereof a method for stabilizing polycrystalline semiconductor layers, comprising: providing a substrate; forming a polycrystalline semiconductor layer on said substrate; then in either order, implanting oxygen into the surface of said polycrystalline semiconductor layer to a dose in the range of 10^{15} ions/cm^2 to 5 x 10^{16}ions/cms^2. and implanting a conductivity altering dopant into said polycrystalline semiconductor layer; and thereafter, heating said polycrystalline semiconductor layer to electrically activate said dopant.

According to the present invention in a further aspect thereof a method for preventing hillock formation in polycrystalline semiconductor layers comprising: providing a substrate having thereon a polycrystalline semiconductor layer with an exposed surface; implanting oxygen into said exposed surface to a dose in the range of 10^{15} oxygen ions/cm^2 to 5 x 10^{16} oxygen ions/cm^2 at energy in the range about 10-50 keV; and thereafter heating said layer.

According to the present invention in a yet further aspect thereof a method for preventing hillock formation in polycrystalline semiconductor layers comprising: providing a substrate having thereon a polycrystalline semiconductor layer with an exposed surface; implanting oxygen into said exposed surface at an energy in the range of 10-50 keV to a peak concentration within the polycrystalline semiconductor layer in the range of 7 x 10^{19} atoms/cm^3 to 3 x 10^{20} atoms/cm^3; and thereafter heating said layer.

According to the present invention in a yet still further aspect thereof a semiconductor structure, comprising: a polycrystalline semiconductor layer having a first surface; and an ion implanted oxygen region in said layer and extending below said first surface, wherein said ion implanted oxygen region has an peak oxygen concentration located below said surface and having a value in the range 7 x 10^{10} oxygen atoms/cm^3 to 3 x 10^{20} oxygen atoms/cm^3.

According to the present invention in an even further aspect thereof a semiconductor structure comprising:

a polycrystalline semiconductor layer having a first surface; and an oxygen doped region in said layer adjacent said first surface and having a peak concentration located below said first surface, wherein said oxygen dopes region is prepared by ion implanting oxygen into said surface to a dose in the range of 10^{15} oxygen ions/cm^2 to of 10^{15} 5 x 10^{16} oxygen ions/cm^2 and then heating said layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs 1A-C show simplified schematic cross-sectional views of a portion of a semiconductor device containing a polycrystalline region and indicating the surface roughening phenomenon observed following uncapped high temperature heat treatment.

Figs 2A-C show simplified schematic cross-sectional views of a semiconductor device similar to Figs 1A-C, but according to the present invention wherein hillock formation is prevented.

Figs 3A-C show SEM photomicrographs at different magnifications of portions of a polysilicon layer, with and without oxygen implantation, and after high temperature heat treatment.

DETAILED DESCRIPTION OF THE DRAWINGS

For purposes of explanation, the device structures and methods herein are shown for the case of silicon based semiconductor devices and polycrystalline silicon layers. However, those of skill in the art will understand that these means and methods apply to other semiconductor substrates and other polycrystalline semiconductors, and are presented merely as an aid to understanding and not intended to be limiting, and that other materials may also be used.

In FIGS. 1-2, unless otherwise noted, implanted or doped regions of the poly are generally shown stippled, dielectric layers or regions are shown hatched, and single crystal regions or undoped poly regions are shown clear. Arrows at the boundaries of the dopant implanted regions in the poly are used to indicate the direction of migration of the dopant atoms in the poly during subsequent high temperature operations.

FIGS 1A-C show in simplified schematic cross-sectional form, a portion of a semiconductor device exhibiting hillock formation in a polysilicon layer. Device portion 29, which may be for example a MOSFET, comprises substrate 30, dielectric region 32, and superposed polycrystalline semiconductor region 33 having substantially smooth upper surface 33a. Implanted dopant ions 34 dope poly region 33 and portions 31 of substrate 30. However it is not essential that substrate 30 be doped and a MOSFET need not be formed. For example, dielectric 32 may cover the surface of substrate 31 while poly region 33 functions merely as a first layer interconnect running into the plane of the figure.

It is observed that if poly region 33 is left uncapped during subsequent heat treatment, as for example, during high temperature processing to activate dopant 34

and anneal the implant damage, that hillocks or bumps 35 form in the surface of region 33, i.e., originally smooth surface 33a changes into rough surface 33b. When rough surface 33b is subsequently covered, for example, with second dielectric 36 and second conductor layer 37, hillocks or bumps 35 degrade the integrity of portion 36a of layer 36 and amy also adversely affect step coverage of portion 37a of layer 37. This is undesirable.

These and other problems are overcome with the means and method of the present invention illustrated in FIGS. 2A-C and described more fully in connection with FIGS. 3A-C.

The problems illustrated in FIGS. 1A-C may be overcome by the means and method illustrated in connection with FIGS. 2A-C wherein device portion 59, similar to portion 29 of FIGS 1A-C, comprises substrate 60, doped regions 61, surface dielectric region 62 and superposed poly region 63. Portion 63b of poly region 63 has been implanted with dopant ions 65 either before or after formation of region 63a, but in FIG> 2A has not yet been subjected to any high temperature processing sufficient to cause grain boundary migration of dopant ions 65 in region 63 or hillock formation. Arrows 63d at dopant implant boundary 63c indicate the direction of movement of dopant ions 65 during high temperature processing. Portion 63a is formed at or immediately adjacent surface 63e of region 63. Portion 63a contains added oxygen, and is preferably formed by implantation of ions 64. Portion 63b containing dopant ions 65 has been illustrated as being placed relatively deeply in region 63 and below portion 63a. However, this is not essential. So far as preventing hillock formation is concerned, the location of doped portion 63b is not important. It is only important

that portion 63a be at or immediately adjacent exposed surface 63e.

It has been found that when oxygen ions, or mixtures thereof are implanted into surface portion 63a of region 63, that hillock formation is prevented during subsequent high temperature processing, as shown in Figs 6B-C. Accordingly surface 63e remains smooth and subsequently formed dielectric layer 66 and poly layer 67 are not disturbed. Portions 66a and 67a above surface 63e are not degraded by an hillock formation in region 63.

EXPERIMENTAL RESULTS

Polycrystalline silicon layers of about 0.6 microns thickness were formed on oxidized silicon wafers using LPCVD techniques well known in the art. The as-deposited films or layers had grains typically 0.02 microns in diameter. Accordingly, prior to heating the layers were about thirty grain sizes thick. After heating, grain sizes increased to about 0.2-0.6 microns. It was observed that if such films were heat treated without a cap layer for example heated from room temperature to a peak temperature of about 1150 degrees C and back to about temperature again in about 20-25 seconds, that the surface of the polysilicon layer was substantially roughened Hillocks, bumps, and spikes formed in what previously been a smooth polysilicon surface. The heating was carried out in a Rapid Thermal Annealing (RTA) apparatus, type IA-200 manufactured by Varian Associates, Gloucester, MA. This type of apparatus is capable of very rapid heating and cooling of semiconductor wafers, and unless otherwise note, was used for all of the high temperature operations carried out in connection with this invention.

The effective time at the peak temperature is estimated to be about one second. Similar hillock growth also occurs when slower heating methods are used. In general, hillock formation increases in severity as heating time and temperature are increased.

It was found that if the exposed surface of the polysilicon layer was implanted with oxygen to a dose far below that required to produce a surface oxide layer, that the tendency of the surface to erupt into hillocks on heating was substantially arrested.

Bare polysilicon layers were implanted with molecular oxygen (O_2^+) at about 60 keV energy to doses in the range 2.5 x $10^{14}/cm^2$ to 1 x $10^{15}/cm^2$. Molcular oxygen was used for convenience in selecting the energy. These implants are equivalent to providing twice the dose of atomic oxygen (O^+) at half the energy, i.e. 5 x 10^{14} to 2 x $10^{15}/cm^2$ to 30 keV. The low equivalent energy was desired in order to place the peak of the implanted oxygen distribution at or very close to the surface of the poly layer.

It is estimated that for a 30 keV equivalent energy implant, the peak of the implanted oxygen distribution lies about 0.06 microns below the poly surface. Since the implanted oxygen concentration falls off exponentially with distance on either side of the peak, the oxygen concentration at the surface in this case is expected to be about ten per cent of the peak value. These doses correspond to a peak concentration of about 7 x 10^{19} to 3 x 10^{20} oxygen atoms/cm^3, respectively, that is, to a peak oxygen concentration in the polysilicon of about 0.1% to 0.6%. The oxygen concentration in the silicon at the exposed poly surface is estimated to be about one tenth of the peak values, i.e.. about 0.01% to 0.06%. These

concentrations are far below that required to form a surface dielectric layer analogous to the cap layer used in the prior art.

FIG. 3A-C shows Scanning Electron Microscope (SEM) micrographs of various portions of the surface of a polysilicon layer at several magnifications, with and without implanted oxygen, after being subjected to the heating procedure described above known to produce hillock formation in un-capped poly layers. The size of the features visible in the micrographs may be judged by reference to the scale bars associated with each figure. The smooth appearing regions at the left of FIGS. 3A-B are the regions of the poly layer which had been oxygen implanted to a dose of 2×10^{15} ions/cm^2 at 30 keV equivalent. The rough appearing regions at the right of FIGS. 3A-B and in FIG. 3C had received no oxygen implant. It is readily apparent that hillock formation is substantially arrested in the portions of the poly layer which have been oxygen implanted.

Samples which had been implanted with a dose of 5×10^{14} ions/cm^2 at 30 keV equivalent showed only a marginal change in the propensity to form hillocks during uncapped heating. The lower the energy, the lower the dose which is likely to be effective in suppressing hillock formation since more of the implanted oxygen is close to the surface grain boundaries. Doses in the range of about 10^{15} to 5×10^{16} ions/cm^2 are believed to be useful with 2×10^{15} to 10^{16} ions/cm^2 being convenient. It is expected that the hillock prevention effect will increase with increasing dose, i.e., the layers will be able to withstand longer exposures to higher and higher temperatures. However, the resistivity of the surface region of the layers is also expected to increase with increasing dose. The presence of a high resistivity region next to or at the upper surface may

cause high contact or sheet resistance. This is generally not desirable. If a silicon implant is used to inhibit hillock formation, there is no risk of forming such an insulating layer. This is an advantage of using silicon implantation.

The energy of the implant should be adjusted to place the peak of the implanted oxygen just under the surface of the polycrystalline semiconductor layer. For polysilicon, 0+ energies in the range 10-50 keV are useful with 20-40 keV being convenient and about 30 keV being typical. Those of skill in the art understand how to vary implant energy in order to achieve different implant penetrations for different grain sizes, different target materials and different implant ions, and that different energies may be required for such different grains sizes, materials and implant ions in order to place the peak concentration of the hillock inhibiting atoms or ions adjacent to or within a diffusion length of the exposed surface of the polycrystalline semiconductor layer.

The stability of the oxygen implants was investigated by Auger Electron Spectroscopy on capped poly layers which had been implanted to 10^{16} ions/cm^2 at 200 keV. The implanted oxygen concentration versus distance from the poly surface was measured on as-implanted samples and on samples that had received high temperature treatments similar to that used to induce hillock formation. Within the accuracy of the measurement technique, no significant migration or spreading of the implanted oxygen distribution was apparent. The above described results indicate that the oxygen has, at most, migrated to the grain boundaries of the polycrystalline layer and precipitated there. It has not migrated throughout the poly layer. It is believed that the precipitation of implanted oxygen on the grain boundaries near the exposed

surface inhibits the grain-to-grain silicon transport that is necessary for formation of hillocks, and thus inhibits hillock growth. It is desirable that the peak of the implanted oxygen distribution be within about 0.1-0.2 microns of the surface for layers thicker than about one micron and within about the top 10-20% of the layer thickness for layers thinner than about one micron.

The oxygen precipitated on the grain boundaries is chemically bound and is therefore believed to permantently block silicon migration along the grain boundaries. Thus the result of implanting oxygen is different than for other materials, such as for example silicon, which merely amorphize the surface and do not form a chemically stable second phase at the grain boundaries. Accordingly, the hillock blocking effect of the oxygen is expected to be more resistant to annealing during high temperature processing and be more permanent as compared to mere amorphization of the poly surface.

The effect of oxygen implantation on the sheet resistance of the poly layers was measured for oxygen implant doses of 10^{14} to 10^{16} ions/cm^2 at 200 keV. The layers were arsenic doped after oxygen implantation to 5×10^{15} arsenic ions/cm^2 at an energy of 150 keV and then activated using the RTA technique at peak temperatures ranging from 1100-1200 degrees. The effective time at temperature was estimated to be about one second. The higher the activation temperature, the lower the resulting sheet resistance. The sheet resistance was measured using a standard four point probe. Such techniques are well known in the art. Some of the layers were annealed prior to oxygen implantation to increase the typical grain size from about 0.02 to 0.2 microns. Control samples without oxygen implantation were similarly doped.

The sheet resistances of the various oxygen free layers varied from about 62-125 ohms per square. Sheet resistance of otherwise identical layers receiving various oxygen doses were 62-130 ohms per square for a dose of 10^{14} ions/cm^2, 65-160 ohms per square for a dose of 10^{15} ions/cm^2, and 90-240 ohms per square for a dose of 10^{16} ions/cm^2. While the oxygen implants in these tests were deeper in the layers than those used for determining the hillock inhibiting effect, the results demonstrate that oxygen implants in the same dose range do not destroy the conducting nature of the polycrystalline silicon layers and that the arsenic doped poly-layers still have comparatively low resistance even after such oxygen implantation.

Those of skill in the art will understand that other dopants besides arsenic can be employed as the conductivity altering dopant. Further, those of skill in the art will understand that the principles taught herein apply to other semiconductor materials, such as for example, but not limited to, germanium and III-V materials. Accordingly, it is intended to include all such variations in the claims which follow.

CLAIMS

1. A method for stabilizing polycrystalline semiconductor layers, comprising:

providing a substrate;

forming a polycrystalline semiconductor layers on said substrate;

then in either order, implanting oxygen into the surface of said polycrystalline semiconductor layer to a doses in the range of 10^{15} ions/cm^2 to 5 x 10^{16} ions/cm^2, and implanting a conductivity altering dopant into said polycrystalline semiconductor layer; and

thereafter, heating said polycrystalline semiconductor layer to electrically activate said dopant.

2. The method of claim 1 wherein said forming step comprises forming on said substrate a polycrystalline semiconductor layer having a substantially smooth upper surface.

3. The method of claim 1 wherein said forming step comprises forming said polycrystalline semiconductor layer without heating to a temperature and for a time sufficient to roughen said surface.

4. A method for preventing hillock formation in polycrystalline semiconductor layers comprising:

providing a substrate having thereon a polycrystalline semiconductor layer with an exposed surface;

implanting oxygen into said exposed surface to a dose in the range of 10^{15} oxygen ions/cm^2 to 5 x 10^{16} oxygen ions/cm^2 at energy in the range about 10-50 keV; and

thereafter heating said layer.

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5. The method of claim 4 wherein said implanting step comprises implanting to a dose in the range of 2×10^{15} ions/cm^2 to 10^{16} ions/cm^2 at energies in the range about 20-40 keV.

6. The method for preventing hillock formation in polycrystalline semiconductor layers comprising:

providing a substrate having thereon a polycrystalline semiconductor layer with an exposed surface;

implanting oxygen into said exposed surface at an energy in the range of 10-50 keV to a peak concentration within the polycrystalline semiconductor layer in the range of 7×10^{19} atoms/cm^3 to 3×10^{20} atoms/cm^3; and

thereafter heating said layer.

7. A semiconductor structure, comprising: a polycrystalline semiconductor layer having a first surface; and

an ion implanted oxygen region in said layer and extending below said first surface, wherein said ion implanted oxygen region has a peak oxygen concentration located below said surface and having a value in the range 7×10^{19} oxygen atoms/cm^3 to 3×10^{20} oxygen atoms/cm^3.

8. The semiconductor structure of claim 7 wherein said ion implanted oxygen region has a concentration between said surface and the location of said peak concentration which is less than said peak concentration.

9. A semiconductor structure comprising: a polycrystalline semiconductor layer having a first surface; and

an oxygen doped region in said layer adjacent said first surface and having a peak concentration located below said first surface, wherein said oxygen doped region is prepared by ion implanting oxygen into said surface to a dose in the range of 10^{15} oxygen ions/cm^2 to of 5×10^{16} oxygen ions/cm^2 and then heating said layer.

10. The semiconductor structure of claim 9 wherein said oxygen dopes region has a concentration between said surface and the location of said peak concentration below said surface which is less than said peak concentration.