What is claimed:

1. A method for design based assessment of a device, comprising:

defining a plurality of patterns of interest utilizing design data of the device;

generating a design based classification database, the design based classification database including design data associated with each of the patterns of interest;

receiving one or more inspection results;

comparing the one or more inspection results to each of the plurality of patterns of interest in order to identify an occurrence of at least one of the patterns of interest in the inspection results;

determining yield impact of each pattern of interest utilizing process yield data;

monitoring a frequency of occurrence of each of the patterns of interest and the criticality of the patterns of interest in order to identify one or more process excursions of the device; and

determining a device risk level by calculating a normalized polygon frequency for the device utilizing a frequency of occurrence for each of the critical polygons and a criticality for each of the critical polygons, the critical polygons defined utilizing design data of the device.

2. The method of claim 1, wherein the plurality of patterns of interest are generated utilizing at least one of a failure analysis process, a design rule checking process, an optical rule checking process, or a process window qualification method.

3. The method of claim 1, wherein the process yield data comprises:

end-of-line process yield data.

4. The method of claim 1, wherein the receiving one or more inspection results comprises:

receiving one or more inspection results from a inspection system.

5. The method of claim 4, wherein the inspection system comprises:

at least one of a dark field inspection system or a bright field inspection system.

6. The method of claim 1, wherein the monitoring a frequency of occurrence of each of the patterns of interest and the criticality of the patterns of interest in order to identify one or more process excursions of the device comprises:

generating a Pareto chart configured to determine a ratio of actual defects to expected defects as a function of pattern type.

7. The method of claim 1, wherein the monitoring a frequency of occurrence of each of the patterns of interest and the criticality of the patterns of interest in order to identify one or more process excursions of the device comprises:

performing a statistical process control routine to the plurality of POIs in order to identify one or more process excursions, the one or more process excursions displaying a defect density above a predetermined defect density.

8. The method of claim 1, wherein the critical polygons of the design data are defined utilizing at least one of a design rule checking process, a failure analysis process, or a simulation process.

9. The method of claim 1, further comprising:

providing feedback to a user interface device indicative of a recommended action, wherein the recommended action is a function of the determined risk level for the device.

10. The method of claim 9, wherein the recommended action comprises:
substantially optimizing a design in order to reduce DFM defects.

11. The method of claim 9, wherein the recommended action comprises:
substantially optimizing a process specification.

12. A method for providing dynamic sampling utilizing critical defects, comprising:

identifying a plurality of critical pattern types on a wafer;

determining a device risk level utilizing a calculated risk level and frequency of occurrence for each of the identified critical pattern types;

identifying one or more relevant excursions of the device;

determining dynamic wafer selection in response to the identification of one or more device excursions; and

dynamically sampling at least some of the identified critical pattern types.

13. The method of claim 12, wherein the dynamically sampling at least some of the identified critical pattern types comprises:

sampling some of the critical pattern types based on a frequency of occurrence and a criticality of each of the critical pattern types.

14. The method of claim 12, wherein the dynamically sampling at least some of the identified critical pattern types comprises:

dynamically inspecting at least some of the identified critical pattern types using an inspection tool.

15. A method for providing risk assessment or yield correlation in a memory device, comprising:

defining a plurality of regions based on one or more functional areas of a device utilizing design data;

performing one or more inspection processes on the one or more defined regions;

identifying one or more dies of the one or more defined regions falling below a predetermined control limit utilizing inspection data from the one or more inspection processes; and

identifying regions impacting yield loss by comparing the one or more dies falling below the predetermined control limit to inline data for each of the regions.

16. The method of claim 15, wherein the one or more functional areas of the device comprise:

at least one of a main area of the device, a redundant memory area of the device, or a dummy area of the device.

17. The method of claim 15, wherein the one or more inspection processes comprise:

at least one of dark field inspection or bright field inspection.

18. A method for monitoring device processing using spatial analysis, comprising:

monitoring a process variation signature by inspecting one or more devices between one or more process steps;

associating one or more patterns of interest of the one or more devices with a monitored process variation using a design based classification process; and

identifying one or more equipment signatures using the one or more associated patterns of interest.

19. The method of claim 18, further comprising:

subtracting the identified one or more equipment signatures from a defect map of the device.

CLAIMS

1. An invention not claimed in any divisional application.