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1 **PRINTED CIRCUIT BOARD WITH SHIELDED CIRCUITRY**

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4 **FIELD OF THE INVENTION**

5 The present invention is related to printed circuit boards and
6 electromagnetic interference (EMI). In particular, the present invention is
7 related to printed circuit boards with shielding against electromagnetic
8 interference.

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10 **BACKGROUND OF THE INVENTION**

11 Printed circuit boards (PCB's), including rigid, flexible, single, double and
12 multilayer boards have found important uses in the semi-conductor and
13 electronic industry. A PCB typically contains metallized layers of electrical
14 circuitry or traces separated by dielectric material. Interconnections are
15 provided for electrical connection between the metallized layers. In certain
16 applications, such as audio-amplifiers, microphones and mobile telephones,
17 the electrical circuitry of the PCB generates an electromagnetic field which
18 interfere with the normal operation of other circuitries in the vicinity.

19 One conventional method of reducing EMI in circuitry embedded in PCB's
20 is to provide metal shield on the surfaces of the board. This shield may be
21 one or more metal plates mounted around the PCB, or a layer of metallic
22 coating plated directly onto the surface of the PCB. Another prior art method



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1 involves the plating of metallic traces internally within the inner layers of the
2 PCB adjacent the prescribed trace or traces for which EMI shielding is
3 needed.

4 Figures 1A to 1D show the traces and structures found in the prior art
5 PCB for internal EMI shielding. A simple six-layer PCB is shown with a metal
6 trace **20** in layer **L1-3** and another metal trace **22** in layer **L1-4**. These two
7 traces require EMI shielding. For ease of illustration, only the traces to be
8 shielded and the relevant shielding structures are shown in layers **L1-2** to
9 **L1-5**. Trace **20** is interconnected to trace **22** through metal-coated via **24**.
10 Two ground traces **26** and **28** are also plated in layer **L1-3** on the two
11 opposing sides of trace **20**. Ground trace **21**, connected to traces **26** and **28**
12 in layer **L1-3**, is provided for top shielding of trace **22**. Two other grounded
13 traces **30** and **32** are plated in **L1-4** on the two adjacent sides of trace **22**.
14 They are connected to trace **31**, which act as the bottom shield for trace **20**.
15 Ground trace **33** is provided in layer **L1-2** directly above metal trace **20** to
16 function as top shielding against EMI. Ground trace **35** is provided in layer
17 **L1-5** directly below metal trace **22** as bottom shield therefor. Between
18 metallic layers **L1-2**, **L1-3**, **L1-4** and **L1-5** are dielectric layers, denoted
19 as **L1-axb** where a and b indicate the layers directly above and below it
20 respectively. To provide partial EMI shielding at the dielectric layers,
21 conventional PCB boards are provided with vias **34a** and **34b** having a
22 coat of metal **36** thereon.

23 It is clear from the above description of the prior art that the shielding
24 provided within the PCB does not provide good EMI shielding, as there are
25 multiple gaps **38** between vias **34a** and **34b** that do not provide shielding.

1 SUMMARY OF THE INVENTION

2 It is therefore an object of the present invention to provide a PCB board
3 with improved internal EMI shielding.

4 Accordingly, the present invention provides PCB boards with in-board
5 EMI shielding in which a prescribed electrical circuitry within a PCB is
6 shielded from EMI by fabricating a uniform metal shielding enclosure
7 therearound. The shielded circuitry may be a single metal trace, a group of
8 interconnected traces in the same or different layers of the same PCB, or a
9 complete electrical circuitry spanning many different layers and locations
10 within the same PCB. Using the same technology, groups of electrical
11 circuitry that require isolation because of EMI may be fabricated together in
12 proximity, with each group shielded from the EMI of the others. The metal
13 shield contains a top shield in a layer above the circuitry, a bottom shield in a
14 layer below the circuitry, and side shields adjacent the circuitry.

15 According to one embodiment of the present invention, the side shields
16 are trenches with metal coating provided adjacent the prescribed circuitry.
17 The side trenches connect the top shield and the bottom shield without gaps.
18 Openings of the uniform metal shield are provided at the sites where the
19 circuitry connects to another circuitry within the same PCB board or with the
20 exterior.

21 In another embodiment, the side shields are solid walls provided
22 adjacent the prescribed circuitry. The walls are built using electroplating
23 and/or electroless plating as described in detail below. As with the metal
24 coated trenches, the solid walls connect the top shield and the bottom shield

1 to form a uniform enclosure around the prescribed circuitry, except for
2 openings where the prescribed circuitry connects to another circuitry within
3 the same PCB board or with the exterior. The present invention not only
4 provides complete shielding of a circuitry, but also gives substantial internal
5 space savings.

6 As used herein, a uniform metallic shield refers to the a complete
7 shield absent any non-metallic gaps within the side shields that connect the
8 top shield and the bottom shield.

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10 **BRIEF DESCRIPTION OF THE DRAWINGS**

11 Figure 1A is a perspective drawing of a piece of a conventional PCB with the
12 various layers indicated by dotted lines.

13 Figure 1B and 1C are cross section drawings along lines A-A' and B-B'
14 respectively of the same conventional PCB.

15 Figure 1D-1J are the art work of area E in layers L1-2, L1-2x3, L1-3, L1-3x4,
16 L1-4, L1-4x5 and L1-5 respectively of the PCB shown in Fig. 1 A to 1C.

17 Figure 2A is a perspective drawing of a part of a PCB according to the
18 present invention with the various layers shown.

19 Figure 2B and 2C are cross section drawings along lines C-C' and D-D'
20 respectively of the PCB shown in Fig.2A.

21 Figure 2D-2J are the art work of area F in layers L2-2, L2-2x3, L2-3, L2-3x4,
22 L2-4, L2-4x5 and L2-5 respectively of the PCB shown in Fig. 2A to 2C.

1 Figure 3A-3F show the steps of one method of producing an EMI shield
2 according to the present invention.

3 Figure 4A-4F show the steps of another method of producing another EMI
4 shield according to the present invention.

5 Figure 5A-H show the steps of yet another method of producing another EMI
6 shield according to the present invention.

7 Figure 6 is a perspective drawing of one interior part of a multilayer PCB
8 showing the metal shield for a multilayer electrical circuitry.

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10 DESCRIPTION OF THE INVENTION

11 Figure 2A-J show an example of a portion of a multi-layer PCB board
12 according to the present invention having metallized layers **L2-1**, **L2-2**,
13 **L2-3**, **L2-4**, and **L2-5**. Each of these layers are separated by dielectric
14 material, denoted as L2-axb, where a and b refer to the metallized layer
15 directly above and below it. For ease of illustration, only the relevant traces
16 to be shielded and the corresponding shielding structures are shown in the
17 internal metallized layers. In this example, traces **40** and **42**, provided in
18 layers **L2-3** and **L2-4** are the electrical circuitry that require EMI shielding.
19 Traces **40** and **42** are electrically connected by solid metallic interconnect
20 **44**. Ground shield **46a** is provided in layer **L2-2** directly above trace **40**,
21 and ground shield **46b** is provided in layer **L2-3** and directly above trace
22 **42**. Ground shields **46a** and **46b** together act as the top shield. Ground
23 shield **48a** is provided in layer **L2-4** directly below trace **40**, and ground

1 shield **48b** is provided in layer **L2-5** directly below trace **42**. Ground shields
2 **48a** and **48b** together act as the bottom shield. Side shields **50a** and **50b**
3 are provided on the two adjacent sides of trace **40**. Side shields **52a** and
4 **52b** are provided on the two adjacent sides of trace **42**. Side shields **51a**
5 and **51b** are provided on adjacent sides of interconnect **44**. The side
6 shields span even in the dielectric interlayers as a continuous wall, as
7 indicated in Fig.2B. The top, bottom and side shields are joined to form a
8 uniform enclosure (i.e. with no need for gaps), except for openings (not
9 shown) provided at desired points, for example, where the shielded circuitry
10 connect to another circuitry.

11 Figure 3A-3F show one method of producing the uniform metal shield
12 according to the present invention. In this example, metallic layers **L3-1**, **L3-**
13 **2** and **L3-3** are shown to illustrate the steps involved. Trace **60** is the
14 electrical circuitry to be shielded. For ease of illustration, other traces not
15 directly relevant to the present invention are not shown. Metallic layer **L3-1**
16 and dielectric layer **L3-1x2** are fabricated according to conventional
17 techniques (Fig.3A). Trenches **62** are then produced by conventional
18 photolithography or laser technology on the two sides where the side shields
19 are desired (Fig.3B). Trace **60** and metal side shields **64**, together with any
20 other desired metallic patterns (not shown) are then plated onto the
21 prescribed positions to form layer **L3-2** using photolithography and
22 electroplating (Fig.3C). A second dielectric layer is then spread onto layer
23 **L3-2** to form layer **L3-2x3** (Fig.3D). The dielectric material used is
24 preferably a liquid to facilitate the filling of trenches **62** remaining within
25 metal coating **64**. Trenches **66** are then fabricated in dielectric layer **L3-**

1 **2x3** above side of trenches **62** (Fig.3E). Side shields **68** are then fabricated
2 as a metal coating in trench **66** within laminated layer **L3-2x3**. At the same
3 time, the metallization pattern for layer **L3-3** is plated, including top metal
4 shield **70** (Fig.3F). Additional layers of dielectric material and metallic
5 patterns can then be built based on conventional technology. It is
6 understood by one skilled in the art that there can be many layers to the
7 board, and that the same principles may be applied to create shielding in
8 multi-layer circuits.

9 Figure 4A-F show another method of producing the uniform metal shield
10 according to the present invention. In this example, trace **74** is the electrical
11 circuitry to be shielded. Layer **L4-1** and **L4-2** are metal layers provided on
12 opposing sides of core layer **76**. Ground metal trace **75**, acting as bottom
13 shield for trace **74** is etched onto layer **L4-2** (Fig. 4A). For ease of
14 illustration, other metallization patterns typically found in PCBs in the various
15 metal layers are not shown. Dielectric layer **L4-2x3** is then layered on, and
16 trenches **78** produced using photolithography (Fig. 4B). After curing of layer
17 **L4-2x3**, two solid metal wall **80** are produced adjacent the position for trace
18 **74** using electroplating techniques (Fig. 4C). The next metallic layer **L4-3**,
19 containing trace **74** and ground shield **75** are produced using conventional
20 photolithography, electroplating and metal etching (Fig. 4D). To complete the
21 side shields, another dielectric layer **L4-3x4** is layered onto layer **L4-3**, and
22 trenches **82** produced by lithography directly above walls **80**. Electroplating
23 can again be performed to plate solid walls **83** in layer **L4-3x4**, together
24 with top shield **84**. For ease of illustration, other metal traces are not
25 indicated.

1 Figures 5A-H shows a further example of how the shielding structure
2 according to the present invention may be constructed. In this example, a
3 core layer **102** having second and first metallic layers **104** and **106**
4 respectively on two opposing sides is provided (Fig.5A). Conventional
5 photolithography, drilling, plating and etching are performed to provide
6 upper trace **108**, lower traces **110** and metal coated via **112** (Fig. 5B).
7 Electroplating and etching processes are then performed to produce two
8 solid metallic walls **114** (Fig. 5C). The remaining surfaces are protected by a
9 photoresist according to conventional methods. Dielectric layer **116** is then
10 coated onto the surface of second metallic layer **104** (Fig. 5D). Trace **120**
11 and other features of the third metallic layer **118** are then plated onto
12 dielectric layer **116** according to conventional plating and etching (Fig.5E).
13 To complete the EMI shielding for trace **120**, electroplating of solid metal
14 walls **122** on the two adjacent sides of trace **120** is performed using
15 conventional photoresist and electroplating technology. An additional
16 dielectric layer **124** is then layered onto third metallic layer **118** (Fig.5C).
17 This is followed by conventional photolithography and plating to complete
18 the top shield **126** for trace **120**.

19 The aforementioned examples illustrate the basic principles of how to
20 produce a shield according to the present invention. It is clear to one skilled
21 in the art that the shield according to the present invention may be applied to
22 complex electrical circuitry within a PCB. Figure 6 shows one example of a
23 more complex circuitry in which shielding may be provided. In this example,
24 electrical circuitry **88**, spanning 6 different layers of an eight-layer PCB **91**
25 (layers **L5-1** to **L5-8**), is shielded by metal shield **90**, as shown by the

1 dotted lines. Metal shield **90**, occupies only one area of the PCB, but the
2 remaining portions of the PCB is not shown for ease of illustration. Circuitry
3 **88** spans layers **L5-2** to **L5-8**. The layer L5-Y in which the various traces of
4 circuitry **88** runs are shown as a reference numeral (Y) in Fig.6. e.g. Trace
5 **88a** is shown with reference numeral **(4)** to show that it is provided in layer
6 **L5-4**. It is understood that other circuitry, outside the shield areas but within
7 the same PCB are also provided, but are not shown in Fig. 6 for ease of
8 illustration. Opening **92** is provided for connection of trace **93** of circuitry **88**
9 with another circuitry (not shown) within the same board. Opening **94** allows
10 interconnect **95** to connect with another circuitry in another layer, or with an
11 outer layer on the PCB.

12 With the teaching provided herein, it is therefore possible for circuitry that
13 normally give EMI can now be produced within the same board and be
14 shield from each other. Complete and uniform shielding is possible at any
15 position in any layer according to the needs of the designer. For example,
16 possible for numerous traces for high frequency signals to be printed
17 adjacent and co-axial to each other and be completely shielded from each
18 other using a side shield therebetween. It is clear that all types of PCBs can
19 utilize the methods disclosed herein. It is contemplated that many changes
20 and modifications may be made by one of ordinary skill in the art without
21 departing from the spirit and the scope of the invention described.

CLAIMS

- 1 1. A printed circuit board comprising an electrical circuitry adapted for electrical
2 connection with a second electrical circuitry, said electrical circuitry having a
3 metal shield therearound, said metal shield forming a box-like enclosure with the
4 electrical circuitry therein, wherein at least three sides of said box-like enclosure
5 being at least partially embedded within said board.
- 1 2. A printed circuit board according to claim 1 wherein said board comprises a
2 plurality of metallic layers insulated by dielectric material therebetween, and said
3 electrical circuitry being a trace, a group of interconnected traces within the same
4 metallic layer, or a group of interconnected traces in more than one metallic layer.
- 1 3. A printed circuit board according to claim 1 wherein said shield comprises :
2 a top shield above said electrical circuitry;
3 a bottom shield below said electrical circuitry; and
4 side shields on at least two opposing sides of said circuitry, said side shield
5 joining said top shield to said bottom shield without gaps.
- 1 4. A printed circuit board according to claim 3 wherein said side shields are solid
2 metal walls.
- 1 5. A printed circuit board comprising an electrical circuitry adapted for electrical
2 connection with a second electrical circuitry, said electrical circuitry having a
3 metal shield therearound, said metal shield at least partially embedded within the
4 interior of said board, wherein said shield comprises:

- 5 a top shield above said electrical circuitry;
- 6 a bottom shield below said electrical circuitry; and
- 7 side shields on at least two opposing sides of said circuitry, said side shield
- 8 joining said top shield to said bottom shield without gaps; and
- 9 wherein said side shields are metal coated trenches.
- 1 6. A printed circuit board according to claim 2 wherein said shield is completely
- 2 embedded within said printed circuit board.
- 1 7. A method of providing electromagnetic shielding for electrical circuitry within a
- 2 multi-layer printed circuit board comprising:
- 3 producing a bottom metallic shield in a layer below said circuitry;
- 4 producing side metallic shields adjacent said circuitry; and
- 5 producing a top metallic shield in a layer above said circuitry, wherein said
- 6 step of producing side metallic shields comprises producing trenches adjacent
- 7 said circuitry; and plating a layer of metal in said trench.
- 1 8. A method according to claim 7 wherein said step of plating the layer of metal in
- 2 said trench comprises producing solid walls adjacent said electrical circuitry.
- 1 9. A printed circuit board in accordance with claim 2 wherein the dielectric material
- 2 within the box-like shielded enclosure and the dielectric material external to the
- 3 box-like shielded enclosure are identical.

- 1 10. A printed circuit board in accordance with claim 9 wherein the dielectric
2 material within the box-like shielded enclosure and the dielectric material external
3 to the box-like shielded enclosure is epoxy.
- 1 11. A printed circuit board in accordance with claim 3 wherein the thickness of
2 the top shield is less than the thickness of either one of the side shields.
- 1 12. A printed circuit board in accordance with claim 3 wherein the thickness of
2 the bottom shield is less than the thickness of either one of the side shields.