CLAIMS

1. A memory cell comprising:

a front-end-of-the-line (FEOL) level comprising a gate structure straddling over a semiconductor fin, wherein a source/drain structure is located on each side of the gate structure, and a source/drain contact structure is located on each source/drain structure;

a middle-of-the-line (MOL) level located above the FEOL and comprising a magnetoresistive random access memory (MRAM) device and a lower contact structure, wherein a bottom electrode of the MRAM device contacts one of the source/drain contact structures located on one side of the gate structure, and the lower contact structure contacts another of the source/drain contact structures located on another side of the gate structure; and

a back-end-of-line (BEOL) level located above the MOL level and comprising a first upper contact structure contacting a surface of the lower contact structure, and a second upper contact structure contacting a surface of a top electrode of the MRAM device, wherein the MOL level further comprises a dielectric material layer having a mesa portion and a recessed portion, and wherein a lower portion of the lower contact structure is embedded in the recessed portion of the dielectric material layer, and the bottom electrode is embedded in an area of the dielectric material layer including the mesa portion.

2. The memory cell of claim 1, wherein the MRAM device further comprises a magnetic tunnel junction (MTJ) pillar contacting the bottom electrode, wherein the MTJ pillar is located on the mesa portion of the dielectric material layer.

3. The memory cell of claim 2, further comprising a dielectric material spacer encapsulating and encircling the MTJ pillar and the top electrode, wherein a portion of the dielectric material spacer contacts a sidewall of the mesa portion of the dielectric material layer.

4. The memory cell of claim 2, wherein the MTJ pillar is a bottom pinned MTJ structure.

5. The memory cell of claim 2, wherein the MTJ pillar is a top pinned MTJ structure.

6. The memory of claim 2, wherein both the MTJ pillar and the top electrode have a first critical dimension, and wherein the bottom electrode has a second critical dimension that is less than the first critical dimension.

7. The memory cell of claim 2, wherein both the MTJ pillar and the top electrode are cylindrical in shape.

8. The memory cell of claim 1, wherein a lower portion of the lower contact structure has tapered sidewalls.

9. The memory cell of claim 1, wherein the first upper contact structure and the second upper contact structure are partially located in a BEOL dielectric material layer that is located above the MOL level.

10. A memory cell comprising:

a front-end-of-the-line (FEOL) level comprising a gate structure straddling over a semiconductor fin, wherein a source/drain structure is located on each side of the gate structure, and a source/drain contact structure is located on each source/drain structure;

a middle-of-the-line (MOL) level located above the FEOL and comprising a magnetoresistive random access memory (MRAM) device and a lower contact structure, wherein a bottom electrode of the MRAM device contacts one of the source/drain contact structures located on one side of the gate structure, and the lower contact structure contacts another of the source/drain contact structures located on another side of the gate structure;

a back-end-of-line (BEOL) level located above the MOL level and comprising a first upper contact structure contacting a surface of the lower contact structure, and a second upper contact structure contacting a surface of a top electrode of the MRAM device, and

a conductive metal-containing liner located between the lower contact structure and the another source/drain structure that is located on the another side of the gate structure, wherein the conductive metal-containing liner has a topmost surface that is coplanar with a topmost surface of the lower contact structure.

11. The memory cell of claim 10, wherein the MOL level further comprises a dielectric material layer having a mesa portion and a recessed portion, and wherein a lower portion of the lower contact structure is embedded in the recessed portion of the dielectric material layer, and the bottom electrode is embedded in an area of the dielectric material layer including the mesa portion.

12. The memory cell of claim 10, wherein the topmost surface of the conductive metal-containing liner is located beneath a topmost surface of the top electrode of the MRAM device.

13. A method of forming a memory cell, the method comprising:

forming a front-end-of-the-line (FEOL) level comprising a gate structure straddling over a semiconductor fin, wherein a source/drain structure is located on each side of the gate structure, and a source/drain contact structure is located on each source/drain structure;

forming a dielectric material layer of a middle-of-the-line (MOL) level over the FEOL level;

forming a bottom electrode of a magnetoresistive random access memory (MRAM) device in the dielectric material layer and contacting one of the source/drain contact structures located on one side of the gate structure;

forming a magnetic tunnel junction (MTJ) pillar and a top electrode of the MRAM device above the bottom electrode;

forming a lower contact structure contacting another of the source/drain contact structures located on another side of the gate structure, wherein a lower portion of the lower contact structure is embedded in the dielectric material layer; and

forming a back-end-of-line (BEOL) level above the MOL level and comprising a first upper contact structure contacting a surface of the lower contact structure, and a second upper contact structure contacting a surface of the top electrode of the MRAM device, wherein the forming of the MTJ pillar and the top electrode comprises forming a MTJ material stack and a top electrode layer, and patterning the MTJ material stack and the top electrode layer utilizing an ion beam etch, wherein, during the ion beam etch, a portion of the dielectric material

layer that is located laterally adjacent to the bottom electrode is recessed, and the lower portion of the lower contact structure is embedded in the recessed portion of the dielectric material layer.

14. The method of claim 13, further comprising forming a dielectric material spacer encapsulating and encircling the MTJ pillar and the top electrode.

15. The method of claim 13, wherein the forming of the lower contact structure comprises:

forming a contact opening in the dielectric material layer that physically exposes a surface of the another of the source/drain contact structures located on the another side of the gate structure;

forming a conductive metal-containing layer on the dielectric material layer including within the contact opening and along a sidewall wall and above a topmost of the top electrode;

forming a contact metal-containing layer on the conductive metal-containing layer;

recessing the contact metal-containing layer and the conductive metal-containing layer to a height that is below a height of the top electrode;

forming a hard mask cap above the recessed contact metal-containing layer; and

patterning the hard mask cap, the recessed contact metal-containing layer and the recessed conductive metal-containing layer that are located in the another side of the gate structure.

16. The method of claim 15, wherein the contact opening has tapered sidewalls, and wherein the lower portion of the lower contact structure that is embedded in the dielectric material layer has tapered sidewalls.

17. The method of claim 13, wherein the MTJ pillar is a bottom pinned MTJ structure.

18. The method of claim 13, wherein the MTJ pillar is a top pinned MTJ structure.