INTEGRATED CIRCUIT DIE CONTAINING METEL- AND PARTICLE-FILLED THROUGH-SILICON VIAS

TECHNICAL FIELD

[0001] The invention relates to the field of microelectronics and more particularly, but not exclusively, to stacked packages and electrically conductive through silicon vias.

BACKGROUND

[0002] The evolution of integrated circuit designs has resulted in higher operating frequency, increased numbers of transistors, and physically smaller devices. This continuing trend has generated ever-increasing area densities of integrated circuits. To further increase possible densities of integrated circuits, it may be desirable in some instances to electrically couple an active circuit layer on a die to another active circuit layer on the same, or a different, die by means of an electrically conductive through silicon via. A typical through silicon via may simply be a void within a bulk silicon portion of a die filled with a bulk material of approximately uniform composition, for example an alloy of copper.

[0003] Many materials may undergo a physical expansion or contraction resulting from a change in temperature. A coefficient of thermal expansion (CTE) may represent a change in unit volume of a bulk material for a unit change in temperature. If a volume of a first bulk material encloses a second volume of a second bulk material with different coefficient of thermal expansion from the first bulk material with zero stress at a given temperature, a change

in temperature may cause a non-zero stress to develop at an interface of the different bulk materials. In some cases, under a sufficient change in temperature, or a sufficient number of temperature excursion cycles, a stress at an interface of the different bulk materials may exceed a certain critical stress and cause a permanent deformation or dislocation in one or the other or both bulk materials. Alternatively, performance of the integrated circuit device may degrade from an increased stress at an interface of different bulk materials, without either material undergoing a permanent deformation or dislocation.

[0004] During a normal manufacturing cycle, packages containing integrated circuits may undergo various processes, some of which may occur at an elevated temperature. For example, a package containing integrated circuits may undergo, for example, a solder reflow process, after perhaps being at room temperature. In a solder reflow process, various components within the package, including the integrated circuits and accompanying bulk silicon to which the integrated circuits may be coupled may approach, or even exceed a temperature at which a solder reflows, e.g., perhaps 230 °C for a representative Pb-free solder, contrasting with a normal storage temperature, for example, perhaps 25 °C. In the present example, a package and its components may undergo a significant temperature change, e.g. based on the present example, as much or greater than 205 °C.

[0005] Further, under normal operation, integrated circuits such as processors generate heat that may cause various components within a package, including the integrated circuits and accompanying bulk silicon to which the

integrated circuits may be coupled, to undergo temperature variations. While temperature excursions under normal operation may not be as extreme as those experienced in a manufacturing process, throughout a product's design life, a package and its components including the integrated circuits and accompanying bulk silicon to which the integrated circuits may be coupled may undergo a high number of temperature excursions resulting from normal operation.

[0006] Copper has a bulk linear CTE of approximately 16.5 ppm/°C in contrast to silicon, which has a bulk linear CTE of approximately 2.6 ppm/°C. Thus, a unit volume of copper expands considerably more than a unit volume of silicon. Because a typical through silicon via may simply be a void in a bulk silicon portion of an integrated circuit die filled with an alloy of copper and the CTE of each material is almost an order of magnitude different, a mechanical stress may be induced at a copper – silicon interface when the package undergoes a temperature excursion.

[0007] For example, **Fig. 1(a)** represents a group of prior art through silicon vias, showing a portion of a bulk silicon die with integrated circuits **100**. Prior art through silicon vias **112** may be electrically coupled to metal pads **108** through an electrically conductive seed layer **114**. Between an electrically conductive seed layer **114** and a portion of the bulk silicon die **102** may be a passivation or electrical insulation layer **116**. Metal pads **108** and a portion of the bulk silicon die **102** may be separated by an interlayer dielectric (ILD) material **104**. A layer of ILD **104** coupled to a portion of the bulk silicon die **102** between metal pads **108** may underlie a layer of passivation material **110**

or a protection layer **106.** **Fig. 1(b)** and **Fig. 1(c)** represent a prior art through silicon via suffering stress induced, mechanical failures of delamination **120** and die cracking **118**, respectively. A prior art through silicon via may have a bulk CTE substantially similar in magnitude to the bulk CTE of the continuous metal phase and substantially different from the bulk CTE of silicon, leading to significant principal stresses under temperature excursions. The significant principal stresses in turn may cause mechanical failures of the integrated circuit such as delamination **120** or die cracking **118**. Further, significant principal stresses, without causing delamination **120** or die cracking **118** may cause degraded performance within an integrated circuit.

[0008] To maintain a mechanical stress resulting from a CTE mismatch below a critical stress of either bulk material for a given temperature excursion, via size may be reduced, spacing between adjacent vias may be increased, or vias may be positioned far from active circuitry. Each of these solution options may lead to increased die size, lower density circuits than may otherwise be realized or increased cost per die.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] **Fig. 1** illustrates a representation of prior art through silicon vias made of a single phase bulk material (**Fig. 1(a)**) leading to delamination (**Fig. 1(b)**) and die cracking (**Fig. 1(c)**).

[0010] **Fig. 2** illustrates one embodiment of a system including an electronic package assembly having particle-filled through silicon vias with reduced thermal expansion.

[0011] **Fig. 3** illustrates a graph of normalized material stress variation with normalized coefficient of thermal expansion for a given array of through silicon vias.

[0012] **Fig. 4** illustrates a graph of normalized material stress variation with via array pitch for vias filled with pure copper and for vias filled with a bulk material with 25% of the CTE of pure copper.

[0013] **Fig. 5** illustrates variation of CTE and variation of Electrical Resistivity with volume fraction of embedded particles for two different filler materials.

[0014] **Fig. 6** illustrates an embodiment of electrically conductive through silicon vias made of a bulk material, the bulk material consisting of a matrix metal forming a continuous phase and embedded particles forming a dispersed phase.

[0015] **Fig. 7** illustrates a portion of a silicon die prior to applying.

[0016] **Fig. 8** illustrates the portion of a silicon die of **Fig. 7** with several areas of bulk silicon removed.

[0017] **Fig. 9** illustrates the portion of a silicon die of **Fig. 8** with a first layer of material deposited on a surface of the bulk silicon and an underside of a metal pad.

[0018] **Fig. 10** illustrates the portion of a silicon die of **Fig. 9** after exposing the metal pads through partial removal of the first layer of material deposited.

[0019] **Fig. 11** illustrates the portion of a silicon die of **Fig. 10** with a second layer of material deposited over the exposed metal pads and first layer of material.

[0020] **Fig. 12** illustrates the portion of a silicon die of **Fig. 11** with photoresist applied.

[0021] **Fig. 13** illustrates the portion of a silicon die of **Fig. 12** immersed in an electrolysis bath with dispersed particles.

[0022] **Fig. 14** illustrates the portion of a silicon die of **Fig. 13** with partially deposited through silicon vias with dispersed particles.

[0023] **Fig. 15** illustrates the portion of a silicon die of **Fig. 14** with fully deposited through silicon vias with dispersed particles.

[0024] **Fig. 16** illustrates the portion of a silicon die of **Fig. 15** with the electrolysis bath removed.

[0025] **Fig. 17** illustrates the portion of a silicon die of **Fig. 16** with the photoresist removed.

[0026] **Fig. 18** illustrates the portion of a silicon die of **Fig. 17** with the first and second layers of material removed in regions between the through silicon vias.

[0027] **Fig. 19** illustrates a method of manufacture of reduced CTE through silicon vias.

[0028] Fig. 20 illustrates a table of possible materials used to form a composite via.

DETAILED DESCRIPTION

[0029] Herein disclosed are a methods, apparatuses, and systems for providing a through silicon via with a desirable bulk coefficient of thermal expansion. In the following detailed description, reference is made to the accompanying drawings which form a part hereof wherein like numerals designate like parts throughout, and in which is shown by way of illustration specific embodiments which may be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the claims presented herein. It should also be noted that directions and references (e.g., up, down, top, bottom, primary side, backside, etc.) may be used to facilitate the discussion of the drawings and are not intended to restrict the breadth of application of the claims presented. Therefore, the following detailed description is not to be taken in a limiting sense and the scope of possible embodiments is defined only by the appended claims and their equivalents.

[0030] Referring to **Fig. 2**, there is illustrated one of many possible systems in which embodiments presented may be used. The integrated circuit package **200** may contain a portion of a silicon die similar to the portion of a silicon die **600, 700, 800, 900, 1000, 1100, 1200, 1300, 1400, 1500, 1600, 1700,** and **1800** depicted in **Fig. 6 – Fig. 18**, respectively. In one embodiment, the integrated circuit package **200** may include a microprocessor. In an alternate embodiment, the integrated circuit package **200** may include an application specific IC (ASIC). Integrated circuits found in chipsets (e.g., graphics,

sound, and control chipsets) or memory may also be packaged in alternate embodiments.

[0031] For the embodiment depicted by **Fig. 2**, the system **90** may also include a main memory **202**, a graphics processor **204**, a mass storage device **206**, and an input/output module **208** coupled to each other by way of a bus **210**, as shown. Examples of the memory **202** include but are not limited to static random access memory (SRAM) and dynamic random access memory (DRAM). Examples of the mass storage device **206** include but are not limited to a hard disk drive, a flash drive, a compact disk drive (CD), a digital versatile disk drive (DVD), and so forth. Examples of the input/output modules **208** include but are not limited to a keyboard, cursor control devices, a display, a network interface, and so forth. Examples of the bus **210** include but are not limited to a peripheral control interface (PCI) bus, and Industry Standard Architecture (ISA) bus, and so forth. In various embodiments, the system **90** may be a wireless mobile phone, a personal digital assistant, a pocket PC, a tablet PC, a notebook PC, a desktop computer, a set-top box, an audio/video controller, a DVD player, a network router, a network switching device, or a server.

[0032] **Fig. 3** illustrates a graph of results from a finite element simulation of a first principal stress with a normalized bulk CTE (reference CTE is that of copper) of a material used to fill a 20 micron via in an array of vias with a 500 micron pitch. A normalized CTE of 0.16 represents silicon. The data of **Fig. 3** shows the first principal stress may reduce as the via material's bulk CTE approaches that of silicon.

[0033] **Fig. 4** illustrates a graph of further finite element simulation showing a variation of a first principal stress with via pitch for a 20 micron pure copper via and a 20 micron via made of a material with a CTE 25% that of copper. The data of **Fig. 4** shows the first principal stress may decrease significantly at small pitch if a bulk material with reduced CTE forms a via. Further, a reduced CTE via may result in a lower first principal stress, at smaller pitch, than a conventional CTE via at large pitch.

[0034] A dispersed phase of filler particles may alter one or more bulk material properties of a through silicon via. For example, a resulting electrical resistivity of a composite of a metal matrix forming a continuous phase and an embedded spherical filler forming a dispersed phase may be approximated by the expression, $k_{composite} = \frac{2k_1 + k_2 + p(k_1 - k_2)}{2k_1 + k_2 - 2p(k_1 - k_2)} k_2$, where $k_{composite}$ represents the resulting bulk electrical resistivity, k_1 represents the bulk electrical resistivity of the spherical filler and k_2 represents the bulk electrical resistivity of the matrix metal and p represents the volume fraction of spherical filler to bulk composite volume.

[0035] Further, a resulting CTE of a composite of a metal matrix forming a continuous phase and an embedded spherical filler forming a dispersed phase may be approximated by the expression, $CTE_{composite} = p \cdot CTE_1 + (1-p)CTE_2$, where $CTE_{composite}$ represents the resulting bulk CTE, CTE_1 represents the bulk CTE of the spherical filler and CTE_2 represents the bulk CTE of the matrix metal and p again represents the volume fraction of spherical filler to bulk composite volume.

[0036] **Fig. 5** illustrates a graph showing an increased volume fraction of a spherical filler with CTE less than a matrix metal may monotonically decrease the bulk CTE of a resulting composite of matrix metal and embedded spherical filler. Further, **Fig. 5** illustrates that increased volume fraction of a spherical filler with electrical resistivity greater than a matrix metal may monotonically increase the bulk resistivity of a resulting composite of matrix metal and embedded spherical filler. Still further, the data of **Fig. 5** implies a choice of filler material may comprehend a tradeoff of reduced CTE with increased electrical resistivity. However, filler particle volume fractions may range up to more than 80%.

[0037] Although spherical particles are modeled for simplicity of calculation, spherical particles reduced to practice may be of arbitary shape. Further, filler particles comprising the dispersed phase may be any one, or combination, of silica, alumina, boron nitride, tungsten, Invar, Super Invar, Kovar or other material with CTE less than the surrounding bulk die material through which the via passes, e.g., silicon. Still further, filler particles made of a ferromagnetic material, e.g., Invar, Super Invar and Kovar, may be used in a magnetic-field assisted electroplating process.

[0038] An embodiment may use one of many metals for the matrix. Exemplary matrix materials include copper (Cu), gold (Au), aluminum (Al), tungsten (W), silver (Ag) and both eutectic and non-eutectic solders. Exemplary eutectic solders include tin-lead (Pb/Sn) and gold-tin (Au/Sn) solders.

[0039] **Fig. 6** illustrates one embodiment of a portion of a die with integrated circuits **600**. In one embodiment, through silicon vias **612** may be

electrically coupled to metal pads **608** through an electrically conductive seed layer **614**. In a further embodiment, the through silicon vias **612** may be a composite wherein the bulk CTE of the vias **612** is less than the bulk CTE of the matrix metal. In still a further embodiment, a reduced CTE through silicon via **612** may comprise a matrix metal forming a continuous phase and embedded particles with a CTE less than the matrix metal, the embedded particles forming a dispersed phase and the reduced CTE through silicon via **612** having a bulk CTE less than the bulk CTE of the matrix metal. Between an electrically conductive seed layer **614** and a portion of the bulk silicon die **602** may be a passivation or electrical insulation layer **616**. Metal pads **608** and a portion of the bulk silicon die **602** may be separated by an interlayer dielectric (ILD) material **604**. A layer of ILD **604** coupled to a portion of the bulk silicon die **602** between metal pads **608** may underlie a layer of passivation material **610** or a protection layer **606.**

[0040] **Fig. 7 – Fig. 18** illustrate articles undergoing a method to manufacture a via through a die containing integrated circuits.

[0041] **Fig. 7** illustrates a substrate **700** to which a method of manufacture may be applied. Metal pads **608** and a portion of a die **602** may be separated by an interlayer dielectric (ILD) material **604**. In one embodiment, the die **602** may be silicon. In still a further embodiment, a layer of ILD **604** coupled to a portion of the bulk silicon die **602** between metal pads **608** may underlie a layer of passivation material **610** or a protection layer **606.**

[0042] **Fig. 8** illustrates the substrate of **Fig. 7** wherein a portion of a die with integrated circuits **800** has material removed in a vicinity near a metal pad

608. In one embodiment, the die **602** may be silicon. Removal of die material may be by photolithography followed by a dry or wet etching process. Alternatively, removal may be by a micromachining technique. In one embodiment, a micromachining technique may be blasting, drilling, or another micromachining technique, or a combination thereof. Further, a portion of the ILD **504** in a vicinity near a metal pad may similarly be removed. As in **Fig. 7**, metal pads **608** and a portion of the bulk silicon die **602** may be separated by an interlayer dielectric (ILD) material **604**. A layer of ILD **604** coupled to a portion of the bulk silicon die **602** between metal pads **608** may underlie a layer of passivation material **610** or a protection layer **606.**

[0043] **Fig. 9** illustrates the substrate of **Fig. 8** during manufacture showing a portion of a die with integrated circuits **900**. In **Fig. 9**, a layer of material **616** may deposited on the surface of the die **602**. In one embodiment, the die **602** may be silicon. The layer of material **616** may be a passivation layer. Alternatively, the layer of material **616** may be an electrical insulation material. As in previous figures, metal pads **608** and a portion of the bulk silicon die **602** may be separated by an interlayer dielectric (ILD) material **604**. A layer of ILD **604** coupled to a portion of the die **602** between metal pads **608** may underlie a layer of passivation material **610** or a protection layer **606.**

[0044] **Fig. 10** illustrates the substrate of **Fig. 9** undergoing manufacture, showing a portion of a die with integrated circuits **1000**. In **Fig. 10**, a layer of material **616** proximate to a metal pad **608** may be removed, re-exposing a previously

exposed metal pad **608**. As in previous figures, the die **602** may be silicon and the metal pads **608** and a portion of the die **602** may be separated by an interlayer dielectric (ILD) material **604**. A layer of ILD **604** coupled to a portion of the bulk silicon die **602** between metal pads **608** may underlie a layer of passivation material **610** or a protection layer **606.**

[0045] **Fig. 11** illustrates a portion of the substrate of **Fig. 10** with integrated circuits **1100** with a second layer of material **614** deposited on the surface of the previously deposited layer of material **616**. The second layer of material **614** may be a barrier layer. Alternatively, the layer of material **614** may be a seed layer to facilitate a later electroplating process. As in previous figures, metal pads **608** and a portion of the bulk silicon die **602** may be separated by an interlayer dielectric (ILD) material **604**. A layer of ILD **604** coupled to a portion of the bulk silicon die **602** between metal pads **608** may underlie a layer of passivation material **610** or a protection layer **606.**

[0046] **Fig. 12** illustrates the substrate of **Fig. 11** with integrated circuits **1200** and a pattern of photoresist **1202** deposited on the surface of the previously deposited layer of material **614**. As in previous figures, a layer of material **616** may overlie the bulk silicon die **502** and underlie a second layer of material **614**. Metal pads **608** and a portion of the bulk silicon die **602** may be separated by an interlayer dielectric (ILD) material **604**. A layer of ILD **604** coupled to a portion of the bulk silicon die **602** between metal pads **608** may underlie a layer of passivation material **610** or a protection layer **606.**

[0047] **Fig. 13** illustrates the substrate of **Fig. 12** showing a portion of a die with integrated circuits immersed in an electroplating bath **1300**. In **Fig. 13**, an

electroplating bath **1302** may contain in solution or suspension particles **1304** of reduced CTE relative to a deposited matrix metal. As in previous figures, a layer of material **616** may overlie the bulk silicon die **602** and underlie a second layer of material **614**. Metal pads **608** and a portion of the bulk silicon die **602** may be separated by an interlayer dielectric (ILD) material **604**. A layer of ILD **604** coupled to a portion of the bulk silicon die **602** between metal pads **608** may underlie a layer of passivation material **610** or a protection layer **606** and a pattern of photoresist **1202** may be further present.

[0048] **Fig. 14** illustrates the substrate of **Fig. 13** with integrated circuits immersed in an electroplating bath **1400**. In **Fig. 14**, a portion of a via **1402** may be deposited within a void previously generated in the die **602**. In one embodiment, the via **1402** may be through silicon. In one embodiment, the die **602** may be silicon. An electroplating bath **1302** may contain in solution or suspension particles **1304** of reduced CTE relative to a deposited matrix metal. During the electroplating process, filler particles **1304** may be co-deposited in a portion of the reduced CTE through silicon via **1402**. Further, to aid co-deposition of filler particles **1304**, a driving potential may be applied. The driving force may be gravity, or some other driving potential made to act on the electroplating bath **1302** or filler particles **1304**. As in previous figures, a layer of material **616** may overlie the bulk silicon die **602** and underlie a second layer of material **614**. Metal pads **608** and a portion of the bulk silicon die **602** may be separated by an interlayer dielectric (ILD) material **604**. A layer of ILD **604** coupled to a portion of the bulk silicon die

602 between metal pads 608 may underlie a layer of passivation material 610 or a protection layer 606 and a pattern of photoresist 1202 may be further present.

[0049] Fig. 15 illustrates a portion of the substrate of Fig. 16 with integrated circuits immersed in an electroplating bath 1500. In Fig. 14, a reduced via 612 may be fully deposited, the via being a composite comprising a metal matrix with greater CTE than the die 602, the metal matrix forming a continuous phase, and embedded filler particles with a CTE less than the CTE of the metal matrix, the filler particles forming a dispersed phase, the composite exhibiting a bulk CTE less than the bulk CTE of the matrix metal. In one embodiment, the die 602 is substantially silicon. As in previous figures, an electroplating bath 1302 may contain in solution or suspension particles 1304 of reduced CTE relative to a deposited matrix metal. During the electroplating process, filler particles 1304 may be co-deposited in a portion of the reduced CTE through silicon via 1402. Further, to aid co-deposition of filler particles 1304, a driving potential may be applied. The driving force may be gravity, or some other driving potential made to act on the electroplating bath 1302 or filler particles 1304. As in previous figures, a layer of material 616 may overlie the bulk silicon die 602 and underlie a second layer of material 614. Metal pads 608 and a portion of the bulk silicon die 602 may be separated by an interlayer dielectric (ILD) material 604. A layer of ILD 604 coupled to a portion of the bulk silicon die 602 between metal pads 608 may underlie a layer of passivation material 610 or a protection layer 606 and a pattern of photoresist 1202 may be further present.

[0050] **Fig. 16** illustrates the substrate of **Fig. 15,** a portion of die with integrated circuits **1600** with the electroplating bath removed. As in previous figures, the die **602** may be silicon, a layer of material **616** may overlie the bulk silicon die **602** and underlie a second layer of material **614**. Metal pads **608** and a portion of the bulk silicon die **602** may be separated by an interlayer dielectric (ILD) material **604**. A layer of ILD **604** coupled to a portion of the bulk silicon die **602** between metal pads **608** may underlie a layer of passivation material **610** or a protection layer **606** and a pattern of photoresist **1202** may be further present.

[0051] **Fig. 17** illustrates the substrate of **Fig. 16**, showing a portion of die with integrated circuits **1700**, the pattern of photoresist removed. As in previous figures, a layer of material **616** may overlie the bulk silicon die **602** and underlie a second layer of material **614**. Metal pads **608** and a portion of the bulk silicon die **602** may be separated by an interlayer dielectric (ILD) material **604**. A layer of ILD **604** coupled to a portion of the bulk silicon die **602** between metal pads **608** may underlie a layer of passivation material **610** or a protection layer **606**.

[0052] **Fig. 18** illustrates the substrate of **Fig. 17** showing a portion of bulk silicon die with integrated circuits **1800** and a first layer **614** and second layer **616** of material etched among the newly deposited vias **612**, exposing a portion of die **602**. The die **602** may be silicon. As in previous figures, a layer of material **616** may overlie the bulk silicon die **602** and underlie a second layer of material **614**. Metal pads **608** and a portion of the bulk silicon die **602** may be separated by an interlayer dielectric (ILD) material **604**. A layer of

ILD **604** coupled to a portion of the bulk silicon die **602** between metal pads **608** may underlie a layer of passivation material **610** or a protection layer **606**.

[0053] **Fig. 19** illustrates a method of forming through hole vias comprising a matrix and dispersed filler particles. In the method illustrated in **Fig. 19**, material may be removed **1902** from a backside of a bulk silicon wafer having a primary side and a backside A metal pad integrated on a primary side of the bulk silicon wafer may be exposed **1904**. A first layer of material may be deposited on an exposed metal pad and an interior surface of the void within the bulk silicon wafer created by material removal **1906**. The layer of material may be etched to expose a region of the metal pad **1908**. A layer of electrically conductive material may be deposited over the exposed region of the metal pad and the previously deposited material **1910**. A pattern of photoresist may be deposited over the layer of electrically conductive material **1912**. An electroplating technique may be applied to deposit an electrically conductive through silicon via made of a two phase bulk material **1914**, a continuous phase being a matrix metal and a dispersed phase being embedded filler particles. The pattern of photoresist may be removed **1916** and the two layers of material deposited on the backside of the bulk silicon wafer may be etched **1918**.

[0054] **Fig. 20** illustrates a partial list of materials, and several associated material properties, that may be used in one embodiment of a composite via.

[0055] Although specific embodiments have been illustrated and described herein for purposes of description of the preferred embodiment, it will be

appreciated by those of ordinary skill in the art that a wide variety of alternate and/or equivalent implementations calculated to achieve the same purposes may be substituted for the specific embodiment shown and described without departing from the scope intended. For example, an alternative embodiment may exist where filler particles are packed into an open via hole within a die and a chemical vapor deposition (CVD) or physical vapor deposition (PVD) process (e.g., sputtering, evaporation, jet vapor deposition) may be used to fill in any volume in the through hole unfilled by packed particles. Yet another embodiment may exist wherein solder balls containing filler particles may reflow into an open via hole within a die. Still another embodiment may reflow solder balls containing filler particles under vacuum to avoid air filled voids within a finished via. Thus, those with skill in the art will readily appreciate implementation may be achieved using a very wide variety of embodiments. This application is intended to cover any adaptations or variations of the embodiments discussed herein. Therefore, it is manifestly intended only the claims and the equivalents thereof limit the scope of possible embodiments.

CLAIMS

What is claimed is:

1. A semiconductor package comprising:
   an integrated circuit;
   a material forming an electrically conductive through hole via coupled to the integrated circuit;
   a matrix forming a continuous phase within the material of the via; and
   particles embedded in the matrix forming a dispersed phase within the material of the via.

2. The semiconductor package of Claim 1, wherein a bulk material property of the material forming the via differs from the matrix.

3. The semiconductor package of Claim 2, wherein the material property is a coefficient of thermal expansion.

4. The semiconductor package of Claim 2, wherein the material property is electrical resistivity.

5. The semiconductor package of Claim 1, wherein the material forming the via has a lower coefficient of thermal expansion than the matrix.

6. The semiconductor package of Claim 1, wherein the matrix comprises a chosen one of the group consisting of copper (Cu), gold (Au), aluminum (Al), tungsten (W), silver (Ag), eutectic solder, and non-eutectic solder.

7. The semiconductor package of Claim 6, wherein the eutectic solder comprises one of the group consisting of tin-lead (Pb/Sn) solder and gold-tin (Au/Sn) solder.

8. The semiconductor package of Claim 1, wherein the filler particles comprise a chosen one of the group consisting of silica, alumina, boron nitride, tungsten, Invar, Super Invar, and Kovar.

9. The semiconductor package of Claim 1, wherein the filler particles comprise a ferromagnetic material.

10. A method comprising:

removing material from a die;

forming in the die an electrically conductive via of a material different from the die, the material being a composite of a matrix forming a continuous phase and embedded particles forming a dispersed phase.

11. The method of claim 10, wherein forming in the die an electrically conductive via further comprises one of the group consisting of electroplating, chemical vapor deposition (CVD), physical vapor deposition (PVD), sputtering, evaporation, jet vapor deposition, and reflowing solder containing filler particles.

12. The method of claim 11, wherein electroplating further comprises providing a driving potential to the first concentration of embedded particles to cause a second concentration of embedded particles in the material of the through hole via.

13. The method of claim 12 wherein the second concentration of embedded particles is greater than the first concentration of embedded particles.

14. The method of claim 12 wherein the driving potential comprises one of the group consisting of gravity and a magnetic field.

15. The method of claim 10 wherein the bulk material of the via has a different material property than the matrix metal.

16. The method of claim 15 wherein the material property is a coefficient of thermal expansion, the material of the via having a lower coefficient of thermal expansion than the matrix.

17. The method of Claim 10, wherein the matrix comprises a chosen one of the group consisting of copper (Cu), gold (Au), aluminum (Al), tungsten (W), silver (Ag), eutectic solder, and non-eutectic solder.

18. The method of Claim 17, wherein the eutectic solder comprises one of the group consisting of tin-lead (Pb/Sn) solder and gold-tin (Au/Sn) solder.

19. The method of Claim 10, wherein the filler particles comprise a chosen one of the group consisting of silica, alumina, boron nitride, tungsten, Invar, Super Invar, and Kovar.

20. The method of Claim 10, wherein the filler particles comprise a ferromagnetic material.

21. A system comprising:

a semiconductor package having an integrated circuit, the integrated circuit including,

an electrically conductive through hole via;

a matrix forming a continuous phase within the via;

particles with a coefficient of thermal expansion lower than the coefficient of thermal expansion of the matrix embedded in the matrix and forming a dispersed phase within the matrix; and

a mass storage device coupled to the semiconductor package.

22. The system of claim 21, further comprising:

a dynamic random access memory coupled to the integrated circuit; and

an input/output interface coupled to the integrated circuit.

23. The system of claim 22, wherein the input/output interface comprises a networking interface.

24. The system of claim 21, wherein the integrated circuit is a processor.

25. The system of claim 24, wherein the system is a selected one of a group comprising a set-top box, a media-center personal computer, and a digital versatile disk player.