ABSTRACT

A semiconductor memory device includes a first channel pattern and a second channel pattern stacked on a substrate, a word line disposed between the first and second channel patterns and that extends in a first direction parallel to a top surface of the substrate, a data storage pattern disposed between a top surface of the word line and the first channel pattern and between a bottom surface of the word line and the second channel pattern, a bit line that extends in a second direction perpendicular to the top surface of the substrate and that is connected to first end portions of the first and second channel patterns, and a source line that extends in the second direction and is connected to second end portions of the first and second channel patterns.

FIG. 4