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METHOD OF FABRICATING CMOS DEVICE WITH DUAL GATE ELECTRODE

ABSTRACT

A method of fabricating a dual gate electrode CMOS device, comprising the following steps. A wafer is provided having an N-MOSFET region and a P-MOSFET region. A sacrificial gate layer/doped N^+ poly-1 layer/gate insulator layer stack is formed over the wafer. The N-MOSFET sacrificial gate layer is patterned to form a once patterned sacrificial gate layer only within the N-MOSFET region, exposing the doped N^+ poly-1 layer within the P-MOSFET region. An undoped poly-2 layer is formed over the once patterned sacrificial gate layer and the exposed N^+ poly-1 layer within the P-MOSFET region. The undoped poly-2 layer is planarized to form a planarized undoped poly-2 layer only within the P-MOSFET region. The once patterned sacrificial gate layer, the doped N^+ poly-1 layer and the gate insulator layer within the N-MOSFET region are planarized to form an initial N-MOSFET gate electrode stack having exposed sidewalls. The planarized undoped poly-2 layer, the doped N^+ poly-1 layer and the gate insulator layer within the P-MOSFET region are planarized to form an initial P-MOSFET gate electrode stack having exposed sidewalls. Sidewall spacers are formed adjacent the exposed sidewalls of the initial N-MOSFET and P-MOSFET gate electrode stacks. An intermetal dielectric layer is formed adjacent and between the initial N-MOSFET and P-MOSFET gate electrode stacks. The initial P-MOSFET gate electrode stack is removed to form a P-MOSFET gate cavity exposing a portion of the wafer. A second P-MOSFET gate insulator layer is formed within the P-MOSFET gate cavity over the exposed portion of the wafer. The upper sacrificial gate layer of the initial N-MOSFET gate electrode stack is removed to form an N-MOSFET gate cavity. A metal layer is formed over the structure, filling the remaining P-MOSFET gate

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cavity and the N-MOSFET gate cavity. The metal layer is planarized to remove the excess metal from over the intermetal dielectric layer leaving planarized N-MOSFET metal gate electrode cap within N-MOSFET gate cavity to form a finalized N-MOSFET and planarized P-MOSFET metal gate within the remaining P-MOSFET gate cavity to form a finalized P-MOSFET, thus completing formation of the dual gate electrode CMOS device.

FIGURE 9