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SEMICONDUCTOR WAFER HAVING ALIGNMENT MARKS FOR A TUNGSTEN PLUG PROCESS AND A METHOD OF MANUFACTURE THEREFORE

Technical Field of the Invention

The present invention is directed, in general, to a semiconductor device and, more specifically, to a semiconductor wafer and its manufacture wherein the semiconductor wafer has alignment marks for a tungsten plug process.

Background of the Invention

It is well known that integrated circuit fabrication on semiconductor wafers requires the formation of precisely controlled apertures, such as contact openings or "vias," that are subsequently interconnected to create components and very large scale integration (VLSI) or ultra large scale integration (ULSI) circuits. Equally well known is that the patterns defining such openings are typically created by optical lithographic processes that require precise alignment with prior levels to accurately contact the active devices located in those prior levels.

It is also well known that alignment of one pattern layer to previous layers is done with the assistance of special alignment patterns (i.e., alignment marks) designed onto each mask level. When these special patterns are aligned, it is accepted that the remainder of the circuit patterns are also correctly aligned. The adjustment of the image of the mask being exposed to the previously produced patterns was originally performed by human operators, who compared the image locations under a microscope and adjusted the position of the mask to bring it into alignment with the wafer patterns. Decreasing feature sizes and the increasing number of alignments per wafer, however, have promoted the development of automatic alignment systems for use with projection aligners.

One type of conventional automatic alignment procedure involves the use of alignment marks consisting of two rectangular patterns, which are parallel to the

directions of the stage motion. In most instances, these alignment marks are formed in the kerf or "street" that separates the individual integrated circuits formed on the semiconductor wafer. Two corresponding rectangular patterns are located on the reticle, and their image is projected onto the wafer. The superimposed alignment target and the reticle image are reflected back into the main optical element of the aligner, and then into an on-axis microscope. The image from the microscope is focused onto the face of a TV camera and is subsequently digitized into a form that can be analyzed by a computer. When alignment is achieved, a signal is obtained.

In conventional processes, alignment marks are formed in the same level of the semiconductor wafer where the active regions are formed. The active regions typically include active devices, for example: gates, field oxides and source and drain regions. An oxide is then usually deposited over the active devices and planarized to form the base for the next level. In subsequent levels, however, the method of depositing a polished metal in the contact opening over another metal results in a mirror, which makes seeing the alignment mark with the automatic alignment device difficult. Methods have been presented that address these problems. However, other problems still remain due primarily to the design of the alignment mark itself.

In the past, aluminum was deposited in the contact openings over the barrier layer. However, some fabrication processes now use a combination of tungsten deposited within the contact opening over a barrier layer of titanium/titanium nitride (Ti/TiN). An aluminum/Ti/TiN metal stack is then deposited over the tungsten. Unfortunately, the use of tungsten has certain disadvantages associated with its use in conventionally designed alignment marks.

In conventional alignment mark designs, the overall dimensions are generally large when compared to the dimensions of the contact openings or vias. Due to the alignment mark's relatively large dimensions, the titanium/titanium nitride layer is often subjected to structural stresses that cause the barrier layer to crack at a microscopic level. The presence of these microcracks provide potential reaction sites for tungsten hexafluoride, which is used to deposit tungsten within the contact openings during a chemical vapor deposition process. The reaction of the tungsten hexafluoride in the

microcracks of the Ti/TiN layer can often result in flaking of the Ti/TiN. This flaking can then cause large particles of Ti/TiN, often coated with tungsten, to contaminate the semiconductor wafer.

The size of the alignment marks are a basic design feature of the stepper created by the stepper manufacturer; thus, the overall size of the alignment marks cannot be modified by the chip manufacturer. Replacing conventional alignment marks with four narrow trenches defining just the perimeter of the conventional alignment marks has been tried to alleviate the flaking problem. With this configuration, the stresses induced in the Ti/TiN layer are eliminated because of the narrow nature of the trenches. However, with the subsequent chemical/mechanical polishing of the wafer, only a small portion of the trench, if any, remains, which makes seeing or reading the mark extremely difficult for the stepper because of the mirror effect.

Accordingly, what is needed in the art is an alignment mark that does not suffer the deficiencies of conventional alignment marks. The present invention addresses this need.

Summary of the Invention

To address the above-discussed deficiencies of the prior art, the present invention provides a semiconductor wafer having a substrate with an active region and an inactive region located therein and that comprises a dielectric substrate located over the active and inactive regions, and an alignment mark located in the dielectric substrate over the inactive region wherein the alignment mark comprises a plurality of discrete individual marks that cooperate to form a perimeter of the alignment mark.

The present invention therefore introduces, in one embodiment, the broad concept of a semiconductor wafer that provides an alignment mark that comprises a plurality of discrete individual marks that cooperate to form a perimeter of the alignment mark. Thus, the discrete individual marks can allow for more reliable deposition within the marks and substantially reduce the possibility of contamination by Ti/TiN flaking during the fabrication process. Moreover, this particular embodiment provides a mark that can be read by a stepper when a metal stack is formed on a

polished metal, such as tungsten.

In one embodiment, the plurality of discrete individual marks comprise discrete openings located in the dielectric substrate. The geometrical shape of these discrete individual marks may vary, however, in one particular embodiment the marks are rectangular in shape. In a typical application of the present invention, these discrete individual marks comprise discrete openings located in the dielectric substrate and have a conductive material deposited therein. In one aspect of this particular embodiment, the conductive material is metal and is located on a titanium/titanium nitride barrier layer within the discrete openings. In yet another aspect of this particular embodiment, the conductive material is tungsten and has a metal stack deposited thereon that includes an indentation over each of the individual discrete marks. In one embodiment, the metal stack may be comprised of a titanium/titanium nitride layer, an aluminum layer and a titanium nitride layer.

In one advantageous embodiment, the inactive region in which the alignment mark is formed is located in a kerf or "street" of the semiconductor wafer, and in another embodiment, the active region includes a transistor. In yet another embodiment, a contact window is located in the dielectric substrate over the active region; in such embodiments, the contact window may be filled with the same layers as found in the individual alignment marks and will typically contact the active region.

The foregoing has outlined, rather broadly, preferred and alternative features of the present invention so that those skilled in the art may better understand the detailed description of the invention that follows. Additional features of the invention will be described hereinafter that form the subject of the claims of the invention. Those skilled in the art should appreciate that they can readily use the disclosed conception and specific embodiment as a basis for designing or modifying other structures for carrying out the same purposes of the present invention. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the invention in its broadest form.

Brief Description of the Drawings

For a more complete understanding of the present invention, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGURE 1 illustrates a schematic overhead view of a semiconductor wafer having individual integrated circuits formed thereon;

FIGURE 2 illustrates an enlarged overhead view of a conventional alignment mark positioned with respect to an individual integrated circuit;

FIGURE 3 illustrates a schematic, enlarged overhead view of an illustrative embodiment of an alignment mark covered by the present invention and positioned with respect to an individual integrated circuit;

FIGURE 4 illustrates an enlarged, exemplary schematic cross-sectional view of FIGURE 3 taken along the line 4A-4A with contact windows formed therein;

FIGURE 4A illustrates an enlarged, exemplary schematic cross-sectional view of the semiconductor wafer of FIGURE 4 with Ti/TiN and tungsten layers formed thereon; and

FIGURE 4B illustrates an enlarged, exemplary schematic cross-sectional view of the semiconductor wafer of FIGURE 4A after chemical mechanical polishing and deposition of a conventional metal stack formed over the dielectric surface.

FIGURE 4C illustrates an enlarged exemplary schematic cross-sectional view of FIGURE 4B after the deposition of a conventional metal stack formed over the dielectric surface.

Detailed Description

Referring initially to FIGURE 1 there is illustrated a schematic overhead view of a semiconductor wafer 100 having individual integrated circuits 112 formed thereon. The construction of the semiconductor wafer 100 and the formation of the individual integrated circuits 112 thereon are well known to those who are skilled in the art. Also illustrated are schematic representations of alignment marks 110 covered by the present invention that are formed in kerfs 114, often referred to as streets, of the

semiconductor wafer 100 and which are inactive areas of the semiconductor wafer 100. As many as one hundred to two hundred integrated circuits 112 may be formed on a single semiconductor wafer 100, however, these numbers may vary with design technology or application. Upon completion of the integrated circuits 112 fabrication, a cutting tool, such as a diamond knife, is used to cut the individual integrated circuits 112 from the semiconductor wafer 100. The cut is conducted in the kerf 114 of the semiconductor wafer 100, which destroys the alignment marks 110. Thus, the alignment marks 110 are only necessary during the fabrication of the integrated circuits 112 and are destroyed in the process of separating the individual integrated circuits 112.

Turning now to FIGURE 2, there is illustrated an enlarged overhead view of a conventional alignment mark 210 positioned with respect to an integrated circuit 212. In this particular illustration, the alignment mark 210 is comprised of a single continuous rectangular cavity that is formed in the kerf 214 of the semiconductor wafer 200. In relation to its overall size, conventional alignment marks 210 are of significant width. As previously discussed, the use of these conventional alignment marks 210 have caused problems in present day integrated circuit manufacturing processes.

Typical integrated circuit contact openings/vias are of relatively short lengths and narrow widths. Conventional alignment marks 210 have a relatively large width and significant length in relation to integrated circuit vias. The deposition process of forming a Ti/TiN barrier layer in the integrated circuit contact openings or vias causes Ti/TiN to also be deposited in the alignment marks 210. The physical size of conventional alignment marks 210 and the nature of the Ti/TiN material combine to create structural stresses in the Ti/TiN layer. These stresses are known to cause microcracking within the Ti/TiN layer of the alignment marks 210.

During the next stage of manufacture tungsten plugs are created when, in a chemical vapor deposition (CVD) process, tungsten hexafluoride is used to deposit tungsten within the contact openings. Microcracks in the Ti/TiN barrier layer of conventional alignment marks 210 provide reaction sites for the tungsten hexafluoride. This reaction typically results in pieces of the Ti/TiN flaking off and potentially

contaminates the integrated circuits 212 on the semiconductor wafer 200. This contamination may interfere with subsequent deposition processes, thereby decreasing the integrated circuit yield. This decrease in yield, of course, decreases the efficiency of the fabrication process, which in turn, increases the costs associated with the production of these integrated circuits.

Referring now to FIGURE 3, there is illustrated a schematic, enlarged overhead view of an illustrative embodiment of an alignment mark 310 covered by the present invention and positioned with respect to an individual integrated circuit 312. In an advantageous embodiment, the alignment mark 310 is located in a dielectric substrate over an inactive region 320 of the semiconductor wafer 300. The alignment mark 310 is comprised of a plurality of discrete individual marks 310a that cooperate to form a perimeter of the alignment mark 310 of the same size as the conventional alignment mark 210 previously described. The location of the alignment mark 310, however, may not necessarily be confined to the kerf 314 of the semiconductor wafer 300, and in other embodiments, the alignment mark 310 may be positioned over other inactive regions of the semiconductor wafer 300. In one advantageous embodiment, the plurality of discrete individual marks 310a is rectangular in shape. It should be noted, however, that these individual discrete marks 310a may be different geometrical shapes, such as other rectilinear or curvilinear shapes.

In one embodiment, the width of the alignment mark 310 may range from about 2 microns to about 10 microns and there is about 4 microns between discrete individual marks 310a. In an alternative embodiment, however, the discrete individual mark's 310a width may be about 10 microns and there is about 4 microns between discrete individual marks 310a.

Due to the significant difference in overall size of these discrete individual marks versus the overall size of the alignment mark, the stress on the Ti/TiN layer is significantly reduced, which may reduce the occurrence of the microcracks in the Ti/TiN layer and thereby, may reduce the amount of contamination in the fabrication process. Therefore, this unique alignment mark can solve the problems caused by using a chemical vapor deposition (CVD) process, which prevents the stepper from reading

the alignment mark, as well as the problems associated with the microcracking and flaking caused by the chemical vapor deposition process used to form the tungsten plug.

Turning now to FIGURE 4, illustrated is an enlarged, exemplary schematic cross-sectional view of FIGURE 3 taken along the line 4A-4A with contact windows 411 formed therein. Shown is a portion of a semiconductor wafer 400 having a dielectric substrate 416 located on a wafer substrate 412. The dielectric substrate 416 comprises an inactive region 420, such as a kerf 414, which is the general area located to the right of the dashed line, and active regions 418 generally designated by the area to the left of the dashed line. In most devices, the active regions 418 may include a gate 419, field oxides regions 421, and source and drain regions, 422,423, respectively associated therewith and electrically connected to other portions of the integrated circuit. As those skilled in the art will understand, contact windows 411 created in the active region 418 provide current access to the gate 419, field oxides 421, etc, which combine to form a transistor. Individual openings 410a created in the inactive region 420 are the plurality of discrete individual marks 310a that form the alignment mark 310 (see FIGURE 3).

Referring now to FIGURE 4A, illustrated is an enlarged, exemplary schematic cross-sectional view of the semiconductor wafer 400 of FIGURE 4 with Ti/TiN and tungsten layers formed thereon. A Ti/TiN barrier layer 413 is deposited on the entire exposed surface of the semiconductor wafer 400 of FIGURE 4. Thus, the Ti/TiN barrier layer 413 is deposited in the contact windows 411 as well as within the individual openings 410a. Those who are skilled in the art will recognize that the Ti/TiN barrier layer 413 is comprised to two separately deposited metal layers. More specifically, the Ti/TiN barrier layer 413 is typically comprised of a titanium nitride layer deposited over a titanium layer. By a chemical vapor deposition process, a conductive metal, which for example may be tungsten, is deposited in the contact windows 411 forming a tungsten plug 417 over the Ti/TiN barrier layer 413. The tungsten deposition process also deposits tungsten 410b conformably in the individual openings 410a. The semiconductor wafer of FIGURE 4A is subjected to a

conventional chemical, mechanical polishing (CMP) process. This CMP process substantially removes the portions of the tungsten layer, which are not located in the contact windows 411 and the individual openings 410a. In addition, the CMP process substantially removes the portions of the Ti/TiN barrier layer 413, which are not located in the contact windows 411 and the individual openings 410a. The CMP process produces a smooth surface on the surface of the dielectric material 416.

Turning now to FIGURE 4B, illustrated is an enlarged, exemplary schematic cross-sectional view of the semiconductor wafer 400 of FIGURE 4A after the above-described CMP process. In the active region 418, the tungsten plugs 417 remain intact in contact windows and are flush with the dielectric surface 416. In the street area 420, the tungsten in the alignment mark 410a form a recess 410c which is shallower than the original mark 410a, but such recesses still produce substantial steps 410d with heights ranging between 0.1 micron and 0.8 micron.

FIGURE 4C illustrates an enlarged exemplary schematic cross-sectional view of FIGURE 4B after the deposition of a conventional metal stack formed over the dielectric surface 416. By a series of conventional deposition processes, a conventional metal stack 415, which may typically comprise layers of Ti/TiN, aluminum and TiN, is formed over both the active and inactive regions 418, 420 of the semiconductor wafer 400. The presence of the depressions 410c in the alignment marks 410a causes corresponding depressions 410e in the surface of the metal stack 415. The depressions 410e provide a mark that can be read or seen by the stepper for alignment purposes. Over the contact windows 422 in the active region 418, the metal stack surface 430 shows no indentation and is of mirror quality. In an advantageous embodiment, the size of the individual openings 410a is large enough to leave a recess 410e in the metal stack 415 when it is deposited over tungsten metal 410b, yet small enough to prevent the problems associated with microcracking of the Ti/TiN layer 413 in conventional alignment marks 210 (see FIGURE 2). The recesses 410e resulting from the plurality of individual openings 410a provide the necessary definition for the stepper to discern the perimeter of the alignment mark 410.

From the foregoing, it is seen that the present invention provides a

semiconductor wafer having a substrate with an active region and an inactive region located therein and that comprises a dielectric substrate located over the active and inactive regions, and an alignment mark located in the dielectric substrate over the inactive region wherein the alignment mark comprises a plurality of discrete individual marks that cooperate to form a perimeter of the alignment mark. The present invention therefore introduces the broad concept of a semiconductor wafer that provides an alignment mark that comprises a plurality of discrete individual marks that cooperate to form a perimeter of the alignment mark. Thus, the discrete individual marks can allow for more reliable deposition within the marks and substantially reduce the possibility of contamination by Ti/TiN flaking during the fabrication process. Moreover, this particular embodiment provides a mark that can be read by a stepper when a metal stack is formed on a polished metal, such as tungsten.

Although the present invention has been described in detail, those skilled in the art should understand that they can make various changes, substitutions and alterations herein without departing from the spirit and scope of the invention in its broadest form.

Claims:

1. A semiconductor wafer having a substrate with an active region and an inactive region located therein, comprising:

a dielectric substrate located over said active and inactive regions; and

an alignment mark located in said dielectric substrate over said inactive region and comprised of a plurality of discrete individual marks that cooperate to form a perimeter of said alignment mark.

2. The semiconductor wafer recited in Claim 1 wherein said plurality of discrete individual marks are comprised of discrete openings located in said dielectric substrate.

3. The semiconductor wafer recited in Claim 1 wherein said plurality of discrete individual marks comprise discrete openings located in said dielectric substrate having a conductive material deposited therein.

4. The semiconductor wafer recited in Claim 3 wherein said conductive material is metal and is located on a titanium/titanium nitride barrier layer within said discrete openings.

5. The semiconductor wafer recited in Claim 3 wherein said conductive material is tungsten and has a metal stack deposited thereon, said metal stack including an recess over each of said individual discrete marks.

6. The semiconductor wafer recited in Claim 5 wherein said metal stack comprises a titanium/titanium nitride layer, an aluminum layer and a titanium nitride layer.

7. The semiconductor wafer recited in Claim 1 wherein said inactive region is located in a kerf of said semiconductor wafer.

8. The semiconductor wafer recited in Claim 1 wherein said active region includes a transistor.

9. The semiconductor wafer recited in Claim 1 wherein a contact window is located in said dielectric substrate over said active region.

10. The semiconductor wafer recited in Claim 1 wherein each of said plurality of discrete individual marks has a rectangular shape.

11. A method for manufacturing a semiconductor wafer having a substrate with an active region and an inactive region located therein, comprising:

forming a dielectric substrate located over said active and inactive regions; and

forming an alignment mark in said dielectric substrate over said inactive region, said step of forming said alignment mark comprising the steps of forming a plurality of discrete individual marks to form a perimeter of said alignment mark.

12. The method recited in Claim 11 wherein said step of forming a plurality of discrete individual marks includes the step of forming discrete openings in said dielectric substrate.

13. The method recited in Claim 11 wherein said step of forming a plurality of discrete individual marks includes the steps of forming discrete openings located in said dielectric substrate, forming a conductive material in said discrete openings, and removing a portion of said conductive material by a chemical, mechanical polishing process.

14. The method recited in Claim 13 wherein said conductive material is metal and is located on a titanium/titanium nitride
barrier layer within said discrete openings.

15. The method recited in Claim 13 wherein said metal is tungsten and said method further comprises the step of forming a metal stack over said tungsten and forming an recess in said metal stack over each of said discrete individual marks.

16. The method recited in Claim 15 wherein said step of forming a metal stack includes the steps of forming a titanium /titanium nitride layer, an aluminum layer and a titanium nitride layer.

17. The method recited in Claim 11 wherein said step of forming said inactive region includes forming said inactive region in a kerf of said semiconductor wafer.

18. The method recited in Claim 11 further comprising the step of forming a transistor in said active region.

19. The method recited in Claim 11 further comprising the step of forming a contact window in said dielectric substrate over said active region.

20. The method recited in Claim 11 wherein said step of forming a plurality of discrete individual marks includes the step of forming a plurality of discrete individual marks each having a rectangular shape.