WHAT IS CLAIMED IS:

1. An electronic device, comprising:

a semiconductor memory device configured to store process information and to output the process information to outside of the semiconductor memory device; and

a host configured to read the process information from the semiconductor memory device, and to:

select one of a plurality of operation modes depending on the process information, and

set an operation mode of the semiconductor memory device,

wherein the process information is information indicating whether a process used to manufacture the semiconductor memory device is an enhanced process or a legacy process,

wherein the plurality of operation modes define a response characteristic of the semiconductor memory device,

wherein the response characteristic defines a latency, by which data are output from the semiconductor memory device in response to a read command, and

wherein the process information is programmed in the semiconductor memory device as part of a process of manufacturing the semiconductor memory device.

2. The electronic device as claimed in claim 1, wherein the process information corresponds to process information applied to a peripheral circuit to control a cell array of the semiconductor memory device.

3. The electronic device as claimed in claim 1 or claim 2, wherein the semiconductor memory device includes a program component for storing the process information.

4. The electronic device as claimed in claim 3, wherein the process information is output through a mode register read by the host.

5. The electronic device as claimed in claim 1, wherein the host is configured to write to a mode register of the semiconductor memory device to set the operation mode of the semiconductor memory device.

6. The electronic device as claimed in claim 1, wherein, when the process information corresponds to the enhanced process, the host sets the semiconductor memory device with an operation parameter corresponding to one selected in advance from among the plurality of operation modes.

7. The electronic device as claimed in claim 6, wherein the host performs a training operation for optimizing a reference voltage and a timing of the semiconductor memory device set with the operation parameter.

8. The electronic device as claimed in any one of the previous claims, wherein the plurality of operation modes define a plurality of respectively different latencies by which data are output in response to the read command of the semiconductor memory device.

9. The electronic device as claimed in any one of claims 1 to 3, wherein the semiconductor memory device includes a mode register set storing information about one or more of an operating voltage or an operating speed corresponding to the selected operation mode.

10. A method for setting a semiconductor memory device, the method comprising:

reading process information from the semiconductor memory device, wherein the process information is programmed in the semiconductor memory device as part of a process of manufacturing the semiconductor memory device;

determining whether the process information indicates an enhanced process or a legacy process;

determining a latency by which data are output in response to a read command of the semiconductor memory device, depending on the determination result; and

setting a mode register set of the semiconductor memory device such that the semiconductor memory device operates depending on the determined latency or the determined operating voltage.

11. The method as claimed in claim 10, wherein:

the semiconductor memory device includes a cell array in which the data are stored, and a peripheral circuit configured to control the cell array and to control an input/output of the data, and

the process information corresponds to a process used to manufacture the peripheral circuit.

12. The method as claimed in claim 10 or claim 11, wherein the enhanced process corresponds to a high-K metal gate process or a fin field effect transistor process.

13. The method as claimed in any one of claims 10 to 12, wherein the reading of the process information is performed by a mode register read for reading the process information stored in the mode register set of the semiconductor memory device.

14. The method as claimed in any one of claims 10 to 12, wherein the reading of the process information is performed by a control operation for reading the process information programmed at a nonvolatile memory element provided in the semiconductor memory device.

15. The method as claimed in any one of claims 10 to 14, wherein the semiconductor memory device includes a dedicated pin for outputting the process information.

16. The method as claimed in any one of claims 10 to 15, further comprising performing a training operation for optimizing a timing and a reference voltage level of the semiconductor memory device, after the mode register set of the semiconductor memory device is set.

17. A semiconductor memory device, comprising:

a cell array including a plurality of DRAM cells to store data;

a peripheral circuit configured to write data in the cell array, or to sense and output data stored in the cell array; and

a mode register set circuit configured to output process information about the peripheral circuit to outside of the semiconductor memory device, and to set an output latency of data and a level of an operating voltage of the peripheral circuit in response to a mode register write request,

wherein the process information is information indicating whether a process used to manufacture the peripheral circuit is an enhanced process or a legacy process, and

wherein the process information is programmed in the semiconductor memory device as part of a process of manufacturing the semiconductor memory device.

18. The semiconductor memory device as claimed in claim 17, wherein the process information is output to the outside in response to a mode register read request from the outside.

19. The semiconductor memory device as claimed in claim 17 or claim 18, further comprising a dedicated pin for outputting the process information to the outside.

20. The semiconductor memory device as claimed in any one of claims 17 to 19, wherein:

the process information is provided by using a flag signal that indicates whether a process used to form the peripheral circuit is an enhanced process or a legacy process, and

the enhanced process includes a high-K metal gate process or a fin field effect transistor process.