

Description

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Method for producing an antifuse and antifuse for the selective electrical connection of adjacent conductive regions

The invention relates to a method for producing antifuses and to an antifuse for the selective electrical connection of adjacent conductive regions.

Fuses are generally understood to be conductive connections which are integrated in an integrated circuit and which can be separated by specific measures after the completion of the circuit, in order to perform specific, individual settings for the integrated circuit. In this case, they maintain their setting even in the absence of a supply voltage, i.e. they are quite generally characterized by a permanent physical connection or separation of two contacts. So-called laser fuses are the most common. These are formed by thin interconnects which can be severed with a laser beam depending on the desired setting and, as a result, the conductive connection is opened.

Antifuses are disclosed for example in "Application-Specific Integrated Circuits", Ch. 4.1, 1997, Addison Wesley Longman, Inc. They are the opposite of a conventional fuse, i.e. they constitute an initially open switch which can be closed by means of a suitable measure, e.g. by the application of programming current. Antifuses usually comprise thin insulating layers between two conductive contacts. They are switched by the insulating layer being made conductive after the application of a programming voltage.

Integrated antifuses generally comprise a dielectric layer which is applied on a contact or interconnect layer and on which a further contact region is

situated. Such antifuse structures are usually produced by a dielectric layer being deposited over the whole area and then being removed again essentially over the whole area, except in the fuse regions defined lithographically, by means of dry etching (RIE: Reactive Ion Etching), so that islands made of dielectric material remain on the contact layer. In this method, the contact or interconnect layers of the bottom interconnect plane which are freed of the dielectric layer by the RIE process are attacked and their surface is altered in an undesirable manner.

Therefore, it is an object of the present invention to provide an improved method for producing antifuses.

This object is achieved by means of the method according to claim 1. Further advantageous embodiments are specified in the dependent claims.

According to the invention, it is provided that antifuses for the selective electrical connection of adjacent conductive regions are produced by firstly a sacrificial layer being applied to the surface of a first conductive region, which is situated in a non-conductive region of a substrate. Said sacrificial layer is firstly patterned e.g. with the aid of a photolithographic method, so that a window is produced above the first conductive region. A fuse layer is applied to the sacrificial layer that has been patterned in this way. Said fuse layer is preferably a dielectric layer. During the subsequent removal of the sacrificial layer, the latter is removed together with the fuse layer deposited thereon, so that the fuse layer remains only in the region of the window previously introduced into the sacrificial layer. A non-conductive layer is applied thereon, which layer is provided with contact openings into which conductive material is introduced in order to form a second conductive region.

This production method has the advantage that open conductive regions are not at any time exposed to an etching method or another harmful process by which they can be attacked and damaged. Moreover, this method
5 constitutes a simple production method by which both standard contacts and antifuse contacts can be jointly produced in a process sequence in a simple manner.

In a particular embodiment, it is provided that the
10 fuse layer is formed from a dielectric material and furthermore has a contact layer via which contact is made between the dielectric material of the fuse layer and of the second conductive region. This has the advantage that the contact layer can be used as an
15 etching stop layer during the step of introducing the contact opening into the non-conductive layer. It is thus possible to avoid the situation in which the dielectric layer is etched through in the event of excessively long action of the etching process for the
20 production of the contact holes and an electrical connection is then produced between the first and second conductive regions and, consequently, a fuse contact is not formed.

25 In a preferred embodiment, it is provided that the removal of the sacrificial layer furthermore comprises previously freeing the surface of said sacrificial layer of the fuse layer with the aid of a CMP method (Chemical Mechanical Polishing). As a result, the
30 sacrificial layer is more easily accessible to a subsequent selective etching process, in which the etchant is chosen such that it does not attack the fuse layer. If the fuse layer situated on the sacrificial layer were not removed by a CMP method, it would be
35 expedient to carry out a further masking step before an etching process for jointly removing the fuse layer and the sacrificial layer. This masking step is then necessary in order to protect the fuse layer on the first conductive region against the etching process,

because the etchant to be used etches fuse layer and sacrificial layer.

5 The invention is explained in more detail with reference to the accompanying drawings, in which:

Figure 1 shows a process for producing an antifuse, Figures 1a to 1e representing cross sections through the semiconductor structure according to the invention
10 after different process steps; and
Figure 2 diagrammatically shows an antifuse which has been produced by the method according to Figure 1.

15 The structures shown in the figures are not to scale.

The production method shown in Figure 1 is carried out on a substrate material which is preferably processed with the aid of standard planar technology in which a sequence of individual processes is carried out which
20 each act on the wafer surface over the whole area and lead to the local alteration of the semiconductor material in a targeted manner by way of suitable masking layers.

25 The starting material used is a preprocessed substrate wafer (not shown) preferably essentially made of silicon, on the surface of which is situated an oxide layer 1, into which are introduced conductive regions 2, 2' made of tungsten, the surfaces of which are
30 uncovered. A sacrificial layer 3 is applied to this surface of the substrate pretreated in this way. The sacrificial layer 3 may comprise BPSG, BSG, polysilicon, amorphous silicon or correspondingly different materials depending on the etching chemistry.
35 The sacrificial layer 3 is preferably patterned with the aid of a photolithographic process. In this case, a photoresist layer 4 is applied to the sacrificial layer 3 and patterned photolithographically, so that the sacrificial layer 3 is not covered by the photoresist

layer 4 over the conductive regions 2, 2' on which an antifuse structure is intended to be formed.

As shown in Figure 1b, through this window in the resist layer 4, the sacrificial layer 3 is uncovered down to the surface of the conductive region 2. The photoresist layer 4 is then removed and a dielectric layer 5 and a contact-making layer 6 are subsequently applied over the whole area. The dielectric layer 5 is preferably composed of a dielectric material such as Si_3N_4 , SiON or SiO_2 , but it is also possible to use other dielectric materials. The contact-making layer 6 is composed of a material which is conductive and which forms a stable connection to the dielectric layer 5.

In a subsequent step (Figure 1c), the dielectric layer 5 and the contact-making layer 6 of the surface of the sacrificial layer 3 are removed by a CMP method (Chemical Mechanical Polishing) where the latter is situated on the sacrificial layer 3. The layers 5, 6 in the previously uncovered window of the sacrificial layer 3 remain. A structure is thus obtained in which the sacrificial layer 3 is uncovered and wherein a dielectric layer 5 and a contact-making layer 6 are situated in the regions above the conductive region 2. The dielectric layer 5 and the contact-making layer 6 can also be removed by an etching method, the region above the conductive region 2 then having to be masked in order that the layers 5, 6 are not removed by the etching step.

Figure 1d illustrates a structure as is produced after the removal of the sacrificial layer 3 and the subsequent application of an oxide layer 7. In this case, depending on the material used, the sacrificial layer 3 can be etched using $\text{H}_2\text{SO}_4/\text{HF}$ -containing solutions or comparable etchants.

In the oxide layer 7, windows are then provided as illustrated in Figure 1e, at the locations at which the contact connections are to be made, with the aid of a photolithographic masking and subsequent etching, which
5 windows extend through the oxide layer 7 completely or as far as the contact-making layer 6, depending on whether a simple contact connection of the conductive region 2' situated below the oxide layer is intended to be made or an antifuse structure is intended to be
10 formed. The etching method or the etchants of the etching process are chosen such that the etching process ends in the case of the antifuse structure either after the etching-through of the oxide layer 7 in a manner defined by the etching time or after the
15 contact-making layer 6 is reached. In this case, the contact-making layer 6 serves as an etching stop layer, so that the dielectric layer 5 is protected against being etched through. A conductive material, e.g. tungsten, which forms a low-resistance connection to
20 the contact-making layer, is then introduced into the contact-making openings thus produced. Contacts 8, 8' accessible from the surface are formed in this way.

As can be seen from the method sequence described
25 above, it is thus possible to produce both standard contacts 2', 8' and antifuse contacts 2, 8 simultaneously by one production method. In this case, the conductive regions 2, 2' are firstly protected with the sacrificial layer 3 over the whole area and
30 afterward only the regions at which an antifuse structure is to be produced are uncovered and provided with a dielectric layer. As a result, it is possible to avoid the situation in which the conductive regions are exposed to an etching process whereby they can be
35 attacked and damaged. The subsequent processes of introducing contact openings in an oxide layer and filling the contact openings with a conductive material are identical for the production of standard contacts and antifuse structures.

In a preferred production method, it is provided that the dielectric layer is composed of Si_3N_4 , the sacrificial layer is composed of BPSG or BSG, which is removed with the aid of a wet-chemical lift-off method by means of $\text{H}_2\text{SO}_4/\text{HF}$ -containing solutions. Since the etching rate of $\text{H}_2\text{SO}_4/\text{HF}$ -containing solutions in the case of BPSG or BSG is significantly higher than that in the case of Si_3N_4 , the sacrificial layer 3 can be removed virtually with no impairment of the dielectric layer 5.

For the production method according to the invention, it is not necessary to provide a contact-making layer 6. It is suitable, however, as an etching stop layer for the contact-making openings of the conductive region 8, whereby the dielectric layer 5 can be protected against being etched through. With the use of suitable etching chemistry, however, it is also conceivable that the dielectric layer 5 itself can constitute such an etching stop layer, as a result of which the use of the contact-making layer 6 becomes superfluous.

Figure 2 diagrammatically illustrates an antifuse which has been produced according to the method described above. It has a first conductive region 2, which is embedded in an oxide layer 1 on a substrate. A dielectric fuse layer 5 is situated on said first conductive region 2, and covers the first conductive region 2. A precise alignment is not necessary. Situated above the fuse layer 5 is a contact-making layer 6, which is provided for process reasons. It primarily serves to avoid destruction or damage of the fuse layer 2 in subsequent process steps. Situated on the contact-making layer 6 is an oxide layer 7, in which is situated a contact opening which reaches as far as the contact-making layer 6 and into which a conductive material 8, e.g. tungsten, is introduced. It goes without saying that it may be provided that

further conductive regions which, under certain circumstances, are in contact with the conductive region may be provided below the conductive layer 2.

- 5 The features of the invention which are disclosed in the above description, the drawings and the claims may be of importance both individually and in any desired combination for the realization of the invention in its various configurations.

Patent Claims

1. A method for producing an antifuse for the selective electrical connection of adjacent conductive regions (2, 8), characterized by the following steps:
 - application of a sacrificial layer (3) to a first conductive region (2);
 - patterning of the sacrificial layer (3), so that an opening is formed in the sacrificial layer (3) above the first conductive region (2);
 - application of a fuse layer (5, 6) at least in the region of the opening in the sacrificial layer (3);
 - removal of the sacrificial layer (3);
 - application of a non-conductive layer (7);
 - introduction of an opening into the non-conductive layer (7) above the first conductive region (2);
 - introduction of conductive material into the opening for the purpose of forming a second conductive region (8).
2. The method as claimed in claim 1, characterized in that the fuse layer is formed from a dielectric material (5).
3. The method as claimed in claim 1, characterized in that the fuse layer is formed from a layer sequence made of dielectric materials.
4. The method as claimed in one of claims 1 to 3, characterized in that the fuse layer has a contact layer (6).
5. The method as claimed in one of claims 1 to 4, characterized in that the removal of the sacrificial layer (3) comprises the following further step:

- removal of the fuse layer (5, 6) on a surface of the sacrificial layer (3) with the aid of a chemical mechanical grinding method (CMP method).

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6. The method as claimed in one of claims 1 to 5, characterized in that the dielectric layer (5) is formed from one or more of the materials from the group Si_3N_4 , SiON and/or SiO_2 .

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7. The method as claimed in one of claims 1 to 6, characterized in that the sacrificial layer (3) is formed from one of the materials from the group BPSG, BSG, Poly-Si, a-Si, Al, Ti, TiN.

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8. The method as claimed in one of claims 1 to 7, characterized in that the sacrificial layer (3) is removed using an $\text{H}_2\text{SO}_4/\text{HF}$ -containing solution.

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9. The method as claimed in one of claims 1 to 8, characterized in that at least one of the conductive regions (2, 8) is formed from tungsten.

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10. An antifuse characterized in that it is produced by a method as claimed in one of claims 1 to 9.

11. An integrated circuit having an antifuse as claimed in claim 10.

Abstract

Method for producing an antifuse and antifuse for the selective electrical connection of adjacent conductive regions

The invention relates to a method for producing antifuse structures and antifuses by which adjacent conductive regions 2, 8 can be selectively electrically connected. The method comprises the application of a sacrificial layer 3 to a first conductive region 2, the patterning of the sacrificial layer 3 with the aid of a photolithographic method, the application of a fuse layer 5, 6, the removal of the sacrificial layer 3, the application of a non-conductive layer 7, the introduction of an opening into the non-conductive layer 7 and the introduction of conductive material 8 into the opening for the purpose of forming a second conductive region 8.

Patent Claims

1. A method for producing an antifuse for the selective electrical connection of adjacent conductive regions (2, 8), characterized by the following steps:
- application of a sacrificial layer (3) to a first conductive region (2);
 - patterning of the sacrificial layer (3), so that an opening is formed in the sacrificial layer (3) above the first conductive region (2);
 - application of a fuse layer (5, 6) at least in the region of the opening in the sacrificial layer (3);
 - removal of the fuse layer (5, 6) on a surface of the sacrificial layer (3) with the aid of a chemical mechanical grinding method (CMP method);
 - removal of the sacrificial layer (3);
 - application of a non-conductive layer (7);
 - introduction of an opening into the non-conductive layer (7) above the first conductive region (2);
 - introduction of conductive material into the opening for the purpose of forming a second conductive region (8).
2. The method as claimed in claim 1, characterized in that the fuse layer is formed from a dielectric material (5).
3. The method as claimed in claim 1, characterized in that the fuse layer is formed from a layer sequence made of dielectric materials.
4. The method as claimed in one of claims 1 to 3, characterized in that the fuse layer has a contact layer (6).

5. The method as claimed in one of claims 1 to 4, characterized in that the dielectric layer (5) is formed from one or more of the materials from the group Si_3N_4 , SiON and/or SiO_2 .

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6. The method as claimed in one of claims 1 to 5, characterized in that the sacrificial layer (3) is formed from one of the materials from the group BPSG, BSG, Poly-Si, a-Si, Al, Ti, TiN.

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7. The method as claimed in one of claims 1 to 6, characterized in that the sacrificial layer (3) is removed using an $\text{H}_2\text{SO}_4/\text{HF}$ -containing solution.

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8. The method as claimed in one of claims 1 to 7, characterized in that at least one of the conductive regions (2, 8) is formed from tungsten.

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9. An antifuse characterized in that it is produced by a method as claimed in one of claims 1 to 8.

10. An integrated circuit having an antifuse as claimed in claim 9.