Description

Field of the invention

This invention relates to the fabrication of semiconductor integrated circuits and, more particularly, to such semiconductor circuits that are gettered with phosphorus.

Background of the invention

A variety of very-large-scale-integrated (VLSI) circuits of practical importance include transistor devices with short channel lengths and with shallow source and drain pn junctions. Typically, electrical interconnections for the transistors are supplied by first and second metallization levels which are insulated from each other by a second level insulating layer, such as a phosphorus-doped glass layer. The shallow junctions, in the case of n-channel MOS transistors, are ordinarily achieved by doping the source and drain regions in the silicon body with the impurity arsenic rather than phosphorus, which diffuses more rapidly than arsenic. With extremely shallow junction depths, the problem arises that metals such as aluminum included in contact window portions of the device, to make electrical connections to the source and drain regions in the semiconductor, undesirably penetrate down through the junctions during required heating steps and consequently degrade the performance of the transistors. To counteract this problem, a polycrystalline silicon (polysilicon) contact electrode layer is deposited in the contact windows prior to the deposition of the aluminum metal thereon, which polysilicon contact layer suppresses the penetration of the aluminum to the junction. The polysilicon contact electrode layer is typically doped with phosphorus to supply both a desirably higher electrical conductivity to the polysilicon and a desirable source of phosphorus for the gettering of impurities during relatively high temperature gettering treatments, typically at a temperature of 1000 degrees C. While such high temperature gettering using phosphorus is quite important, it is found that this prior art gettering technique limits the packing density of neighboring devices in the integrated circuit owing to lateral diffusion of the phosphorus through the semiconductor body. That is, a minimum spacing between neighboring devices must be preserved to avoid interactions caused by this lateral diffusion. A purpose of this invention is to reduce the necessary minimum spacing where high temperature gettering with phosphorus is used, thereby allowing a greater packing density of neighboring devices even where phosphorus gettering is used.

Patent Abstracts of Japan, Vol. 7, Number 233 (E-204) page 1378, October 15, 1983, describes a method of gettering a semiconductor body prior to formation of transistor structures, simply by coating only the top surface of the body with a thick oxide layer that can act as a mask against phosphorus diffusion and introducing phosphorus into the body at an elevated temperature through its (uncoated) bottom surface. After the gettering, conventional processes are used to form transistor structures.

Summary of the invention

In order to reduce the distance between neighboring integrated circuit MOS transistor devices without shorting them, each of the polysilicon source and drain electrode contacts is doped with the impurity arsenic or antimony (rather than phosphorus). Then, the problem remains of how to perform a phosphorus gettering process after the formation of gate, source, and drain electrodes. In accordance with this invention, this gettering is accomplished by means of a high-temperature treatment in an atmosphere containing phosphorus at a time when (1) a polysilicon layer for the source and drain electrodes has been formed on the top surface but has not yet been patterned, (2) the entire front surface, but not the back (bottom) surface, of the semiconductor body is protected against phosphorus penetration by means of a sacrificial protective layer, and (3) the back surface of the semiconductor is exposed.

Thus, gettering occurs through the bottom of the workpiece while avoiding exposure of the top of the workpiece to the phosphorus. Also, during the gettering the polysilicon layer and the sacrificial protective layer mechanically prevent an insulating layer on the top surface from flowing which would distort the contour of the polysilicon layer. After the gettering, the sacrificial protective layer is removed.

Figs. 1—8 illustrate in cross section various successive stages in the fabrication of an integrated circuit in accordance with one embodiment of the invention.

Detailed description

The workpiece shown in Fig. 1 has already experienced several processing steps which are first briefly described. The starting material was a single crystal silicon wafer 12 of substantially uniform p-type conductivity oriented <100>. A relatively thick oxide layer of silicon dioxide, typically about 350 nm (3,500 Angstroms) thick, was thermally grown everywhere on a top major surface 13.5 of the wafer 12, and a uniform boron implant was performed through the field oxide to form a p^+ surface region 13.

The thick oxide layer was then patterned by reactive sputter etching to form field oxide layers 14 on the top major surface 13.5 of the wafer, and arsenic doped p^- region 13.1 was selectively implanted through a protective masking layer to form the structure *10* illustrated in Fig. 1.

Then, a relatively thin gate oxide layer 15 (Fig. 2) was grown, typically to a thickness of about 25 nm (250 Angstroms); and immediately thereafter a polysilicon layer 16, vertically about 150 nm (1,500 Angstroms) thick, was deposited (undoped) over this gate oxide layer 15, to form the structure illustrated in Fig. 2.

Next (Fig. 3), apertures were opened through the polysilicon layer 16 and the gate oxide layer

15, for forming buried contacts, that is, contacts between a first level polysilicon metallization and the top surface 13.5 of the body. For this purpose, reactive sputter etching with chlorine to etch the polysilicon, followed by a mxiture of CHF_3 and oxygen to etch the gate oxide, was used, and a second polysilicon layer 17 was then deposited and implanted with arsenic ions. Then a tantalum silicide layer 18 was deposited to a thickness of typically about 250 nm (2,500 Angstroms, to form the structure *30* illustrated in Fig. 3, including the contacts 18.5 through the oxide layer 15 and the polysilicon layer 16 to the surface region 13.

Next, lithographic patterning to define the gates and gate-level interconnections was accomplished by reactive sputter etching with $CFCl_3$, to etch through the tantalum silicide layer 18, followed by a mixture of chlorine and oxygen to complete the etching through the polysilicon layers 17 and 16. The surface 13.5 of the wafer is thus exposed through an opening or a window 31. As a consequence of the patterning of the tantalum silicide layer 18 and the polysilicon layers 17 and 16, there remain in the structure being built (Fig. 4) polysilicon layer portions 26, 36, 46, and 56, stemming from the original polysilicon layer 16, as well as polysilicon layer portions 27, 37, 47, and 57 stemming from the original polysilicon layer 17, and tantalum silicide layer portions 28, 38, 48, and 58 stemming from the original tantalum silicide layer 18. The layer portions 26, 27, and 28 form the gate electrode of an enhancement transistor being built; the layer portions 36, 37, and 38 form the gate electrode of a next neighboring enhancement transistor being built; the layer portions 46, 47, and 48 from a gate electrode of a depletion mode transistor being built with its source connected to its gate electrode; and the layer portions 56, 57, and 58 form drain interconnection metallization for this depletion transistor.

Then the tantalum silicide is sintered, whereby the impurities in the polysilicon layer portions 27, 37, 47, and 57 diffuse into the polysilicon layer portions 26, 36, 46, and 56 to form separate polysilicon layers 127, 137, 147, and 157, respectively (Fig. 5).

Next, the wafer is thermally reoxidized to grow a protective silicon dioxide layer 25 over the previously exposed portion of the top surface 13.5, as well as to coat the polysilicon and silicide layers with oxides (not shown), and then a source and drain implant is performed with arsenic ions. Thereby in the structure *50* illustrated in Fig. 5, an n^+ impurity region 221 forms the source or drain region of the enhancement transistor being built, an n^+ impurity region 222 forms the source or drain region of the next neighboring enhancement transistor being built, an n^+ impurity region 223 forms the source region of the depletion transistor being built, and an n^+ impurity region 224 forms the drain region of this depletion transistor. As a result of the high temperature of the thermal reoxidation, the doped and undoped polysilicon layer portions stemming from the doped and undoped polysilicon layers 17 and 16 become less distinguishable, and more consolidated and indicated in Fig. 5 by reference numerals 127, 137, 147, and 157.

Next, a P-glass layer 19 (Fig. 6) was deposited from phosphorus doped tetra-ethyl-ortho-silicate (P-TEOS) to a thickness of about two microns; the phossphorus concentration therein was about 5 percent by weight, to within about 0.5 percent. This phosphorus concentration is, in any event, preferably less than about 6 percent, although concentrations as high as about 8 percent can be used. The presence of phosphorus in the layer 19, which is an insulating layer, serves to control the fixed charges (ions) at the interface between the silicon dioxide layer and the top surface of the silicon semiconductor and to suppress undesired migration of ions such as sodium.

The P-glass layer 19 was then densified by heating in a nitrogen ambient. Then a polychrome photoresist was applied everywhere upon the top surface of the P-glass layer for the purpose of plasma planarization with a mixture of CF_4 and oxygen, whereby the thickness of the P-glass layer was reduced to about one micron. The top surface of this polysilicon layer is advantageously substantially planar so that second level aluminum metallization strips can be formed thereon with uniform thickness.

Then the P-glass layer was annealed in steam. Windows were opened through the P-glass layer and the silicon dioxide layer 115 by photolithographic masking and etching to expose the top surface 13.5. For the masking of the P-glass layer, a tri-level resist process was used as described, for example, in a paper by J. M. Moran and D. Maydan entitled "High Resolution, Steep Profile Resist Patterns," published in the *Bell System Technical Journal*, Vol. 58, 1979, pp. 1027—1036, but with a thinner than conventional bottom resist layer (about 1.0 micron thick to within 0.2 micron, rather than the conventional thickness of about 1.8 micron or more). Briefly, this thinner bottom resist layer (without the need for plasma planarization thereof) was found to be desirable to produce reliable and uniform window patterns. For the patterning by etching of the P-glass layer, a mixture of CHF_3 and oxygen was used.

Then a polysilicon contact layer 20 was deposited on the top surface of the structure to a thickness of typically about 250 nm (2,500 Angstroms). Advantageously, the polysilicon contact layer 20 is deposited by chemical vapor deposition, so that it deposits conformally over steps; that is, it deposits with good step coverage over the P-glass layer even though the apertures therein are not smoothed by the usual reflow. In order to minimize the undesirable effects of lateral diffusion of impurities, particularly in the p^+ region 13, and to minimize possible lateral leakage under the field oxide, the polysilicon contact layer was doped by arsenic implantation, typically at about 60 keV to a dose of about 7×10^{15} impurity atoms per square centimeter. Other dopants (other then phosphorus), e.g., antimony, can

be used. The resulting structure *60* is illustrated in Fig. 6.

The use of arsenic or antimony doping in the polysilicon layer *20* is a departure from prior art practice where phosphorus is normally used; the phosphorus, as previously explained, being used in a subsequent gettering process. In accordance with this invention, the gettering process is accomplished as follows.

A protective glass layer 21 (Fig. 7) was then deposited from phosphorus-free TEOS to a thickness of about 300 nm (3,000 Angstroms) in order to cap the structure being built, and thereby also to fill any remaining portions of the apertures in the P-glass layer 19 (not occupied by the polysilicon layer 20). While the layer 21 is preferably undoped, it can have a concentration of as much as 1 or 2 percent phosphorus by weight (such a concentration ordinarily unavoidably resulting from residual contamination of the walls of the chamber in which the undoped TEOS deposition is performed—i.e., the same chamber as that in which the phosphorus doped glass was deposited earlier). All layers of polysilicon, tantalum silicide, and glass (not shown) which have accumulated on the bottom surface of the silicon body 12 are then removed by etching while the entire top surface of the structure is protected by a photoresist layer (not shown).

This photoresist layer was then removed and the structure was subjected to a gettering treatment at about 950 degrees C for about an hour in an ambient containing phosphorus, typically phosphorus tribromide. Owing to the presence of the protective glass layer 21, little if any of the phosphorus from the ambient atmosphere penetrates into the upper surface of the wafer 12, hence no lateral diffusion of phosphorus occurs, and closer spacing between neighboring devices than heretofore possible is attainable.

During the gettering process, a phosphorus doped glass layer 11 (Fig. 7) and an n^+ impurity region 11.5 are formed. Both this phosphorus doped glass layer 11 located on the bottom surface and the (undoped) glass layer 21 located on the top surface were removed by a liquid etching which does not attack silicon. The n^+ region 11.5 was thereafter removed, as by sputter etching with a mixture of CF_4 and oxygen. Then the structure being fabricated was annealed in a hydrogen ambient. Then an aluminum (metallization) layer was deposited to a thickness of about a micron upon the top and bottom surfaces of the structure. The aluminum layer on the top surface together with the polysilicon layer 20 was then patterned in accordance with the desired second level metallization pattern by lithographic resist masking and reactive sputter etching with a mixutre of BCl_3 and Cl_2 followed by pure Cl_2 to complete the etching of the polysilicon. Immediately thereafter, the remaining resist was removed by sputter etching with a mixture of CF_4 and oxygen. Thus (Fig. 8) a patterned aluminum layer 41 on a patterned polysilicon layer 40 was formed on the top surface whereas an unpatterened aluminum layer 51 remains on the bottom surface, to form the structure *80* shown in Fig. 8. A final anneal in a hydrogen ambient was performed.

Note that during the gettering step, despite the high gettering temperature of 950 degrees C, the P-glass layer 19 does not flow because of the presence of the polysilicon layer 20 and the undoped glass layer 21 (Fig. 7) which thus mechanically prevents flow of the P-glass layer 19. Thus, in particular, there is no undesired distortion of the contours of the polysilicon layer 20 in regions of contact with the top surface 13.5 of the semiconductor or in other regions of the apertures in the P-glass layer 19 where the aluminum layer 41 later (Fig. 8) fills in.

In this way, static random access memory (SRAM) circuits were successfully built and tested with 1.0 micron design rules. Fig. 8 depicts an illustrative portion of such circuit, with a source region 221 and a polysilicon gate electrode 127 of one enhancement transistor, together with a source region 222 and polysilicon gate electrode 137 of a next neighboring enhancement transistor. The distance d_1 between the proximate edges of the gate electrode 127 and the polysilicon layer 40—serving as a source contact electrode—was about 1.0 micron, i.e., the minimum feature size of the 1.0 micron design rules; the width d_2 of this source contact electrode was about 1.1 micron (corresponding to the size of the aperture in the P-glass layer 19); the distance d_3 between proximate edges of this contact electrode and the field oxide layer 14—i.e., the remaining lateral thickness of the P-glass layer 19 thereat—was about 0.2 micron; the width d_4 of the field oxide layer 14 was about 1.0 micron; and the distance d_5 between proximate edges of this field oxide layer 14 and the source contact electrode of the next neighboring transistor was about 0.2 micron, i.e., approximately the same as d_3. The distance d_6 that the source region 221 tucked under the field oxide layer 14 was about 0.25 micron, and similarly the vertical depth of the source region 221 was also about 0.25 micron. On the other hand, a phosphorus (instead of arsenic) doped polysilicon electrode layer 40 (even though the source and drain regions were doped with arsenic) was found to cause the source region 221 to tuck under the field oxide to such a lateral extent that it overlaps the source region 222, whereby an undesirable short circuit formed between these source regions 221 and 222. An exemplary figure of merit for the dense packing in the structure *80* is the distance $(d_3+d_4+d_5)$ of closest approach between the edges of next neighboring polysilicon electrode contacts, that is, about $0.2+1.0+0.2=1.4$ micron.

Claims

1. A method of fabricating a semiconductor integrated circuit integrated at a top major surface of a semiconductor body, the circuit

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Claims

1. A method of fabricating a semiconductor integrated circuit integrated at a top major surface of a semiconductor body, the circuit

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including MOS transistors having polysilicon source and drain electrodes, characterized by

forming a polysilicon layer (20), for the source and drain electrodes, upon the sidewalls and the bottom surfaces of apertures extending through an insulating layer (19) on the top surface, whereby the polysilicon layer makes contact with surface regions of the body which are doped with arsenic or antimony and are located at the bottom of each of the apertures, and

gettering the body with phosphorus by heating the body at an elevated temperature for a prescribed time duration in an atmosphere containing phosphorus at a time when the top surface, but not the bottom surface, of the body is protected against the penetration of phosphorus by means of a sacrificial glass layer (21) which has a sufficiently low phosphorus concentration that essentially no phosphorus diffuses from it into the body which would decrease the transistor packing density, and at said time the polysilicon layer (20) has been formed on the top surface of the body but has not yet been patterned, so that during the gettering the polysilicon layer and the sacrificial glass layer mechanically prevent the insulating layer (19) from flowing which would distort the contours of the polysilicon layer.

2. The method of claim 1 including:

removing, after the gettering, the sacrificial glass layer (21) to expose the polysilicon layer (20);

depositing a metal layer (41) upon the thus exposed polysilicon layer, and

patterning the metal layer and the polysilicon layer in accordance with the circuit.

3. The method of claim 2 in which the metal is aluminum.

4. The method of claim 1 in which the insulating layer (19) is a glass layer doped with phosphorus to a concentration of about 5 percent by weight and in which the surface regions and the polysilicon layer are doped with arsenic or antimony.

5. The method of claim 4 in which the gettering temperature is about 950 degrees C, the sacrificial protective layer being a glass layer containing less than about 2 percent phosphorus by weight and having a sufficient thickness whereby any significant flow of the glass layer (19) doped with phosphorus into the apertures during the gettering is mechanically prevented by the presence of the polysilicon layer and the sacrificial glass layer.

Patentansprüche

1. Verfahren zum Herstellen einer intergrierten Halbleiterschaltung, die in eine obere Hauptfläche eines Halbleiterkörpers integriert ist und MOS-Transistoren mit Source- und Drain-Elektroden aus polykristallinem Silicium ("Polysilicium") aufweist, gekennzeichnet durch

Herstellen einer Polysiliciumschicht (20) für die Source- und Drain-Elektroden auf den Seitenwänden und den Bodenflächen von Öffnungen, die sich durch eine Isolierschicht (19) auf der oberen Fläche hindurcherstrecken, wodurch die Polysiliciumschicht Kontakt mit Oberflächenzonen des Körpers bildet, die mit Arsen oder Antimon dotiert am Boden einer jeden der Öffnungen gelegen sind, und

Gettern des Körpers mit Phosphor durch Erwärmen des Körpers während einer vorgeschriebenen Zeitspanne auf erhöhte Temperatur in einer Atmosphäre, die Phosphor zu einer Zeit enthält, wenn die obere Fläche des Körpers, jedoch nicht dessen untere Fläche, gegen das Eindringen von Phosphor durch eine Opfer-Glasschicht (21) geschützt ist, die hinreichend niedrige Phosphorkonzentration besitzt derart, daß im wesentlichen kein Phosphor aus ihr in den Körper diffundiert, was die Transistorpackungsdichte erniedrigen würde, sowie Phosphor zu der Zeit enthält, zu der die Polysiliciumschicht (20) auf der oberen Fläche des Körpers gebildet, aber noch nicht gemustert worden ist, so daß während des Getterns die Polysiliciumschicht und die Opfer-Glasschicht mechanisch die Isolierschicht (19) an einem Fließen hindern, das die Konturen der Polysiliciumschicht verzeichnen würde.

2. Verfahren nach Anspruch 1, umfassend

nach dem Gettern erfolgendes Entfernen der Opfer-Glasschicht (21), um die Polysilicuimschicht (20) freizulegen,

Niederschlagen einer Metallschicht (41) auf die solcherart freigelegte Polysiliciumschicht und

Mustern der Metallschicht und der Polysiliciumschicht entsprechend der Schaltung.

3. Verfahren nach Anspruch 2, bei dem das Metall Aluminium ist.

4. Verfahren nach Anspruch 1, bei dem die Isolierschicht (19) eine mit Phosphor auf eine Konzentration von etwa 5 Gewichtsprozent mit Phosphor dotierte Glasschicht ist und

die Oberflächenzonen und die Polysiliciumschicht mit Arsen oder Antimon dotiert sind.

5. Verfahren nach Anspruch 4, bei dem die Getterungstemperatur etwa 950°C beträgt,

die Opfer-Schutzschicht eine Glasschicht mit weniger als 2 Gewichtsprozent Phosphor ist und hinreichende Dicke besitzt, wodurch jeglicher nennenswerte Fluß der phosphordotierten Glasschicht (19) in die Öffnungen während der Getterung mechanisch verhindert ist durch die Gegenwart der Polysiliciumschicht und der Opfer-Glasschicht.

Revendications

1. Un procédé de fabrication d'un circuit intégré à semiconducteurs, intégré sur une surface principale supérieure d'un bloc de semiconducteur, le circuit comprenant des transistors MOS ayant des électrodes de source et de drain en silicium polycrystallin, caractérisé en ce que

on forme une couche de silicium polycristallin (20), pour les électrodes de source et de drain, sur les parois latérales et les surfaces inférieures d'ouvertures qui s'étendent à travers une couche isolante (19) sur la surface supérieure, grâce à quoi la couche de silicium polycristallin vient en contact avec des régions de surface du bloc qui

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sont dopées avec de l'arsenic ou de l'antimoine et qui se trouvent au fond de chacune des ouvertures, et

on soumet le bloc à une opération de piégeage d'impuretés avec du phosphore, en chauffant le bloc à une température élevée pendant une durée déterminée, dans une atmosphère contenant du phosphore, à un moment auquel la surface supérieure du bloc, mais non la surface inférieure, est protégée contre la pénétration de phosphore au moyen d'une couche de verre perdue (21) qui a une concentration en phosphore suffisamment faible pour qu'il n'y ait pratiquement aucune diffusion de phosphore vers le bloc, à partir de cette couche, qui diminuerait la densité d'implantation des transistors, et à ce moment la couche de silicium polycristallin (20) a été formée sur la surface supérieure du bloc, mais un motif n'a pas encore été défini dans cette couche, ce qui fait que pendant le piégeage d'impuretés, la couche de silicium polycristallin et la couche de verre perdue empêchent mécaniquement un écoulement de la couche isolante (19) qui déformerait les contours de la couche de silicium polycristallin.

2. Le procédé de la revendication 1 comprenant les opérations suivantes:

après l'opération de piégeage d'impuretés, on enlève la couche de verre perdue (21) pour mettre à nu la couche de silicium polycristallin (20);

on dépose une couche de métal (41) sur la couche de silicium polycristallin qui est ainsi mise à nu, et

on définit des motifs dans la couche de métal et la couche de silicium polycristallin conformément au circuit.

3. Le procédé de la revendication 2, dans lequel le métal est de l'aluminium.

4. Le procédé de la revendication 1, dans lequel la couche isolante (19) est une couche de verre qui est dopée avec du phosphore jusqu'à une concentration d'environ 5% en poids, et dans lequel les régions de surface et la couche de silicium polycristallin sont dopées avec de l'arsenic ou de l'antimoine.

5. Le procédé de la revendication 4, dans lequel la température de piégeage d'impuretés est d'environ 950°C, la couche de protection perdue étant une couche de verre qui contient moins d'environ 2% de phosphore en poids et qui a une épaisseur suffisante, grâce à quoi la présence de la couche de silicium polycristallin et de la couche de verre perdue empêche mécaniquement tout écoulement notable de la couche de verre (19) dopée avec du phosphore dans les ouvertures, pendant le piégeage d'impuretés.

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