METHOD FOR INTEGRATED CIRCUIT FABRICATION USING PITCH MULTIPLICATION

Background of the Invention

Field of the Invention

This invention relates generally to integrated circuit fabrication and, more particularly, to masking techniques.

Description of the Related Art

As a consequence of many factors, including demand for increased portability, computing power, memory capacity and energy efficiency in modern electronics, integrated circuits are continuously being reduced in size. To facilitate this size reduction, the sizes of the constituent features, such as electrical devices and interconnect line widths, that form the integrated circuits are also constantly being decreased.

The trend of decreasing feature size is evident, for example, in memory circuits or devices such as dynamic random access memories (DRAMs), static random access memories (SRAMs), ferroelectric (FE) memories, etc. To take one example, DRAM typically comprises millions of identical circuit elements, known as memory cells. In its most general form, a memory cell typically consists of two electrical devices: a storage capacitor and an access field effect transistor. Each memory cell is an addressable location that can store one bit (binary digit) of data. A bit can be written to a cell through the transistor and read by sensing charge on the storage electrode from the reference electrode side. By decreasing the sizes of constituent electrical devices and the conducting lines that access then, the sizes of the memory devices incorporating these features can be decreased. Additionally, storage capacities can be increased by fitting more memory cells into the memory devices.

The continual reduction in feature sizes places ever greater demands on techniques used to form the features. For example, photolithography is commonly used to pattern features, such as conductive lines, on a substrate. The concept of pitch can be used to describe the size of these features. Pitch is defined as the distance between an identical point in two neighboring features. These features are typically defined by spacings between adjacent features, which are typically filled by a material, such as an insulator. As a result, pitch can be viewed as the sum of the width of a feature and of the width of the space separating that feature from a neighboring feature. Due to factors such as optics and light or radiation wavelength, however, photolithography techniques each have a minimum pitch below which a particular photolithographic technique cannot reliably

form features. Thus, the minimum pitch of a photolithographic technique can limit feature size reduction.

Pitch doubling is one method proposed for extending the capabilities of photolithographic techniques beyond their minimum pitch. Such a method is illustrated in Figures 1A-1F and described in U.S. Patent No. 5,328,810, issued to Lowrey *et al.* With reference to Figure 1A, photolithography is first used to form a pattern of lines 10 in a photoresist layer overlying a layer 20 of an expendable material and a substrate 30. As shown in Figure 1B, the pattern is then transferred by an etch step (preferably anisotropic) to the layer 20, forming placeholders, or mandrels, 40. The photoresist lines 10 can be stripped and the mandrels 40 can be isotropically etched to increase the distance between neighboring mandrels 40, as shown in Figure 1C. A layer 50 of material is subsequently deposited over the mandrels 40, as shown in Figure 1D. Spacers 60, *i.e.*, material extending or originally formed extending from sidewalls of another material, are then formed on the sides of the mandrels 40 by preferentially etching the spacer material from the horizontal surfaces 70 and 80 in a directional spacer etch, as shown in Figure 1E. The remaining mandrels 40 are then removed, leaving behind only the spacers 60, which together act as a mask for patterning, as shown in Figure 1F. Thus, where a given pitch formerly included a pattern defining one feature and one space, the same width now includes two features and two spaces defined by the spacers 60. As a result, the smallest feature size possible with a photolithographic technique is effectively decreased.

It will be appreciated that while the pitch is actually halved in the example above, this reduction in pitch is conventionally referred to as pitch "doubling," or, more generally, pitch "multiplication." That is, conventionally "multiplication" of pitch by a certain factor actually involves reducing the pitch by that factor. The conventional terminology is retained herein.

Because the layer 50 of spacer material typically has a single thickness 90 (see Figures 1D and 1E) and because the sizes of the features formed by the spacers 60 usually corresponds to that thickness 90, pitch doubling typically produces features of only one width. Circuits, however, often employ features of different sizes. For example, random access memory circuits typically contain arrays of memory cells and logic circuits in the so-called "periphery." In the arrays, the memory cells are typically connected by conductive lines and, in the periphery, the conductive lines typically contact landing pads for connecting arrays to logic. Peripheral features such as landing pads, however, can be larger than the conductive lines. In addition, periphery electrical devices such as transistors can be larger than electrical devices in the array. Moreover, even if peripheral features can be formed with the same pitch as the array, the flexibility required to define circuits will typically not be possible using a single mask, particularly if the patterns are limited to those that can be formed along the sidewalls of patterned photoresist.

Some proposed methods for forming patterns at the periphery and at the array involve etching a pattern into the array region of a substrate and into periphery of the substrate separately. Thus, a pattern in the array is first formed and transferred to the substrate using one mask and then another pattern in the periphery is formed and separately transferred to the substrate using another mask. Because such methods form patterns using different masks at different locations on a substrate, they are limited in their ability to form features that require overlapping patterns, such as when a landing pad overlaps an interconnect line, and yet a third mask may be necessitated to "stitch" two separate patterns with interconnects. Additionally, such a third mask would face even greater challenges with respect to mask alignment due to the fine features defined by the pitch multiplication technique.

Accordingly, there is a need for methods of forming features of different sizes, especially where the features require different overlapping patterns and especially in conjunction with pitch multiplication.

Summary of the Invention

According to one aspect of the invention, a method is provided for semiconductor processing. The method comprises providing a substrate having a primary mask layer overlying the substrate, a temporary layer overlying the primary mask layer and a first photoresist layer overlying the temporary layer. A photoresist pattern is formed in the first photoresist layer. A first pattern, having features derived from features of the photoresist pattern, is formed in the temporary layer. A second photoresist layer is subsequently formed above the level of the first pattern and an other photoresist pattern is formed in the second photoresist layer. The other photoresist pattern and the first pattern are transferred to the primary mask layer to form a mixed pattern in the primary mask layer. The substrate is processed through the mixed pattern in the primary mask layer. It will be appreciated that the substrate can comprise any material or materials to be processed through the primary masking layer.

According to another aspect of the invention, a method is provided for forming an integrated circuit. The method comprises providing a substrate and forming an amorphous carbon layer over the substrate. A first hardmask layer is formed over the first amorphous carbon layer. A temporary layer is formed over the first hardmask layer and a second hardmask layer is formed over the temporary layer.

According to another aspect of the invention, a method is provided for semiconductor fabrication. The method comprises forming a first pattern by pitch multiplication and separately forming a second pattern by photolithography without pitch multiplication. The first and second patterns are transferred to a mask layer and a substrate is etched through the mask layer.

According to yet another aspect of the invention, a method is provided for forming an integrated circuit. The method comprises forming a mask pattern in which a first part of the mask

pattern has a first pitch and a second part of the mask pattern has a second pitch. The first pitch is below a minimum pitch of a photolithographic technique for defining the second pattern. The method also comprises etching a substrate through the mask pattern.

According to another aspect of the invention, a method is provided for forming a memory device. The method comprises forming a pattern of temporary placeholders in a layer over a first carbon layer. A layer of mask material is deposited over surfaces of the temporary placeholders and is then selectively removed from horizontal surfaces of the memory device. The temporary placeholders are selectively removed relative to the mask material to form a pattern of mask material corresponding to features in an array region of the memory device.

According to yet another aspect of the invention, a method is provided for for manufacturing an integrated circuit. The method comprises forming a plurality of mandrel strips. A spacer is formed on sidewalls of each mandrel strip. The mandrel strips are removed to form a pattern of spaced apart spacers. A mask layer is formed in a plane above the spacers and a pattern is formed in the mask layer. The pattern is transferred to the same horizontal plane as the spacers.

According to another aspect of the invention, a method is provided for manufacturing an integrated circuit. The method comprises providing a plurality of spaced-apart lines of a mask material above a substrate, where the mask material is different from photoresist. A plurality of features is defined in a photodefinable material above the substrate by a photolithographic technique. The spaced-apart lines and the plurality of features are replicated in an amorphous carbon layer below the spaced-apart lines.

According to another aspect of the invention, a method is provided for forming a mask pattern to fabricate an integrated circuit. The method comprises providing a plurality of lines of a first mask material. The lines are separated by a first temporary material. The first temporary material is selectively etched. Spaces between the lines are filled with a second temporary material. The second temporary material is selectively etched to open the spaces. A pattern is then formed in a layer of another mask material below the plurality of lines by selectively etching through the spaces.

According to another aspect of the invention, a process is provided for fabricating an integrated circuit. The process comprises providing a masking layer extending over a first and a second region of a partially fabricated integrated circuit. A pattern is formed in the masking layer. A minimum feature size of a portion of the pattern corresponding to the first region is equal to or less than about half a minimum feature size of an other portion of the pattern corresponding to the second region.

According to another aspect of the invention, a partially formed integrated circuit is provided. The partially formed integrated circuit comprises a carbon layer and a plurality of

pitch-multiplied spacers on a level overlying the carbon layer. The spacers have a pitch of about 100 nm or less.

According to yet another aspect of the invention, a partially formed integrated circuit is provided. The partially formed integrated circuit comprises a substrate and a primary mask layer overlying the substrate. The primary mask layer formed of a material different from photoresist. A mask material defining a first pattern is disposed in a first plane overlying the primary mask layer. A photodefinable material defining a second pattern is disposed in a second plane overlying the mask material.

Brief Description of the Drawings

The invention will be better understood from the Detailed Description of the Preferred Embodiments and from the appended drawings, which are meant to illustrate and not to limit the invention, and wherein:

Figures 1A-1F are schematic, cross-sectional side views of partially formed conductive lines, formed in accordance with a prior art pitch doubling method;

Figures 2A-2B are a schematic, cross-sectional top and side views of a partially formed memory device, in accordance with preferred embodiments of the invention;

Figure 3 is a schematic, cross-sectional side view of the partially formed memory device of Figure 2 after forming lines in a selectively definable layer in the array of the memory device, in accordance with preferred embodiments of the invention;

Figure 4 is a schematic, cross-sectional side view of the partially formed memory device of Figure 3 after widening spaces between photoresist lines, in accordance with preferred embodiments of the invention;

Figure 5 is a schematic, cross-sectional side view of the partially formed memory device of Figure 4 after etching through a hard mask layer, in accordance with preferred embodiments of the invention;

Figure 6 is a schematic, cross-sectional side view of the partially formed memory device of Figure 5 after transferring a pattern from the photoresist layer to a temporary layer, in accordance with preferred embodiments of the invention;

Figure 7 is a schematic, cross-sectional side view of the partially formed memory device of Figure 6 after depositing a layer of a spacer material, in accordance with preferred embodiments of the invention;

Figure 8 is a schematic, cross-sectional side view of the partially formed memory device of Figure 7 after a spacer etch, in accordance with preferred embodiments of the invention;

Figure 9 is a schematic, cross-sectional side view of the partially formed memory device of Figure 8 after removing a remaining portion of the temporary layer to leave a pattern of

spacers in the array of the memory device, in accordance with preferred embodiments of the invention;

Figure 10 is a schematic, cross-sectional side view of the partially formed memory device of Figure 9 after surrounding the spacers with a removable material and forming a hard mask layer and a selectively definable layer over the spacers, in accordance with preferred embodiments of the invention;

Figure 11 is a schematic, cross-sectional side view of the partially formed memory device of Figure 10 after forming a pattern in the selectively definable layer in the periphery of the memory device, in accordance with preferred embodiments of the invention;

Figure 12 is a schematic, cross-sectional side view of the partially formed memory device of Figure 11 after etching through the top hard mask layer, in accordance with preferred embodiments of the invention;

Figure 13 is a schematic, cross-sectional side view of the partially formed memory device of Figure 12 after transferring the pattern from the selectively definable layer to the same level as the spacers, in accordance with preferred embodiments of the invention;

Figure 14 is a schematic, cross-sectional side view of the partially formed memory device of Figure 13 after etching the pattern in the periphery and the spacer pattern in the array into an underlying hard mask layer, in accordance with preferred embodiments of the invention;

Figure 15 is a schematic, cross-sectional side view of the partially formed memory device of Figure 14 after transferring the pattern in the periphery and the spacer pattern in the array together to a primary mask layer, in accordance with preferred embodiments of the invention;

Figure 16 is a schematic, cross-sectional side view of the partially formed memory device of Figure 15 after transferring the periphery pattern and the spacer pattern to the underlying substrate, in accordance with preferred embodiments of the invention; and

Figures 17A and 17B are micrographs, as viewed through a scanning electron microscope, of a pattern etched into the array and the periphery, respectively, of a partially formed memory device, formed in accordance with preferred embodiments of the invention.

Detailed Description of the Preferred Embodiments

In addition to problems with forming different size features, it has been found that pitch doubling techniques can have difficulty transferring spacer patterns to a substrate. In particular, in common methods of transferring patterns, both the spacers and the underlying substrate are exposed to an etchant, which preferentially etches away the substrate material. It will be appreciated, however, that the etchants also wear away the spacers, albeit at a slower rate. Thus, over the course of transferring a pattern, the spacers can be worn away by the etchant before the pattern transfer is complete. These difficulties are exacerbated by the trend towards decreasing feature size, which, for example, increasingly leads to higher aspect ratios as the widths of these

trenches decrease. In conjunction with difficulties of producing structures of different feature sizes, these pattern transfer limitations make even more difficult the application of pitch-doubling principles to integrated circuit manufacture.

In view of these difficulties, preferred embodiments of the invention allow for improved pattern transfer and for the formation of different size features in conjunction with pitch doubling. In a first phase of the method, photolithography and pitch doubling are preferably used to form a spacer pattern. This typically forms features of one size in one region of the chip, *e.g.*, the array of a memory chip. In a second phase, photolithography is again performed to form a second pattern in another region of the chip, *e.g.*, the periphery of the memory chip, in a layer overlying the spacer pattern. Both the spacer pattern and the second pattern are then transferred to an underlying primary masking layer, which preferably can be preferentially etched relative to an underlying substrate. The spacer and second patterns are then transferred from the primary masking layer to the underlying substrate in a single step. Thus, patterns for forming different size features, some of which are below the minimum pitch of the photolithographic technique used for patterning, can be formed and these patterns can be successfully transferred to the underlying substrate.

Moreover, because the second pattern is initially formed on a layer overlying the spacer pattern, the second pattern can overlap the spacer pattern. As a result, overlapping features of different sizes, such as conducting lines and landing pads or periphery transistors, can advantageously be formed.

Preferably, the primary masking layer is the masking layer that directly overlies and, due to etch selectivity, is primarily used to perform a process (*e.g.*, etch) on the substrate through the primary masking layer. In particular, the primary masking layer is preferably formed of a material that allows good etch selectivity relative to both the spacer material and the substrate material, so that spacer pattern can effectively be transferred to it; so that the primary masking layer can be selectively removed after processing without harming the substrate; and, when the mask is used for etching the substrate, so that the pattern in it can effectively be transferred to the substrate. Due to its excellent etch selectivity relative to a variety of materials, including oxides, nitrides and silicon, the primary masking layer is preferably formed of carbon and, more preferably, amorphous carbon.

It will be appreciated that a substrate can comprise any material or materials that are to be processed through the primary masking layer. Thus, a substrate can include a layer of a single material, a plurality of layers of different materials, a layer or layers having regions of different materials or structures in them, etc. These materials can include semiconductors, insulators, conductors, or combinations thereof. Typically, the substrate comprises structures or layers ultimately form part of the integrated circuit being fabricated.

It will also be appreciated that transferring a pattern from a first level to a second level involves forming features in the second level that generally correspond to features on the first level. For example, the path of lines in the second level will generally follow the path of lines on the first level and the location of other features on the second level will correspond to the location of similar features on the first level. The precise shapes and sizes of features can vary from the first level to the second level, however. For example, depending upon etch chemistries and conditions, the sizes of and relative spacings between the features forming the transferred pattern can be enlarged or diminished relative to the pattern on the first level, while still resembling the same initial "pattern."

Reference will now be made to the Figures, wherein like numerals refer to like parts throughout. It will be appreciated that Figures 2-16 are not necessarily drawn to scale.

While the preferred embodiments will find application in any context in which features of different sizes are formed on a substrate, in particularly advantageous embodiments, part of the pattern to be transferred to a substrate is formed by pitch multiplication and that has a pitch below the minimum pitch of the photolithographic technique used for processing the substrate. In addition, while the preferred embodiments can be used to form any integrated circuit, they are particularly advantageously applied to form devices having arrays of electrical devices, including logic or gate arrays and volatile and non-volatile memory devices such as DRAM, ROM or flash memory. In such devices, pitch multiplication can be used to form, *e.g.*, transistor gate electrodes and conductive lines in the array region of the chips, while conventional photolithography can be used to form larger features, such as contacts, at the peripheries of the chips. Exemplary masking steps in the course of fabricating a memory chip are illustrated in the Figures.

Figure 2A shows a top view of a partially fabricated integrated circuit, or memory chip, 100. A central region 102, the "array," is surrounded by a peripheral region 104, the "periphery." It will be appreciated that, after fabrication of the integrated circuit 100 is complete, the array 102 will typically be densely populated with conducting lines and electrical devices such as transistors and capacitors. Desirably, pitch multiplication can be used to form features in the array 102, as discussed below. On the other hand, the periphery 104 can have features larger than those in the array 102. Conventional photolithography, rather than pitch multiplication, is typically used to pattern these features, because the geometric complexity of logic circuits located in the periphery 104 makes using pitch multiplication difficult. In addition, some devices in the periphery require larger geometries due to electrical constraints, thereby making pitch multiplication less advantageous than conventional photolithography for such devices.

With reference to Figure 2B, a partially formed integrated circuit 100 is provided. A substrate 110 is provided below various layers 120-160. The substrate 110 will be patterned to form various features and the layers 120-160 will be etched to form a mask for the pattern, as

discussed below. The materials for the layers overlying the substrate 110 are preferably chosen based upon consideration of the chemistry and process condition requirements for the various pattern forming and pattern transferring steps discussed herein. Because the layers between a topmost selectively definable layer 120, which preferably is definable by a lithographic process, and the substrate 110 function to transfer a pattern derived from the selectively definable layer 120 to the substrate 110, the layers between the selectively definable layer 120 and the substrate 110 are preferably chosen so that they can be selectively etched relative to other exposed materials during their etch. It will be appreciated that a material is considered selectively, or preferentially, etched when the etch rate for that material is at least about 5 times greater, preferably about 10 times greater, more preferably about 20 times greater and, most preferably, at least about 40 times greater than that for surrounding materials.

In the illustrated embodiment, the selectively definable layer 120 overlies a first hard mask, or etch stop, layer 130, which overlies a temporary layer 140, which overlies a second hard mask, or etch stop, layer 150, which overlies a primary mask layer 160, which overlies the substrate 110 to be processed (*e.g.*, etched) through a mask. The thicknesses of the layers are preferably chosen depending upon compatibility with the etch chemistries and process conditions described herein. For example, when transferring a pattern from an overlying layer to an underlying layer by selectively etching the underlying layer, materials from both layers are removed to some degree. Thus, the upper layer is preferably thick enough so that it is not worn away over the course of the etch.

In the illustrated embodiment, the first hard mask layer 130 is preferably between about 10-50 nm thick and, more preferably, between about 10-30 nm thick. The temporary layer 140 is preferably between about 100-300 nm thick and, more preferably, between about 100-200 nm thick. The second hard mask layer 150 is preferably between about 10-50 nm thick and, more preferably, about 20-40 nm thick and the primary mask layer 160 is preferably between about 100-1000 nm thick and, more preferably, about 100-500 nm thick.

With reference to Figure 2, the selectively definable layer 120 is preferably formed of a photoresist, including any photoresist known in the art. For example, the photoresist can be any photoresist compatible with 13.7 nm, 157 nm, 193 nm, 248 nm or 365 nm wavelength sytems, 193 nm wavelength immersion systems or electron beam lithographic systems. Examples of preferred photoresist materials include argon fluoride (ArF) sensitive photoresist, *i.e.*, photoresist suitable for use with an ArF light source, and krypton fluoride (KrF) sensitive photoresist, *i.e.*, photoresist suitable for use with a KrF light source. ArF photoresists are preferably used with photolithography systems utilizing relatively short wavelength light, *e.g.*, 193 nm. KrF photoresists are preferably used with longer wavelength photolithography systems, such as 248 nm systems. In other embodiments, the layer 120 and any subsequent resist layers can be formed

of a resist that can be patterned by nano-imprint lithography, *e.g.*, by using a mold or mechanical force to pattern the resist.

The material for the first hard mask layer 130 preferably comprises a silicon oxide (SiO_2), silicon or a dielectric anti-reflective coating (DARC), such as a silicon-rich silicon oxynitride. DARCs can be particularly advantageous for forming patterns having pitches near the resolution limits of a photolithographic technique because they can enhance resolution by minimizing light reflections. It will be appreciated that light reflections can decrease the precision with which photolithography can define the edges of a pattern. Optionally, a bottom anti-reflective coating (BARC) (not shown) can similarly be used in addition to the first hard mask layer 130 to control light reflections.

The temporary layer 140 is preferably formed of amorphous carbon, which offers very high etch selectivity relative to the preferred hard mask materials. More preferably, the amorphous carbon is a form of transparent carbon that is highly transparent to light and which offers further improvements for photo alignment by being transparent to wavelengths of light used for such alignment. Deposition techniques for forming a highly transparent carbon can be found in A. Helmbold, D. Meissner, Thin Solid Films, 283 (1996) 196-203.

As with the first hard mask layer 130, the second hard mask layer 150 preferably comprises a dielectric anti-reflective coating (DARC) (*e.g.*, a silicon oxynitride), a silicon oxide (SiO_2) or silicon. In addition, a bottom anti-reflective coating (BARC) (not shown) can also optionally be used to control light reflections. While the first and the second hard mask layers 130 and 150 can be formed of different materials, these layers are preferably formed of the same material for ease of processing and to minimize the number of different etch chemistries utilized, as described below. Like the temporary layer 140, the primary mask layer 160 is preferably formed of amorphous carbon and, more preferably, transparent carbon.

It will be appreciated that the various layers discussed herein can be formed by various methods known to those of skill in the art. For example, various vapor deposition processes, such as chemical vapor deposition can be used to form the hard mask layers. Preferably, a low temperature chemical vapor deposition process is used to deposit the hard mask layers or any other materials, *e.g.*, spacer material (Figure 7), over the mask layer 160, where the mask layer 160 is formed of amorphous silicon. Such low temperature deposition processes advantageously prevent chemical or physical disruption of the amorphous carbon layer.

Spin-on-coating processes can be used to form the photodefinable layers. In addition, amorphous carbon layers can be formed by chemical vapor deposition using a hydrocarbon compound, or mixtures of such compounds, as carbon precursors. Exemplary precursors include propylene, propyne, propane, butane, butylene, butadiene and acetelyne. A suitable method for

forming amorphous carbon layers is described in U.S. Patent No. 6,573,030 B1, issued to Fairbairn *et al.* on June 3, 2003.

In a first phase of the method in accordance with the preferred embodiments and with reference to Figures 3-9, pitch multiplication in the array of the partially formed integrated circuit 100 is performed. A pattern is formed on the photodefinable layer 120, as shown in Figure 3. The photodefinable layer 120 can be patterned by, *e.g.*, photolithography, in which the layer 120 is exposed to radiation through a reticle and then developed. After being developed, the remaining photodefinable material, photoresist in this case, comprises lines 122, which define spaces 124.

As shown in Figure 4, the widths of the spaces 122 and the photoresist lines 122 can be altered to a desired dimension. For example, the spaces 122 can be widened by etching the photoresist lines 124. The photoresist lines 124 are preferably etched using an isotropic etch, such as a sulfur oxide plasma, *e.g.*, a plasma comprising SO_2, O_2, N_2 and Ar. The extent of the etch is preferably selected so that a resulting line 124a has a width corresponding to the desired spacing of the spacers to be formed, as will be appreciated from the discussion below with respect to Figures 8-16. Advantageously, in addition to allowing the formation of lines 124a that are narrower than features defined by the photolithographic technique used to pattern the photodefinable layer 120, this etch can smooth the edges of the lines 124 thereby improving the uniformity of the lines 124. The resulting photoresist lines 124 and 124a thus constitute the placeholders or mandrels upon which a pattern of spacers 175 (Figure 9) will be formed. In other embodiments, the spaces between the spaces 122 can be narrowed by expanding the lines 124 to a desired size. For example, additional material can be deposited over the lines 124 or the lines 124 can be chemically reacted to form a material having a larger volume to increase their size.

The pattern of the (modified) photodefinable layer 120 is preferably transferred to a layer 140 of material that can withstand with the process conditions for spacer material deposition, discussed below. In addition to having higher heat resistance than photoresist, the material forming the temporary layer 140 is preferably selected such that it can be selectively removed relative to the spacer material and the underlying layer. As noted above, the layer 140 is preferably formed of amorphous carbon. Because the preferred chemistries for etching photoresist also typically etch significant amounts of amorphous carbon and because chemistries are available for etching amorphous carbon with excellent selectivity relative to a variety of materials, a hard mask layer 130 selected from such materials preferably separates the layers 120 and 140. Suitable materials for the hard mask layer 130 include, for example, DARCs, silicon oxides or nitrides, and silicon.

The pattern in the photodefinable layer 120 is preferably transferred to the hard mask layer 130, as shown in Figure 5. This transfer is preferably accomplished using an anisotropic

etch, such as an etch using a fluorocarbon plasma, although a wet (isotropic) etch may also be suitable if the hard mask layer 130 is thin. Preferred fluorocarbon plasma etch chemistries can include CF_4, CFH_3, CF_2H_2, CF_3H, etc.

The pattern is then transferred to the temporary layer 140, as shown in Figure 6, preferably using a SO_2-containing plasma, *e.g.*, a plasma containing SO_2, O_2 and Ar. Advantageously, the SO_2-containing plasma can etch carbon of the preferred temporary layer 140 at a rate greater than 20 times and, more preferably, greater than 40 times the rate that the hard mask layer 130 is etched. A suitable SO_2-containing plasma is described in U.S. Patent Application No. 10/931,772 to Abatchev *et al.*, filed August 31, 2004, entitled Critical Dimension Control. It will be appreciated that the SO_2-containing plasma simultaneously etches the temporary layer 140 and removes the photodefinable layer 120.

As shown in Figure 7, a layer 170 of spacer material is preferably next deposited over the hard mask layer 130 and the temporary layer 140. The spacer material is preferably deposited by chemical vapor deposition or atomic layer deposition. The spacer material can be any material capable of use as a mask to transfer a pattern to the underlying primary mask layer 160. The spacer material preferably: 1) can be deposited with good step coverage, 2) can be deposited at a low temperature compatible with the temporary layer 140 and 3) can be selectively etched relative to the temporary layer 140 and any layer underlying the temporary layer 140. Preferred materials include silicon nitrides and silicon oxides.

As shown in Figure 8, the spacer layer 170 is then subjected to an anisotropic etch to remove spacer material from horizontal surfaces 180 of the partially formed integrated circuit 100. Such an etch, also known as a spacer etch, can be performed using a fluorocarbon plasma, which can also advantageously etch the hard mask layer 130. Next, the amorphous carbon layer 140 can be selectively removed, using, *e.g.*, a SO_2-containing plasma. Figure 9 shows a pattern of spacers 175 left after the amorphous carbon etch. Thus, pitch multiplication in the array of the partially formed integrated circuit 100 has been accomplished and, in the illustrated embodiment, the pitch of the spacers is half that of the photoresist lines 124 (Figure 3) originally formed by photolithography. It will be appreciated that the spacers 175 generally follow the outline of the pattern or lines 124 originally formed in the photodefinable layer 120.

Next, in a second phase of a method according to the preferred embodiments, a second pattern is formed at the periphery 104. To form this second pattern, the spacers 175 are protected and another photodefinable layer 220 is formed, as shown in Figure 10, to allow for patterning of the second pattern at the periphery 104. The spacers 175 are protected by forming a protective layer 200 over the spacers 175. The protective layer 200 is preferably at least as tall as the spacers 175 and preferably about 100-500 nm thick and, more preferably, about 100-300 nm thick. A hard mask layer 210 is next preferably formed over the protective layer 200 to aid in

transferring a pattern from the photodefinable layer 220 to the protective layer 200. Preferably, the hard mask layer 210 is about 40-80 nm thick and, more preferably, about about 50-60 nm thick.

The protective layer 200 is preferably formed of a material that is readily removed selectively relative to the spacers 175. For example, the protective layer 200 can be formed of a photoresist, and may be the same or a different photoresist from that used to form the photodefinable layer 120 (Figures 2-5), which can be the same or a different material from than used to form the photodefinable layer 220 (Figure 10). More preferably, the protective layer 200 is formed of amorphous carbon, which can be etched with excellent selectivity relative to the spacers 175.

In other embodiments where the protective layer 200 is formed of a material that can be selectively etched relative to both the spacers 175 and the photodefinable layer 220, the hard mask layer 210 can be omitted. For example, the protective layer 200 can be formed of a bottom anti-reflective coating (BARC) and a photoresist can be formed directly above the BARC. The spacers 175 can be formed of a material which allows good etch selectivity to the BARC, including silicon nitrides or oxides.

While it can be patterned using any photolithographic technique, the photodefinable layer 220 is preferably patterned using the same photolithographic technique used to pattern the photodefinable layer 120. Thus, with reference to Figure 11, a pattern 230 is formed in the photodefinable layer 220. While the pattern 177 preferably has a pitch or resolution smaller than the minimum pitch or resolution of the photolithographic technique, the pattern 230 preferably has a pitch or resolution equal to or greater than the minimum pitch or resolution of the photolithographic technique. It will be appreciated that the pattern 230 at the periphery 104 can be used to form landing pads, transistors, local interconnects etc. It will also be appreciated that, while illustrated laterally separated from the pattern 177, the pattern 230 can also overlap the pattern 177. Thus, the use of different reference numerals (177 and 230) for these patterns indicates that they were originally formed in different steps.

The pattern 230 is then transferred to the same level as the pattern 177 of spacers 175. As shown in Figure 12, the hard mask layer 210 is selectively etched relative to the photodefinable layer 220, preferably using an anisotropic etch such as a fluorocarbon plasma etch. Alternatively, a wet (isotropic) etch may also be suitable for the hard mask layer 210 is appropriately thin. The pattern 230 is then transferred to the protective layer 200 by another anisotropic etch, such as an etch with a SO_2-containing plasma, as shown in Figure 13. Because the hardmask layer 210 overlying the spacers 175 has previously been removed, this etch also removes the protective layer 200 around the spacers 175, thereby leaving those spacers 175 exposed.

With reference to Figures 14 and 15, the patterns 177 and 230 are then transferred down to the primary mask layer 160, which preferably comprises a material having good etch selectivity to the substrate 110, and vice versa, to allow the patterns 177 and 230 to be simultaneously transferred to the substrate 110. Thus, the patterns 177 and 230 form a mixed pattern in the primary mask layer 160.

To transfer to the patterns 177 and 230, the hard mask layer 150 overlying the primary mask layer 160 is first etched (Figure 14). The hard mask layer 150 is preferably anisotropically etched, preferably using a fluorocarbon plasma. Alternatively, an isotropic etch may be used if the hard mask layer 150 is relatively thin.

The primary mask layer 160 is then anisotropically etched, preferably using a SO_2-containing plasma, which can simultaneously remove the photodefinable layer 200 (Figure 15). As noted above, the SO_2-containing plasma has excellent selectivity for the amorphous carbon of the primary mask layer 160 relative to the hard mask layer 150. Thus, a thick enough mask can be formed in the primary mask layer 160 to later effectively transfer the mask pattern to the substrate 110 using conventional etch chemistries and without wearing away the primary mask layer 160 before the pattern transfer is complete.

Having both been transferred to the primary mask layer 160, the patterns 177 and 230 can then be transferred to the subtrate 110 using the layer 160 as a mask, as illustrated in Figure 16. Given the disparate materials typically used for the primary mask layer 160 and the substrate 110 (*e.g.*, amorphous carbon and silicon or silicon compounds, respectively), the pattern transfer can be readily accomplished using conventional etches appropriate for the material or materials comprising the substrate 110. For example, a fluorocarbon etch comprising CF_4, CHF_3 and/or NF_3 containing plasma can be used to etch silicon nitride, a fluorocarbon etch comprising CF_4, CHF_3, CH_2F_2 and/or C_4F_8 containing plasma can be used to etch silicon oxide and a HBr, Cl_2, NF_3, SF_6 and/or CF_4 containing plasma etch can be used to etch silicon. In addition, the skilled artisan can readily determine suitable etch chemistries for other substrate materials, such as conductors, including aluminum, transition metals, and transition metal nitrides. For example, an aluminum substrate can be etched using a fluorocarbon etch.

It will be appreciated that where the substrate 110 comprises layers of different materials, a succession of different chemistries, preferably dry-etch chemistries, can be used to successively etch through these different layers. It will also be appreciated that, depending upon the chemistry or chemistries used, the spacers 175 and the hard mask layer 150 may be etched. Amorphous carbon of the primary mask layer 160, however, advantageously offers excellent resistance to conventional etch chemistries, especially those used for etching silicon-containing materials. Thus, the primary mask layer 160 can effectively be used as a mask for etching through a plurality of substrate layers, or for forming high aspect ratio trenches. In addition, the pitch

doubled pattern 177 and the pattern 230 formed by conventional lithography can simultaneously be transferred to the substrate 110, or each individual layer of the substrate 110, in a single etch step.

Figures 17A and 17B show the resultant structure. Figure 17A shows the array portion of the integrated circuit 100, while Figure 17B shows the periphery of the integrated circuit 100 (Figures 2-16). As noted above, the substrate 110 can be any layer of material or materials that the patterns 177 and 230 are etched into. The composition of the substrate 110 can depend upon, *e.g.*, the electrical device to be formed. Thus, in Figures 17A and 17B, the substrate 110 comprises a Si_3N_4 layer 110a, a polysilicon layer 110b, a SiO_2 layer 110c and a silicon layer 110d. Such an arrangement of layers can be advantageously used in the formation of, *e.g.*, transistors.

Note that the etched surfaces exhibit exceptionally low edge roughness. In addition, the trenches formed in the array show excellent uniformity, even at the low 100 nm pitch pictured. Advantageously, these results are achieved while also forming well-defined and smooth lines in the periphery, as illustrated in Figure 17B.

It will be appreciated that the formation of patterns according to the preferred embodiments offers numerous advantages. For example, because multiple patterns, with different size features, can be consolidated on a single final mask layer before being transferred to a substrate, overlapping patterns can easily be transferred to the substrate. Thus, pitch-doubled features and features formed by conventional photolithography can easily be formed connected to each other. Moreover, as evident in Figures 17A and 17B, exceptionally small features can be formed, while at the same time achieving exceptional and unexpectedly low line edge roughness. While not limited by theory, it is believed that such low line edge roughness is the result of the use of the layers 140 and 160. Forming the spacers 175 and performing multiple anisotropic etches to transfer the patterns 177 and 230 from the level of the temporary layer 140 to the primary mask layer 160 and then to the substrate 110 are believed to beneficially smooth the surfaces of the features forming the patterns 177 and 230. Moreover, the preferred amorphous carbon etch chemistries disclosed herein allow the use of thin hard mask layers, such as the layers 130 and 150, relative to the depth that underlying amorphous carbon layers, such as the layers 140 and 160, are etched. This advantageously reduces demands on the identity of layers (*e.g.*, photoresist layers) overlying the hard mask layers and also reduces demands on the chemistries used to etch the hard mask layers while at the same time ensuring that the primary mask layers form thick enough masks to withstand subsequent substrate etches.

It will also be appreciated that various modifications of the illustrated process flow are possible. For example, pitch multiplied patterns typically formed closed loops, since the patterns are formed by spacers that surround a mandrel. Consequently, where the pitch multiplied pattern

is used to form conductive lines, additional processing steps are preferably used to cut off the ends of these loops, so that each loop forms two individual, non-connected lines.

Also, while the composition of the various layers discussed herein is chosen based upon consideration of etch chemistries and process conditions, the various hardmask layers are preferably each formed of the same material, as are the primary mask layers. Advantageously, such an arrangement reduces processing complexity.

In addition, the pitch of the pattern 177 can be more than doubled. For example, the pattern 177 can be further pitch multiplied by forming spacers around the spacers 175, then removing the spacers 175, then forming spacers around the spacers that were formerly around the spacers the 175, and so on. An exemplary method for further pitch multiplication is discussed in U.S. Patent No. 5,328,810 to Lowrey *et al.* In addition, while the preferred embodiments can advantageously be applied to formed patterns having both pitch multiplied and conventionally photolithographically defined features, the patterns 177 and 230 can both be pitch multiplied or can have different degrees of pitch multiplication.

Moreover, more than two patterns 177 and 230 can be consolidated on the primary mask layer 160 if desired. In such cases, additional mask layers can be deposited between the layers 140 and 160. For example, the patterns 177 and 230 can be transferred to an additional mask layer overlying the hard mask layer 150 and then the sequence of steps illustrated in Figures 10-16 can be performed to protect the patterns 77 and 230, to form the new pattern in an overlying photodefinable layer and to transfer the patterns to the substrate 110. The additional mask layer preferably comprises a material that can be selectively etched relative to the hard mask layer 150 and a protective layer that surrounds the patterns 177 and 230 after being transferred to the additional mask layer.

Also, while "processing" through the various mask layers preferably involve etching an underlying layer, processing through the mask layers can involve subjecting layers underlying the mask layers to any semiconductor fabrication process. For example, processing can involve ion implantation, diffusion doping, depositing, or wet etching, etc. through the mask layers and onto underlying layers. In addition, the mask layers can be used as a stop or barrier for chemical mechanical polishing (CMP) or CMP can be performed on the mask layers to allow for both planarizing of the mask layers and etching of the underlying layers,

Accordingly, it will be appreciated by those skilled in the art that various other omissions, additions and modifications may be made to the methods and structures described above without departing from the scope of the invention. All such modifications and changes are intended to fall within the scope of the invention, as defined by the appended claims.

WE CLAIM:

1. A method for semiconductor processing, comprising:

providing a substrate, wherein a primary mask layer overlies the substrate, wherein a temporary layer overlies the primary mask layer, wherein a first photoresist layer overlies the temporary layer;

forming a photoresist pattern in the first photoresist layer;

forming a first pattern in the temporary layer, wherein features of the first pattern are derived from features of the photoresist pattern;

forming a second photoresist layer above a level of the first pattern;

forming an other photoresist pattern in the second photoresist layer;

transferring the other photoresist pattern and the first pattern to the primary mask layer to form a mixed pattern in the primary mask layer; and

processing the substrate through the mixed pattern in the primary mask layer.

2. The method of Claim 1, wherein processing the substrate comprises transferring the mixed pattern to the substrate by etching the substrate.

3. The method of Claim 1, wherein forming a photoresist pattern and/or forming an other photoresist pattern comprise performing electron beam lithography.

4. The method of Claim 1, wherein forming a photoresist pattern and forming an other photoresist pattern comprise performing photolithography with light having a wavelength chosen from the group consisting of 13.7 nm, 157 nm, 193 nm, 248 nm or 365 nm wavelength light.

5. The method of Claim 4, wherein the first and the second photoresist layer comprise the same photoresist material.

6. The method of Claim 4, wherein forming the first pattern further comprises reducing a width of the photoresist, remaining after performing photolithography, to a desired width by isotropically etching the photoresist.

7. The method of Claim 6, wherein the first pattern follows an outline of lines of photoresist remaining after isotropically etching, wherein forming the first pattern comprises:

etching the temporary layer through the photoresist layer;

forming spacers on sidewalls of remains of the temporary layer after etching the temporary layer; and

preferentially removing temporary layer material relative to the spacers, wherein the spacers form the first pattern.

8. The method of Claim 1, wherein the temporary layer comprises amorphous carbon.

9. The method of Claim 8, wherein the primary mask layer comprises amorphous carbon.

10. The method of Claim 9, wherein hard mask layers directly overlie the temporary layer and the primary mask layer.

11. The method of Claim 10, wherein the hard mask layers comprise a material selected from the group consisting of silicon, silicon dioxide or an antireflective coating material.

12. The method of Claim 11, wherein the antireflective coating material is a dielectric antireflective coating.

13. The method of Claim 1, wherein the temporary layer comprises a bottom anti-flective coating.

14. The method of Claim 13, wherein the second photoresist layer directly contacts and overlies the bottom anti-flective coating.

15. The method of Claim 1, wherein the substrate is an insulator.

16. The method of Claim 15, wherein processing the substrate defines conductive lines of an array of a memory device.

17. A method for forming an integrated circuit:

providing a substrate;

forming an amorphous carbon layer over the substrate;

forming a first hardmask layer over the first amorphous carbon layer;

forming a temporary layer over the first hardmask layer; and

forming a second hardmask layer over the temporary layer.

18. The method of Claim 17, wherein forming an amorphous carbon layer comprises chemical vapor deposition.

19. The method of Claim 17, wherein the temporary layer comprises amorphous carbon.

20. The method of Claim 19, wherein forming a second amorphous carbon layer comprises chemical vapor deposition.

21. The method of Claim 17, wherein forming a first hardmask layer and forming a second hardmask layer comprise chemical vapor deposition.

22. The method of Claim 17, wherein the first hardmask layer comprises a material chosen from the group comprising silicon oxide, silicon or a dielectric anti-reflective coating.

23. The method of Claim 22, wherein the second hardmask layer comprises a material chosen from the group comprising silicon oxide, silicon or a dielectric anti-reflective coating.

24. The method of Claim 17, wherein the amorphous carbon layer is about 100 - 1000 nm thick.

25. The method of Claim 17, wherein the first hardmask layer is about 10 - 50 nm thick.

26. The method of Claim 17, wherein the temporary carbon layer is about 100 - 300 nm thick.

27. The method of Claim 17, wherein the second hardmask layer is about 10-- 50 nm thick.

28. The method of Claim 17, further comprising depositing and forming a pattern in a resist layer over the second hardmask layer by nano-imprinting.

29. The method of Claim 17, further comprising depositing a photoresist layer over the second hardmask layer.

30. The method of Claim 29, further comprising patterning the photoresist layer to form a photoresist pattern.

31. The method of Claim 30, further comprising altering a size of openings in the photoresist pattern.

32. The method of Claim 31, wherein altering the size of the openings comprises narrowing the size of the openings.

33. The method of Claim 31, wherein altering the size of openings comprises isotropically etching the photoresist pattern to form a widened photoresist pattern.

34. The method of Claim 33, further comprising transferring the widened photoresist pattern to the second hardmask layer.

35. The method of Claim 34, further comprising transferring the widened photoresist pattern to the temporary layer.

36. The method of Claim 35, further comprising forming spacers on sidewalls of the temporary layer formed by transferring the widened photoresist pattern.

37. The method of Claim 36, further comprising preferentially removing the temporary layer relative to the spacers to form a spacer pattern.

38. The method of Claim 37, further comprising transferring the spacer pattern to the first hardmask layer.

39. The method of Claim 38, further comprising transferring the spacer pattern to the amorphous carbon layer.

40. The method of Claim 39, further comprising transferring the spacer pattern to the substrate.

41. The method of Claim 17, wherein the substrate comprises a plurality of layers of different materials.

42. The method of Claim 41, wherein the plurality of layers comprises semiconductors, insulators and/or conductors.

43. A method for semiconductor fabrication, comprising:

forming a first pattern by pitch multiplication;

separately forming a second pattern by photolithography without pitch multiplication;

transferring the first and second patterns to a mask layer; and

etching a substrate through the mask layer.

44. The method of Claim 43, wherein forming the first pattern comprises:

forming a plurality of mandrels composed of amorphous carbon;

depositing a blanket layer of a silicon-containing material over the mandrels; and

anisotropically etching the blanket layer.

45. The method of Claim 43, wherein forming a first pattern is accomplished by pitch doubling.

46. The method of Claim 43, wherein separately forming a second pattern comprises overlapping the second pattern with the first pattern.

47. The method of Claim 43, wherein the substrate comprises a plurality of layers of different materials.

48. The method of Claim 47, wherein etching a substrate comprises employing a different etch chemistry for each of the plurality of layers.

49. A method for forming an integrated circuit, comprising:

forming a mask pattern, wherein a first part of the mask pattern has a first pitch and wherein a second part of the mask pattern has a second pitch, wherein the first pitch is below a minimum pitch of a photolithographic technique for defining the second pattern; and

etching a substrate through the mask pattern.

50. The method of Claim 49, wherein forming a mask pattern comprises patterning an area corresponding to the second part and separately patterning an area corresponding to the first part.

51. The method of Claim 50, wherein patterning an area corresponding to the second part is performed using a photolithographic technique utilizing 248 nm light.

52. The method of Claim 50, wherein forming a mask pattern comprises etching an amorphous carbon layer.

53. The method of Claim 50, wherein etching an amorphous carbon layer comprises exposing the amorphous carbon layer to SO_2-containing plasma.

54. The method of Claim 50, wherein the substrate comprises insulating and conducting layers.

55. A method for forming a memory device, comprising:

forming a pattern of temporary placeholders in a layer over a carbon layer;

depositing a layer of mask material over surfaces of the temporary placeholders;

selectively removing the mask material from horizontal surfaces; and

selectively removing the temporary placeholders relative to the mask material to form a pattern of mask material corresponding to features in an array region of the memory device.

56. The method of Claim 55, wherein depositing a layer of mask material comprises depositing the mask material by a low temperature chemical vapor deposition process.

57. The method of Claim 56, wherein the mask material comprises silicon nitride or silicon oxide.

58. The method of Claim 57, wherein selectively removing the mask material comprises etching with a fluorocarbon plasma.

59. The method of Claim 55, wherein the temporary placeholders comprise amorphous carbon.

60. The method of Claim 59, wherein selectively removing the temporary placeholders comprises etching with a sulfur dioxide-containing plasma.

61. The method of Claim 55, wherein a hardmask layer separates the temporary placeholders and the carbon layer.

62. The method of Claim 55, further comprising transferring the pattern of mask material to the carbon layer.

63. The method of Claim 62, wherein transferring the pattern of mask material to the carbon layer comprises exposing the hard mask layer to a fluorocarbon plasma.

64. The method of Claim 63, wherein transferring the pattern of mask material to the carbon layer comprises subsequently exposing the second carbon layer to a plasma containing sulfur dioxide.

65. The method of Claim 55, wherein a location of mask material of the pattern of mask material corresponds to a location of conductive lines in the array.

66. A method for manufacturing an integrated circuit, comprising:

forming a plurality of mandrel strips;

forming a spacer on sidewalls of each mandrel strip;

removing the mandrel strips to form a pattern of spaced apart spacers;

forming a mask layer in a plane above the spacers;

forming a pattern in the mask layer; and

transferring the pattern to the same horizontal plane as the spacers.

67. The method of Claim 66, wherein the spacers extend in spaced, generally parallel relation to one another at least between first and second spaced planes extending perpendicular to the spacers.

68. The method of Claim 66, further comprising transferring the pattern and an other pattern formed by the spacers to an other masking layer underlying the horizontal plane.

69. The method of Claim 66, wherein the mandrel strips have substantially vertical sidewalls.

70. The method of Claim 69, wherein forming a spacer comprises depositing a spacer material on exposed surfaces of the mandrel strips and subsequently selectively removing the spacer material from surfaces other than the sidewalls of the mandrel strips.

71. The method of Claim 70, wherein depositing a spacer material comprises performing a chemical vapor deposition or an atomic layer deposition process.

72. The method of Claim 70, wherein the spacer material comprises silicon nitride or silicon oxide.

73. The method of Claim 66, wherein forming a mask layer comprises:

surrounding the spacers with a layer of a removable material, wherein the removable material is selectively etchable relative to the spacers;

forming a hard mask layer directly above the layer of the removable material; and

forming a photoresist layer in the plane above the spacers.

74. The method of Claim 73, wherein forming a pattern in the mask layer comprises performing photolithography.

75. The method of Claim 66, wherein transferring the pattern to the same horizontal plane as the spacers comprises anisotropically etching amorphous carbon.

76. A method for manufacturing an integrated circuit, comprising:

providing a plurality of spaced-apart lines of a mask material above a substrate, wherein the mask material is different from photoresist;

patterning a plurality of features in a photodefinable material above the substrate by a photolithographic technique; and

replicating the spaced-apart lines and the plurality of features in an amorphous carbon layer below the spaced-apart lines.

77. The method of Claim 76, wherein the lines extend in spaced, generally parallel relation to one another at least between first and second spaced planes extending perpendicular to the lines.

78. The method of Claim 76, wherein a pitch of the lines is less than a minimum pitch of the photolithographic technique used for patterning a plurality of features.

79. The method of Claim 78, wherein patterning a plurality of features comprises exposing photoresist to light having a wavelength of 248 nm.

80. The method of Claim 76, wherein the lines are substantially in an array region of a memory circuit and wherein the plurality of features is substantially in a periphery of the memory circuit.

81. The method of Claim 76, wherein the lines are encased by a material selectively removable relative to the mask lines and wherein the photodefinable material is above the plurality of mask lines and the removable material.

82. The method of Claim 76, further comprising replicating the opening in the removable material by anisotropically etching the removable material.

83. The method of Claim 76, wherein the lines comprise silicon nitride or silicon oxide.

84. A method for forming a mask pattern to fabricate an integrated circuit, comprising:

providing a plurality of lines of a first mask material, the lines separated by a first temporary material;

selectively etching the first temporary material;

filling spaces between the lines with a second temporary material;

selectively etching the second temporary material to open the spaces; and

selectively etching through the spaces to form a pattern in a layer of another mask material.

85. The method of Claim 84, wherein selectively etching the first temporary material comprises etching amorphous carbon.

86. The method of Claim 85, wherein etching amorphous carbon comprises exposing the first material to a plasma containing sulfur dioxide.

87. The method of Claim 85, wherein filling a space between the lines comprises depositing amorphous carbon.

88. The method of Claim 85, wherein filling a space between the lines comprises depositing an underlayer photoresist.

89. The method of Claim 88, wherein the underlayer resist is a krypton fluoride photoresist.

90. The method of Claim 85, wherein selectively etching the second material comprises performing an etch using a sulfur dioxide-containing plasma.

91. The method of Claim 85, wherein selectively etching through the space comprises performing a hard mask etch and then etching an amorphous carbon layer using a sulfur dioxide-containing plasma.

92. The method of Claim 91, further comprising etching through the space to form openings in a substrate underneath the amorphous carbon layer.

93. The method of Claim 92, wherein etching through the space to form openings in a substrate comprises forming the openings in an insulating layer.

94. A process for fabricating an integrated circuit, comprising:

providing a masking layer extending over a first and a second region of a partially fabricated integrated circuit;

forming a pattern in the masking layer, wherein a minimum feature size of a portion of the pattern corresponding to the first region is equal to or less than about half a minimum feature size of an other portion of the pattern corresponding to the second region.

95. The process of Claim 94, wherein the masking layer comprises amorphous carbon.

96. The process of Claim 94, wherein the integrated circuit is a memory device, wherein the first region corresponds to the array of the memory device and wherein the second region corresponds to the periphery of the memory device.

97. The process of Claim 94, wherein forming a pattern in the masking layer comprises performing pitch multiplication for parts of the pattern over the first region and performing photolithography without pitch multiplication for parts of the pattern over the second region.

98. A partially formed integrated circuit, comprising:

a carbon layer; and

a plurality of pitch-multiplied spacers on a level overlying the carbon layer, wherein the spacers have a pitch of about 100 nm or less.

99. The partially formed integrated circuit of Claim 98, wherein the spacers extend in spaced, generally parallel relation to one another at least between first and second spaced planes extending perpendicular to the strips.

100. The partially formed integrated circuit of Claim 98, wherein the carbon layer comprises amorphous carbon.

101. The partially formed integrated circuit of Claim 98, wherein each of the plurality of spacers comprises silicon nitride or silicon oxide.

102. The partially formed integrated circuit of Claim 98, wherein the amorphous carbon layer is between about 100-1000 nm thick.

103. The partially formed integrated circuit of Claim 98, wherein a hard mask layer separates the amorphous carbon layer and the plurality of spacers.

104. The partially formed integrated circuit of Claim 103, wherein the hard mask layer is between about 10-50 nm thick.

105. The partially formed integrated circuit of Claim 103, wherein the spacers are located substantially at an array region of the partially formed integrated circuit.

106. The partially formed memory device of Claim 105, further comprising a pattern defined by carbon material overlying the hard mask layer.

107. The partially formed memory device of Claim 106, wherein the pattern defined by carbon material is located substantially at a periphery of the partially formed integrated circuit.

108. A partially formed integrated circuit, comprising:

a substrate;

a primary mask layer overlying the substrate, the primary mask layer formed of a material different from photoresist;

a mask material defining a first pattern in a first plane overlying the primary mask layer; and

a photodefinable material defining a second pattern in a second plane overlying the mask material.

109. The partially formed integrated circuit of Claim 108, wherein the mask material is surrounded by a material selectively removable relative to the mask material.

110. The partially formed integrated circuit of Claim 109, wherein the selectively removable material comprises an underlayer resist.

111. The partially formed integrated circuit of Claim 110, wherein the underlayer resist comprises a krypton fluoride photoresist.

112. The partially formed integrated circuit of Claim 109, wherein the selectively removable material comprises amorphous carbon.

113. The partially formed integrated circuit of Claim 108, wherein the primary mask layer is an amorphous carbon layer.

114. The partially formed integrated circuit of Claim 113, wherein a hard mask layer separates the amorphous carbon layer and the mask material.

115. The partially formed integrated circuit of Claim 113, wherein the mask material comprises a silicon-containing material.

116. The partially formed integrated circuit of Claim 115, wherein the mask material is silicon nitride or silicon oxide.

117. The partially formed integrated circuit of Claim 115, wherein the photodefinable material is a photoresist.

118. The partially formed integrated circuit of Claim 117, wherein the photoresist is a photoresist compatible with krypton fluoride, argon fluoride or 157 nm wavelength photoligthography systems or 193 nm wavelength immersion systems.

119. The partially formed integrated circuit of Claim 108, wherein a substrate underlies the primary mask layer.

120. The partially formed integrated circuit of Claim 108, wherein the substrate is conductive.

121. The partially formed integrated circuit of Claim 108, wherein the substrate comprises a plurality of layers of different materials.