

SYSTEMS AND METHODS FOR FORMING ADDITIONAL METAL ROUTING IN SEMICONDUCTOR DEVICES

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] This invention relates to a method of fabrication of semiconductor devices, and more particularly, to a method of providing extra metal routing in a gate portion of semiconductor devices.

Description of the Related Art

[0002] Combining both embedded DRAM memory and other components, such as high speed logic circuits, onto a single chip is often useful. In many embodiments, the DRAM memory components are fabricated in a central array portion of a semiconductor device while the logic circuits are fabricated in periphery portions of the semiconductor device. In some embodiments, faster speed is achieved, and bandwidth and capacitance problems are reduced when incorporating both memory and logic components on a single memory device, or chip.

[0003] In a typical memory device having both memory (array components) and logic (periphery components), the memory device often includes one or more local interconnects formed above the memory or logic components. The local interconnect may include metal routing between components of the memory device, either in the array or the periphery. Above the local interconnects, additional layers containing additional circuitry, such as logic components, memory contacts, or metal routing, may be formed. In some embodiments, a metal layer above the local interconnects comprises many of the metal routings used by the memory device.

[0004] As the density of components on a single memory device increases, the metal routing in the metal layer of the memory device also becomes increasingly dense and difficult to fabricate. Accordingly, there is an increasing need for systems and methods of incorporating additional routing in a memory device without increasing the size of the memory device.

SUMMARY OF THE INVENTION

[0005] In one embodiment, a method of forming additional metal routing in a semiconductor device comprising a memory array and a peripheral array comprises the steps of forming a plurality of transistors in at least one of the memory array and the peripheral array, wherein nitride caps are formed above each of the transistors, etching a portion of selected nitride caps, and depositing a metal film in the etched-away portions of the selected nitride caps in order to form additional metal routing.

[0006] In another embodiment, a semiconductor device comprises one or more gate structures each having a nitride cap, a metallization layer comprising metal routing, additional metal routing embedded in a selected group of the nitride caps, wherein the selected group of nitride caps are each partially etched in order to form a cavity in which a metal is deposited in order to form the extra metal routing, and one or more contacts between the metal routing in the metallization layer and the additional metal routing embedded in the nitride caps.

[0007] In another embodiment, a semiconductor device comprises a semiconductor substrate having an upper surface, a plurality of electronic devices formed on the semiconductor substrate, the plurality of electronic devices including at least a plurality of transistors, wherein the plurality of transistors includes a gate stack extending above the upper surface of the substrate, a gate conductor that interconnects the gates stacks of the plurality of transistors, wherein the gate conductor is surrounded by a protective isolation structure, a global insulative layer overlying the substrate, the plurality of electronic devices, and the gate conductor, at least one conductor layer having a plurality of conductive elements formed therein to interconnect selected ones of the plurality of electronic devices, wherein the conductive layer is formed in the global insulative layer so as to be positioned above the plurality of electronic devices, and a plurality of supplemental conductive elements formed in the protective isolation structure of the gate conductors, wherein the plurality of supplemental conductive elements are selectively coupled to the plurality of conductive elements in order to provide additional interconnection between the plurality of electronic devices without increasing a density of the conductive elements in the at least one conductor layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figure 1 is a cross-sectional view of a semiconductor device having an array portion and a periphery portion.

[0009] Figure 2 is a cross-sectional view of the periphery portion of the semiconductor device illustrated in Figure 1.

[0010] Figure 3 is a cross-sectional view of the periphery portion of the semiconductor device illustrated in Figure 2 at a subsequent processing stage.

[0011] Figure 4 is a cross-sectional view of the periphery portion of the semiconductor device illustrated in Figure 3 at a subsequent processing stage.

[0012] Figure 5 is a cross-sectional view of the periphery portion of the semiconductor device illustrated in Figure 4 at a subsequent processing stage.

[0013] Figure 6 is a cross-sectional view of the periphery portion of the semiconductor device illustrated in Figure 5 at a subsequent processing stage.

[0014] Figure 7 is a cross-sectional side view of the periphery portion of the semiconductor device taken across section A-A of Figures 6.

[0015] Figure 8 is a cross-sectional side view of an exemplary periphery portion of a semiconductor device having additional metal runners recessed in nitride caps of transistors.

[0016] Figure 9 is a cross-sectional side view of another exemplary periphery portion of a semiconductor device having additional metal runners recessed in nitride caps of transistors.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0017] Embodiments of the invention will now be described with reference to the accompanying Figures, wherein like numerals refer to like elements throughout. The terminology used in the description presented herein is not intended to be interpreted in any limited or restrictive manner, simply because it is being utilized in conjunction with a detailed description of certain specific embodiments of the invention. Furthermore, embodiments of the invention may include several novel features, no single one of which is solely responsible for its desirable attributes or which is essential to practicing the inventions herein described.

[0018] As discussed above, semiconductor memory devices, such as DRAM memory devices, for example, may include one or more metal layers above a local interconnect of the DRAM memory that make contact to lower gate regions of the memory device through vias in one or more insulating layers. However, due to the reduction in size of semiconductor components and increased circuit density, the density of the metal routing in these upper metal layers is becoming increasingly difficult to fabricate. As described in further detail below, by providing extra metal layers in lower memory regions, such as transistor gate regions, that may be coupled to the upper metal layers, the spacing requirements of the metal routing in the upper metal layers may be eased, while maintaining the size of the semiconductor device. In addition, the extra metal routing formed in the gate regions of the memory devices may be disposed parallel to other metal contacts and coupled to either end of the other metal contacts, such as buried digit lines, in order to reduce a resistance of the other metal contacts.

[0019] Figure 1 is a cross-sectional view of a semiconductor device 100 having an array portion 120 and a periphery portion 110. In one embodiment, the array portion 120 comprises a plurality of transistors 122A, such as DRAM transistors, and the periphery portion 110 comprises a plurality of transistors 122P, such as DRAM or SRAM transistors, for example. In the embodiment of Figure 1, the semiconductor device 100 comprises a silicon substrate 102 having isolation areas 103, such as shallow trench isolation (STI) regions.

[0020] In one embodiment, each of the transistors 122A, 122P comprises a number of layers that are fabricated in any of a number of well known manners. In the exemplary transistors 122A, 122P, a gate oxide layer 123 comprising silicon dioxide, for example, is formed on the substrate 102. A layer 124 may be formed on the gate oxide layer 123. In one embodiment, the layer 124 comprises a doped polysilicon, which provides a wordline for the array transistors 122A. In exemplary Figure 1, a layer 125 is formed on the layer 124. In one embodiment, the layer 125 comprises a Tungsten, Tungsten Nitride, or Tungsten Silicide. In the embodiment of Figure 1, a cap 126 is formed on the layer 125. In one embodiment, the cap 126 comprises a nitride material, such as Silicon Nitride. In the embodiment of Figure 1, the transistors 122A, 122P are surrounded on their lateral sides by a

silicon nitride spacer 127. The exemplary transistors 122A, 122P are overlaid with an insulative layer 128. In one embodiment, the insulative layer 128 comprises borophosphosilicate (BPSG), phosphosilicate glass (PSG), or silicon dioxide.

[0021] As illustrated in Figure 1, the insulative layer 128 covers the previously exposed sides and top surfaces of the transistors 122. As described further below, in an advantageous embodiment, portions of the insulative layer 128 are removed, followed by etching away of portions of selected nitride caps 126, and finally depositing a metal in the etched-away portions in the nitride caps 126 in order to form extra metal routing. In certain embodiments, the extra metal routing formed above the nitride caps 126 may be parallel to digit lines of a memory device.

[0022] Figure 2 is a cross-sectional view of the periphery portion 110 of the semiconductor device 100 illustrated in Figure 1. As illustrated in Figure 2, a top surface of the insulative layer 128 has been removed so that top surfaces of the transistors 122P are exposed. In one embodiment, a post chemical-mechanical polishing (PCMP) process is performed in order to remove an upper portion of the insulative layer 128.

[0023] Figure 3 is a cross-sectional view of the periphery portion 110 of the semiconductor device 100 illustrated in Figure 2 at a subsequent processing stage. In the illustration of Figure 3, a photoresist material 310 has been placed over one of the transistors 122P. In order to form the extra metal routing only in the areas desired, a photoresist material 310 may be placed over the portions of the semiconductor device 100, such as selected transistors 122P, that are not to be further etched.

[0024] Figure 4 is a cross-sectional view of the periphery portion 110 of the semiconductor device 100 illustrated in Figure 3 at a subsequent processing stage. As illustrated in Figure 4, a top portion of the nitride cap 126A has been removed, such as by a selective etching process. In one embodiment the nitride cap 126A is in the range of about 1,000-1,500 Angstroms thick. In another embodiment, the nitride cap 126A is about 1,500 Angstroms thick. In one embodiment, a nitride etch selective to oxide is performed on the periphery 110 in order to remove a portion of the nitride cap 126A. In one embodiment, about 100-1000 Angstroms of the nitride cap 126A is etched back. In one embodiment, about 500 Angstroms of the nitride cap 126A is etched back.

[0025] Figure 5 is a cross-sectional view of the periphery portion 110 of the semiconductor device 100 illustrated in Figure 4 at a subsequent processing stage. As illustrated in Figure 5, the photoresist 310 has been removed, using any suitable process that is known in the art, and a metal film 510 has been deposited on the exposed surfaces of the periphery 110. In one embodiment, the metal film 510 comprises Tungsten. In other embodiments, the metal film 510 may include other suitable conductive materials.

[0026] Figure 6 is a cross-sectional view of the periphery portion 110 of the semiconductor device 100 illustrated in Figure 5 at a subsequent processing stage. As illustrated in Figure 6, the metal layer 510 has been partially removed, such as by etching or CMP, leaving only a metal runner 610 (also referred to herein as “additional metal routing 610”) that was formed by the deposition of the metal film in the etched-away portion of the nitride cap 126A. The metal runner 610 may now be used to provide additional metal routing for the semiconductor device. For example, contacts between the additional metal routing and the underlying transistors may be formed in order to electrically couple desired portions of the transistors. Because such routing was previously performed by one or more upper metal layers, the additional metal routing 610 allows the spacing of the upper metal layers to be relaxed.

[0027] Figure 7 is a cross sectional side view of the periphery portion 110 of the semiconductor device 100 across section A-A of Figure 6. As shown in Figure 7, the metal runner 610 is selectively deposited, as described above with respect to take Figures 3-6. Thus, the metal runners 610 may be patterned to connect various portions of the semiconductor device 100.

[0028] Figure 8 is a cross-sectional side view of an exemplary periphery portion 800 of a semiconductor device having additional metal routing 810 recessed in nitride caps of transistors (transistor details are not illustrated in Figure 8). In the embodiment of Figure 8, a metallization layer 820 is selectively coupled to metal runners 810 via contacts 830. In prior art embodiments, routing is primarily performed at the metallization layer 820. However, in semiconductor devices having significant routing needs, the metallization layer 820 may become tightly pitched and thus, difficult to fabricate. With the addition of the additional metal routing 810, the metallization layer 820 is able to drop contacts 830 to the metal runner

810 in order to reduce the metal routing at the metallization layer 820. Thus, by patterning the additional metal routing 810 and the contacts 830 appropriately, the peripheral portion 800 may have an improved routing density by dropping a contact down to the metal runners 810, running the metal runner 810 to a desired location, and dropping another contact at the desired location to connect to the metal runner 810, thereby reducing the metal routing in the metallization layer 820.

[0029] Figure 9 is a cross-sectional side view of another exemplary periphery portion 900 of a semiconductor device having additional metal runners 810 recessed in nitride caps of transistors (transistor details are not illustrated in Figure 8). As those of skill in the art will recognize, high diffusion resistance in semiconductor devices is commonly reduced by placing metal across the diffusion wherever possible. This technique is known as strapping and is often accomplished by connecting a parallel metal path to the primary metal path. In Figure 9, the contact layer 830 straddles the metal runners 810 so that the additional metal routing 820 is positioned parallel to the layer 125, which may comprise a buried digit line, for example. In this embodiment, the metal runners 810 may be coupled to the layer 125 at two or more locations in order to reduce a resistance of the routing in layer 125.

[0030] Although described herein with respect to the periphery portion of a semiconductor device, extra metal routing may also be embedded into nitride caps of transistors in the array portion of semiconductor devices. Thus, additional metal routing may be implemented according to the systems and methods described herein in any portion of a semiconductor device.

[0031] The foregoing description details certain embodiments of the invention. It will be appreciated, however, that no matter how detailed the foregoing appears in text, the invention can be practiced in many ways. As is also stated above, it should be noted that the use of particular terminology when describing certain features or aspects of the invention should not be taken to imply that the terminology is being re-defined herein to be restricted to including any specific characteristics of the features or aspects of the invention with which that terminology is associated. The scope of the invention should therefore be construed in accordance with the appended claims and any equivalents thereof.

WHAT IS CLAIMED IS:

1. A method of forming runners in a semiconductor device comprising a memory array and a peripheral array of transistors, the method comprising:
 - forming a plurality of transistors in at least one of the memory array and the peripheral array, wherein isolation caps are formed above each of the transistors and wherein the plurality of transistors comprise at least one conductive layer;
 - forming an insulative layer so as to overlay the transistors;
 - removing a portion of the insulative layer so as to expose top surfaces of the isolation caps;
 - etching a portion of selected isolation caps such that the underlying conductive layer remains covered by remaining portions of the selected isolation caps; and
 - depositing a metal film in the etched-away portions of the selected isolation caps in order to form runners such that the runners are insulated from electrical contact with the at least one conductive layer by the remaining portions of the selected isolation caps.
2. The method of Claim 1, further comprising masking a portion of the periphery transistors that are not to be etched by the step of etching.
3. The method of Claim 1, further comprising forming a metal layer comprising metal routing on the periphery transistors, wherein portions of the metal routing electrically contact the runners.
4. The method of Claim 1, wherein the metal film comprises Tungsten.
5. The method of Claim 1, wherein the runners are parallel to a buried digit line of at least one of the periphery transistors.
6. The method of Claim 5, wherein the runners are electrically coupled to at least two portions of the buried digit line.

7. The method of Claim 1, wherein the isolation caps each have a thickness of about 150 nm.
8. The method of Claim 7, wherein the etching recesses the selected isolation caps by about 50 nm.
9. The method of Claim 7, wherein the etching recesses the selected isolation caps in the range of about 10 to 100nm.
10. The method of Claim 3, wherein the runners are electrically connected to two portions of the metal routing so as to form a jumper between the two portions.
11. The method of Claim 1, wherein the semiconductor device comprises a DRAM.
12. A semiconductor device comprising:
 - a semiconductor substrate having an upper surface;
 - a plurality of electronic devices formed on the semiconductor substrate, the plurality of electronic devices including at least a plurality of transistors, wherein the plurality of transistors includes a gate stack extending above the upper surface of the substrate;
 - a gate conductor that interconnects the gates stacks of the plurality of transistors, wherein the gate conductor is surrounded by a protective isolation structure, the protective isolation structure comprising spacers and a cap;
 - an insulative layer overlying the substrate, the plurality of electronic devices, and the gate conductor; and
 - a plurality of runners formed in the protective isolation structure of the gate conductors, wherein the plurality of runners are electrically isolated from the gate conductors by portions of the protective isolation structure.

13. The semiconductor device of Claim 12, wherein the runners comprise one or more metals.
14. The semiconductor device of Claim 12, wherein the protective isolation structure comprises a nitride material.
15. The semiconductor device of Claim 12, wherein the runners form jumpers between conductive elements in at least one conductive layer.
16. The semiconductor device of Claim 12, wherein at least a portion of the runners is parallel to a buried digit line of at least one of the plurality of transistors.
17. The semiconductor device of Claim 15, wherein the at least a portion of the runners is electrically coupled to at least two portions of the conductive elements.
18. The semiconductor device of Claim 12, wherein the protective isolation structure has a thickness of about 150nm.
19. The semiconductor device of Claim 18, wherein the protective isolation structure is recessed in the range of about 10 to 100nm and wherein the runners are formed in the recessed portions of the protective isolation structure.
20. The semiconductor device of Claim 12, wherein the semiconductor device comprises a DRAM.