METHODS OF FABRICATING INTERCONNECTS FOR SEMICONDUCTOR COMPONENTS

TECHNICAL FIELD

[0001] The invention pertains to methods of fabricating interconnects for semiconductor components.

BACKGROUND OF THE INVENTION

[0002] Semiconductor components, such as dice, wafers and chip scale packages, are fabricated to include external contacts to allow electrical connections to be made from the outside of the components to integrated circuits contained on the components. A semiconductor die, for example, typically includes patterns of bond pads formed on a face of the die. At the wafer level, the bond pads are used for probe testing the integrated circuits on the die. At the die level, the bond pads are used for testing, and also for making electrical connections, such as wire bonds, for packaging. Typically, the bond pads comprise planar aluminum pads, or alternatively solder bumps on solder wettable pads.

[0003] The interconnects described above are but one type of interconnect that can be utilized with semiconductor components. Numerous other types of interconnects are known. For instance, semiconductor packages, such as chip scale packages, can utilize solder balls arranged in a dense array, such as a ball grid array (BGA), or fine ball grid array (FBGA).

[0004] Figs. 1-5 illustrate an exemplary semiconductor component 10 having interconnects associated therewith. Fig. 1 is a top view of a fragment of the component 10, and shows a plurality of conductive traces 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, 34 and

36. The conductive traces extend from inner lead bond pads 38, 40, 42, 44, 46, 48, 50, 52, 54, 56, 58, 60 and 62 to outer lead bonds 64, 66, 68, 70, 72, 74, 76, 78, 80, 82, 84, 86 and 88. The shown relative sizes of the outer lead bonds and inner lead bonds are for diagrammatic purposes only. Accordingly, although the inner lead bonds are shown uniform in size and larger than the outer lead bonds which are also uniform in size, it is to be understood that the constructions can also have inner lead bonds and/or outer lead bonds which are not uniform in size, and can have inner lead bonds which are smaller than the outer lead bonds.

[0005] Figs. 2 and 3 show a top view and a cross-sectional side view of an expanded region of the Fig. 1 fragment. Such views show that the trace 18 is a layer 100 of conductive material. Outer lead bond 70 comprises a solder ball 102 over a nickel-containing solder-wettable material 104. Inner lead bond 44 comprises a solder interconnect 106 having a conductive material cap 108 thereover. Conductive material cap 108 can comprise, for example, nickel and/or a solder ball.

[0006] Trace 100 can be referred to as a redistribution layer, in that it distributes an electrical signal from the central location of the inner lead bond 44 to the laterally outward location of outer lead bond 70 and vice versa.

[0007] The semiconductor component of fragment 10 comprises a semiconductor die 110 which can correspond to, for example, a monocrystalline silicon wafer. The die 110 has various levels of integrated circuitry (not shown) associated therewith. An electrically insulative passivation layer 112 extends around die 110 and insulates the die from the solder material 106. Passivation layer 112 can comprise, consist essentially of, or consist of silicon dioxide, and will typically have a thickness of from about 2000Å to about 8000Å.

An insulative material 114 is provided over passivation layer 112, and is utilized to support circuit trace 100, and can also be utilized during patterning of circuit trace 100. Layer 114 can comprise, for example, polyimide.

[0008] Semiconductor die 110 can be considered a semiconductor substrate, or alternatively the die 110 in combination with various other materials of component 10 can be considered a semiconductor substrate. To aid in interpretation of the claims that follow, the terms "semiconductive substrate" and "semiconductor substrate" are defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

[0009] The die 110 has two opposing sides 111 and 113, which are typically referred to as a front side and a back side, respectively. Component 10 has opposing outer surfaces 115 and 117 that are proximate the front side 111 and the back side 113, respectively, of die 110. Surfaces 115 and 117 can be referred to as a front-side surface and back-side surface, respectively, of component 10.

[0010] Solder material 106 extends entirely through component 10, and accordingly extends from the front-side surface 115 of the component to the back-side surface 117 of the component. Solder material 106 can ultimately be utilized for an electrical connection to an external device proximate back-side surface 117, and can be utilized for electrically interconnecting such device to another device associated with pad 102 of outer lead 70.

[0011] A method of forming the structure of Figs. 2 and 3 is described with reference to Figs. 4 and 5. Specifically, the construction 10 is shown prior to formation of leads 44 and 70 (Figs. 2 and 3). A hole 130 is etched through component 10 to extend from front-side surface 115 to back-side surface 117. The hole can be formed by, for example, laser-etching. The hole comprises a depth 132 extending from the front-side surface 115 to the back-side surface 117, and comprises a width dimension 134 orthogonal to the depth. The hole can be substantially circular when viewed from above (as shown), and accordingly width dimension 134 can correspond to a diameter of the circle. Alternatively, the hole can have a polygonal shape (such as, for example, a square shape) when viewed from above. Regardless of the shape of the hole 130, the maximum width dimension will typically be less than or equal to about 100 microns, and frequently will be less than or equal to about 35 microns.

[0012] A problem is encountered in uniformly filling hole 130 with solder. Specifically, the small dimension of hole 130 makes it difficult to flow solder into the hole. Various efforts have been made to provide solder-wetting agents along the peripheral sidewalls of the hole 130 in order to draw the solder into the hole. However, the provision of the solder-wetting agents will frequently comprise relatively high-temperature processing (specifically, processing in excess of 300°C), which can adversely impact circuitry associated with die 110. Accordingly, it is desired to develop new methods for forming interconnects within semiconductor components.

SUMMARY OF THE INVENTION

[0013] In one aspect, the invention encompasses a method of fabricating an interconnect for a semiconductor component. A semiconductor substrate is provided, and an opening is formed which extends entirely through the substrate. A first material is deposited along sidewalls of the opening at a temperature of less than or equal to about 200°C. A second material is then plated within the opening and over the first material.

[0014] In one aspect, the invention encompasses a method of fabricating an interconnect for a semiconductor component. A semiconductor substrate is provided and an opening is formed to extend entirely through the substrate. A metal nitride is deposited along sidewalls of the opening. The deposition is conducted in a reaction chamber utilizing a first precursor containing the metal of the metal nitride, and a second precursor containing the nitrogen of the metal nitride. The deposition comprises at least one cycle in which the first and second precursors are in the reaction chamber at different and substantially non-overlapping time intervals relative to one another. A second material is subsequently plated within the opening and over the metal nitride.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

[0016] Fig. 1 is a diagrammatic top view of a prior art semiconductor component construction.

[0017] Fig. 2 is an enlarged view of the region 2 of the Fig. 1 prior art construction.

[0018] Fig. 3 is a view along the line 3-3 of the Fig. 2 prior art construction.

[0019] Fig. 4 is a view of a prior art construction at a processing stage prior to that of Fig. 2.

[0020] Fig. 5 is a cross-sectional view along the line 5-5 of the Fig. 4 prior art construction.

[0021] Fig. 6 is a diagrammatic, cross-sectional view of a semiconductor component at a preliminary processing stage of an exemplary method of the present invention.

[0022] Fig. 7 is a view of the Fig. 6 fragment shown at a processing stage subsequent to that of Fig. 6.

[0023] Fig. 8 is a view of the Fig. 6 fragment shown at a processing stage subsequent to that of Fig. 7.

[0024] Fig. 9 is a view of the Fig. 6 fragment shown at a processing stage subsequent to that of Fig. 8.

[0025] Fig. 10 is a view of the Fig. 6 fragment shown at a processing stage subsequent to that of Fig. 9.

[0026] Fig. 11 is a view of the Fig. 6 fragment shown at a processing stage subsequent to that of Fig. 10.

[0027] Fig. 12 is a view of the Fig. 6 fragment shown at a processing stage subsequent to that of Fig. 11.

[0028] Fig. 13 is a view of the Fig. 6 fragment shown at a processing stage subsequent to that of Fig. 12.

[0029] Fig. 14 is a view of the Fig. 6 fragment shown at a processing stage subsequent to that of Fig. 7 in accordance with a second aspect of the present invention.

[0030] Fig. 15 is a view of the Fig. 14 fragment subsequent to that of Fig. 14.

[0031] Fig. 16 is a view of the Fig. 14 fragment shown at a processing stage subsequent to that of Fig. 15.

[0032] Fig. 17 is a diagrammatic, cross-sectional view of an exemplary deposition apparatus which can be utilized in various aspects of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0033] In particular aspects, the invention encompasses methods for forming solder within openings extending through semiconductor components. Low temperature deposition is utilized to form a film within an opening. The film can comprise a metal nitride, such as, for example, titanium nitride. A surface of the film is plated with a solder-wetting material (such as, for example, nickel). The plating can comprise activation of the surface, (such as, for example, by dipping the film in a solution comprising hafnium and/or palladium), followed by electroless plating of the activated surface with the solder-wetting material. Alternatively, the plating can comprise utilization of activationless plating chemistry to form a plating on the surface. The activationless plating chemistry can utilize reduced stabilizer content and can utilize the TiN of the film to carry an electrical potential for the plating chemical reaction. As another example, a low temperature TiN film can be used as a low temperature base or adhesion layer for another low temperature chemical vapor deposited layer (such as, for example, tungsten). The solder-wetting material can then be plated onto the low temperature chemical vapor deposited layer.

[0034] After formation of the solder-wetting material over the film, solder can be drawn into the opening along the solder-wetting material to fill the opening.

[0035] The low-temperature deposition of the film is preferably conducted at a temperature of less than or equal to about 200°C so that a temperature of the semiconductor component does not exceed 200°C during the deposition. Suitable deposition technologies can comprise atomic layer deposition (ALD) and/or chemical vapor deposition (CVD). To assist the reader in understanding the invention, ALD technology and CVD technology will be initially described in some detail. Referring first to ALD technology, such typically involves formation of successive atomic layers on a substrate. Such layers may comprise, for example, an epitaxial, polycrystalline, and/or amorphous material. ALD may also be referred to as atomic layer epitaxy, atomic layer processing, etc.

[0036] Described in summary, ALD includes exposing an initial component to a first chemical species to accomplish chemisorption of the species onto the component. Theoretically, the chemisorption forms a monolayer that is uniformly one atom or molecule thick on the entire exposed initial component. In other words, a saturated monolayer. Practically, as further described below, chemisorption might not occur on all portions of the component. Nevertheless, such an imperfect monolayer is still a monolayer in the context of this document. In many applications, merely a substantially saturated monolayer may be suitable. A substantially saturated monolayer is one that will still yield a deposited layer exhibiting the quality and/or properties desired for such layer.

[0037] The first species is purged from over the component and a second chemical species is provided to chemisorb onto the first monolayer of the first species. The second species is then purged and the steps are repeated with exposure of the second species monolayer to the first species. In some cases, the two monolayers may be of the same species. Also, a third species or more may be successively chemisorbed and purged just

as described for the first and second species. It is noted that one or more of the first, second and third species can be mixed with inert gas to speed up pressure saturation within a reaction chamber.

[0038] Purging may involve a variety of techniques including, but not limited to, contacting the component and/or monolayer with a carrier gas and/or lowering pressure to below the deposition pressure to reduce the concentration of a species contacting the component and/or chemisorbed species. Examples of carrier gases include N_2, Ar, He, Ne, Kr, Xe, etc. Purging may instead include contacting the component and/or monolayer with any substance that allows chemisorption byproducts to desorb and reduces the concentration of a species preparatory to introducing another species. A suitable amount of purging can be determined experimentally as known to those skilled in the art. Purging time may be successively reduced to a purge time that yields an increase in film growth rate. The increase in film growth rate might be an indication of a change to a non-ALD process regime and may be used to establish a purge time limit.

[0039] ALD is often described as a self-limiting process, in that a finite number of sites exist on a component to which the first species may form chemical bonds. The second species might only bond to the first species and thus may also be self-limiting. Once all of the finite number of sites on a component are bonded with a first species, the first species will often not bond to other of the first species already bonded with the component. However, process conditions can be varied in ALD to promote such bonding and render ALD not self-limiting. Accordingly, ALD may also encompass a species forming other than one monolayer at a time by stacking of a species, forming a layer more than one atom or molecule thick. The various aspects of the present invention described herein are

applicable to any circumstance where ALD may be desired. It is further noted that local chemical reactions can occur during ALD (for instance, an incoming reactant molecule can displace a molecule from an existing surface rather than forming a monolayer over the surface). To the extent that such chemical reactions occur, they are generally confined within the uppermost monolayer of a surface.

[0040] Traditional ALD can occur within frequently-used ranges of temperature and pressure and according to established purging criteria to achieve the desired formation of an overall ALD layer one monolayer at a time. Even so, ALD conditions can vary greatly depending on the particular precursors, layer composition, deposition equipment, and other factors according to criteria known by those skilled in the art. Maintaining the traditional conditions of temperature, pressure, and purging minimizes unwanted reactions that may impact monolayer formation and quality of the resulting overall ALD layer. Accordingly, operating outside the traditional temperature and pressure ranges may risk formation of defective monolayers.

[0041] The general technology of chemical vapor deposition (CVD) includes a variety of more specific processes, including, but not limited to, plasma-enhanced CVD and others. CVD is commonly used to form non-selectively a complete, deposited material on a component. One characteristic of CVD is the simultaneous presence of multiple species in the deposition chamber that react to form the deposited material. Such condition is contrasted with the purging criteria for traditional ALD wherein a component is contacted with a single deposition species that chemisorbs to a component or previously deposited species. An ALD process regime may provide a simultaneously contacted plurality of species of a type or under conditions such that ALD chemisorption, rather than CVD

reaction occurs. Instead of reacting together, the species may chemisorb to a component or previously deposited species, providing a surface onto which subsequent species may next chemisorb to form a complete layer of desired material.

[0042] Under most CVD conditions, deposition occurs largely independent of the composition or surface properties of an underlying component. By contrast, chemisorption rate in ALD might be influenced by the composition, crystalline structure, and other properties of a component or chemisorbed species. Other process conditions, for example, pressure and temperature, may also influence chemisorption rate. Accordingly, observation indicates that chemisorption might not occur appreciably on portions of a component though it occurs at a suitable rate on other portions of the same component. Such a condition may introduce intolerable defects into a deposited material.

[0043] An exemplary method of the present invention is described with reference to Figs. 6-13. Referring initially to Fig. 6, such shows a fragment of a construction 200 at a preliminary processing stage. Construction 200 comprises several of the structures described previously with reference to Figs. 1-5, and such structures are labeled identically in construction 200 as they were labeled in Figs. 1-5. Accordingly, construction 200 is shown to comprise a semiconductor component 110 having a front side 111 and a back side 113, and further is shown to comprise a passivation layer 112 extending around component 110. Construction 200 further comprises a conductive metal trace 100 analogous to the trace described previously, and comprises a thick passivation layer 114 beneath trace 100. The thick passivation layer can be, for example, a polyimide-containing layer.

[0044] Construction 200 differs from the construction 10 of Figs. 1-5 in that construction 200 comprises a pair of insulative-material layers 202 and 204 over conductive-material layer 100. Insulative material layers 202 and 204 can be referred to as a first and second insulative-material layer, respectively. Insulative-material layer 202 can comprise, for example, polyimide, and insulative-material layer 204 can comprise, for example, silicon dioxide formed by low-temperature deposition. Insulative-material layer 202 is patterned to have a gap 206 extending therethrough, which is ultimately to be a location for an outer lead bond.

[0045] Construction 200 can be considered a semiconductor component, and such component comprises a front-side surface 208 outwardly of the front side of semiconductor die 110, and a back-side surface 210 outwardly of the back side 113 of die 110.

[0046] An opening 212 extends entirely through semiconductor component 200, and specifically extends from front-side surface 208 to back-side surface 210. Opening 212 comprises a depth 214 between the front-side surface 208 and the back-side surface 210, and comprises a width 216 orthogonal to the depth 214. Opening 212 can have any suitable shape when viewed from above, including, for example, a substantially circular shape. If opening 212 is substantially circular when viewed from above, then width 216 will correspond to a diameter of the circle. Regardless of the shape of opening 212, the opening will have a maximum cross-sectional width. In particular aspects, such maximum cross-sectional width will be less than about 100 microns, and in further aspects such maximum cross-sectional width will be less than about 35 microns.

[0047] Opening 212 has sidewall peripheries 218 which comprise a surface of passivation material 112 and a surface of insulative material 204. In particular aspects,

materials 204 and 112 can comprise the same composition as one another, and specifically can comprise, consist essentially of, or consist of silicon dioxide. Accordingly, sidewalls 218 can comprise, consist essentially of, or consist of silicon dioxide along the entirety of the sidewalls.

[0048] As discussed previously, structure 110 can comprise a semiconductor die, and in particular aspects will comprise a monocrystalline semiconductor material, such as, for example, a monocrystalline silicon wafer. Accordingly, opening 212 can be considered to extend through a monocrystalline silicon wafer in some aspects of the invention.

[0049] It is noted that an interface between materials 204 and 112 should be shown in the opening 212 of Fig. 6 as such interface would be visible behind the plane of the opening. However, such interface is not shown within the opening in order to simplify the drawings. Generally, interfaces occurring behind the illustrated planes of the cross-sectional views of this disclosure will not be shown, except in instances in which it is believed that the showing of such interfaces will enhance clarity in the drawings and/or description.

[0050] Structures 114, 100, 202 and 204 can be considered to be proximate the front side 111 of structure 110. Specifically, the structures 114, 100, 202 and 204 are closer to the front side 111 than to the back side 113.

[0051] The processing described previously with reference to Figs. 4 and 5 showed a hole 130 punched through conductive material 100, and accordingly the hole 130 comprised a periphery containing the conductive material 100. A difference between the Fig. 6 structure 200 and the structure described with reference to Figs. 4 and 5 is that hole 212 does not comprise a periphery extending entirely to conductive material 100.

Construction 200 can be formed by initially forming conductive-material layer 100 to be patterned such that the material 100 comprises a gap extending therethrough where hole 212 is ultimately to be formed. The gap can then be filled with the electrically-insulative material 204, and the opening 212 can be punched through electrically-insulative material 204.

[0052] Although construction 200 is shown with opening 212 not contacting conductive material 100, it is to be understood that the processing of Figs. 4 and 5 could be utilized instead of the shown processing. Accordingly the opening could be formed through a conductive pad of material as shown in Figs. 4 and 5, and could have a periphery comprising the conductive material of the pad.

[0053] Referring next to Fig. 7, a layer (which can also be referred to herein as a film) 220 is deposited within opening 212 along sidewalls 218, and also along back-side surface 210 of component 200. Layer 220 can comprise an electrically-conductive material, and in particular aspects will comprise, consist essentially of, or consist of metal nitride. For instance, layer 220 can comprise, consist essentially of, or consist of one or more of titanium nitride, tungsten nitride, tantalum nitride and hafnium nitride. Layer 220 can be referred to as a first material in particular aspects of the invention to distinguish layer 220 from subsequent materials formed within opening 212.

[0054] Although layer 220 is described as being formed over back-side surface 210, it is to be understood that layer 220 can be alternatively considered to define a new back-side surface so that the back-side surface 210 becomes associated with layer 220 rather than with material 112. However, as will become apparent from the discussion that follows, the portion of layer 220 associated with the back side of construction 200 is ultimately removed,

so it is simpler for the discussion herein if the back-side surface is considered to remain associated with material 112 even after formation of layer 220.

[0055] Layer 220 can be formed by, for example, ALD and/or CVD, and is preferably formed at a temperature of less than or equal to about 200°C. The utilization of temperatures at or below 200°C can avoid problems discussed above in the "Background" section of this disclosure, and specifically can avoid heating circuitry associated with die 110 (not shown) to temperatures which can adversely impact the circuitry.

[0056] Fig. 17 shows an exemplary deposition apparatus 1000 that can be utilized for forming layer 220. Apparatus 1000 comprises a reaction chamber 1002. An inlet 1004 extends into the reaction chamber, and a valve 1006 is provided across inlet 1004 for controlling flow of materials through the inlet. An outlet 1008 also extends into the reaction chamber, and a valve 1010 is provided to control flow of materials through the outlet.

[0057] A substrate holder 1012 is provided within the reaction chamber, and such is shown holding an exemplary substrate 1014. Substrate 1014 can correspond to, for example, the semiconductor component 200 of Figs. 6 and 7.

[0058] In operation, materials are flowed into chamber 1002 through inlet 1004, and expelled from chamber 1002 through outlet 1008. The materials flowed into the chamber are represented by arrow 1016, and the materials expelled from the chamber represented by arrow 1018. The materials flowed into chamber 1002 can be suitable reactants (i.e., one or more precursors), carrier gases, purge gases, etc.

[0059] If apparatus 1000 is utilized for an ALD-type process, two precursors can be introduced into the chamber at different and substantially non-overlapping time intervals relative to one another. Specifically, a first precursor can be introduced into the chamber to

form a first substantially-saturated monolayer over an exposed surface of substrate 1014, and subsequently the first precursor can be expelled from the reaction chamber. A second precursor can then be introduced into the reaction chamber to react with the monolayer formed from the first precursor to form a desired material from the monolayer. The utilization of the first and second precursors can be considered one cycle of the process, and multiple cycles can be utilized to form a desired material to a desired thickness. The first and second precursors are described as being within the chamber at "non-overlapping time intervals" relative to one another in that each of the precursors is substantially entirely flushed from within the reaction chamber prior to introduction of the other. The term "substantially" non-overlapping time interval is utilized to indicate that there may be some residual precursor within the chamber when a subsequent precursor is introduced into the chamber, but such residual precursor concentration will be very low, and typically low enough so that there is no detectable interaction of the precursors with one another except at the surface of substrate 1014.

[0060] In an exemplary aspect of the invention, layer 220 comprises metal nitride. In such aspect, a first precursor can comprise the metal of the metal nitride and a second precursor can comprise the nitrogen of the metal nitride. The layer 220 can be formed utilizing at least one cycle in which the first and second precursors are in the reaction chamber at different and substantially non-overlapping time intervals relative to one another. Typically, each cycle will comprise introduction of the first precursor, followed by a purge, and then followed by introduction of the second precursor. If the metal nitride is titanium nitride, exemplary precursors containing the metal of the titanium nitride are $TiCl_4$

and tetrakis-dimethyl-amido-titanium (TDMAT), and an exemplary precursor containing the nitrogen of the metal nitride is ammonia (NH_3).

[0061] A titanium nitride layer 220 can be formed at a temperature of from about 68°C to about 400°C if formed from titanium tetrachloride and ammonia, but preferably will be formed at a temperature of less than about 200°C.

[0062] In applications in which layer 220 is titanium nitride, the first precursor comprises TDMAT and the second precursor comprises ammonia, the formation of layer 220 can be accomplished utilizing multiple cycles at a temperature of from about 100°C to about 180°C, typically from about 130°C to about 170°C, with an exemplary temperature being 155°C; a pressure from about 200 milliTorr to about 2 Torr, with an exemplary pressure being about 800 milliTorr; a cold wall reaction chamber; a pulse of the TDMAT into the chamber for a time of about 1 second; a purge for a time of about 10 seconds; and a second pulse of the ammonia into the reaction chamber for at time of about 4 seconds. The pulse of the ammonia can be followed by a purge for about 10 seconds, to complete an individual cycle. The purge can be accomplished utilizing vacuum and/or a suitable purge gas. The purge gas can comprise, for example, argon, and is preferably a gas which is inert relative to reaction with the precursors and any exposed materials on the substrate.

[0063] The temperatures described above for formation of a metal nitride layer are exemplary temperatures. It can be preferred, however, that temperatures utilized for formation of the layer 220 be at or below about 200°C, and more preferred that the temperatures be at or below about 160°C.

[0064] Layer 220 can be formed to any desired thickness through multiple cycles of an ALD-type process. A typical thickness of layer 220 will be at least about 100Å, with

exemplary thicknesses being from about 100Å to about 3000Å. If the TDMAT/NH_3 processing is utilized, each of the above-described cycles will typically form a layer less than or equal to about 10Å thick (with typical layers being about 9Å thick), and accordingly it can be desired to repeat the cycles at least about 10 times to form layer 220 to a desired thickness.

[0065] The methods described above for the TDMAT/NH_3 processing and the $TiCl_4/NH_3$ processing are ALD-like, in that the methods utilize two precursors which are provided in a reaction chamber at substantially non-overlapping times relative to one another. It is to be understood, however, that the processing utilized to form layer 220 can be any suitable processing, including CVD-type processes.

[0066] It is noted that a TiN film formed from TDMAT will frequently oxidize upon exposure to air unless treated with a post-deposition anneal of about 400°C. As will become apparent below, the metal nitride film 220 of the present invention is utilized as a substrate for a plating procedure. In such applications, the conductive properties of the film are not generally of concern, and accordingly, the film can oxidize to some extent. Thus, the post-deposition anneal typically utilized with TDMAT formation of TiN can be omitted, and the film 220 can be formed with a process which remains at or below 200°C (typically at or below 160°C, and frequently at or below 155°C) for the entirety of the process.

[0067] Referring to Fig. 8, layer 220 is shown removed from over back-side surface 210 of component 200. Such removal can be accomplished utilizing any suitable etch, and/or utilizing planarization methods (such as, for example, chemical-mechanical polishing).

[0068] Fig. 8 also shows a layer 222 formed over an exposed surface of layer 220. Layer 222 represents activation of layer 220. The activation of layer 220 is accomplished

by exposing layer 220 to one or both of hafnium and palladium. An exemplary method of activating a surface of layer 220 is to expose the layer to a solution comprising about 0.15 grams per liter of palladium chloride, and about 4 milliliters per liter hydrofluoric acid, with the remainder being deionized water. The exposure can be accomplished with a dip into the solution for a time of from about 30 seconds to about 60 seconds, with about 30 seconds typically being adequate at room temperature. The activation can form a separate layer 222 as shown, or can instead alter a surface composition of layer 220. Regardless, the activation prepares layer 220 for subsequent electroless deposition over the layer. In particular aspects, the activation forms the shown separate layer 222 comprising, consisting essentially of, or consisting of one or both of hafnium and palladium. Layer 222 can have a thickness of from about 1 micron to about 7 microns, with an exemplary suitable thickness being about 5 microns.

[0069] The activation of the surface of layer 220 can be performed before or after removal of layer 220 from over back-side surface 210. If layer 220 comprises hafnium or palladium, the activation of the layer can be omitted.

[0070] Referring next to Fig. 9, a layer 224 is electroless plated onto activation layer 222. The material of layer 224 can be referred to as a second material to distinguish the material from the first material of layer 220. Layer 224 preferably comprises a solder-wettable material, and is formed within opening 212 to effectively line sidewalls of the opening with the solder-wettable material.

[0071] Layer 224 can comprise, consist essentially of, or consist of, for example, nickel. In such aspects, layer 224 can be formed by dipping construction 200 into a nickel hypophosphate solution utilizing an operating temperature of from about 59°C to about

64°C, and a deposition time of from about 5 minutes to about 10 minutes. The nickel hypophosphate solution can be a solution manufactured by Shipley Corporation for utilization with p-dimethylaminobenzaldeyhyde (DMAB) applications. The nickel hypophosphate solution will typically have a pH of from about 5 to 7, with a preferred pH being about 7. The electroless-plated layer 224 can have a thickness of from about 1 micron to about 7 microns, with about 5 microns being a preferred thickness. If the thickness gets too low, a solder material formed over the nickel layer (the solder material is described below) can consume the electroless-plated layer before the opening 212 is completely filled with solder, so that the electroless-plated material does not accomplish the desired task of providing adequate wetting for solder utilized to fill opening 212.

[0072] As discussed previously, activation and subsequent electroless plating is but one of many methods that can be utilized for plating a solder-wetting material over a metal nitride. Other methods include, for example, activationless plating onto the metal nitride, and formation of a low temperature chemical vapor deposited layer onto the metal nitride followed by plating onto the low temperature chemical vapor deposited layer. If such other methods are utilized, the activation layer 222 can be omitted, or can be substituted by a low temperature chemical vapor deposited layer. Alternatively, the activation layer can be formed over a low temperature chemical vapor deposited layer which in turn is formed over the metal nitride.

[0073] Although layer 224 is shown formed after removal of layer 220 from over back-side surface 210, it is to be understood that the invention encompasses other aspects in which electroless-plated material 224 is provided prior to removal of layer 220 from over the

back-side surface, and in which both the electroless-plated material and material 220 are removed from over the back-side surface.

[0074] Referring to Fig. 10, insulative-material layer 204 (Fig. 9) is removed to leave an opening 232 in the polyimide-containing layer 202 where an outer lead bond is to be formed. Also, an upper region of opening 212 is extended to form a region 230 of the opening that extends entirely across the gap within conductive-material layer 100. Accordingly, the extended region 230 of opening 212 has a periphery comprising an exposed surface of conductive material 100. In particular aspects of the invention, the opening 212 can be considered a first opening which does not extend to the conductive material 100, and the extended region 230 can be considered a portion of the first opening which is extended to reach the conductive material 100. The formation of extended region 230 can be accomplished utilizing any suitable etch. Although an entirety of insulative material 204 is shown removed during formation of extended region 230, it is to be understood that the invention encompasses other aspects in which only a portion of material 204 is removed to form the extended region 230. Regardless, at least some of the material 204 is removed.

[0075] In the shown aspect of the invention, the formation of extended region 230 occurs after activation of first material 220, and also after formation of electroless-plated material 224. It is to be understood, however, that the invention encompasses other aspects in which the extended region 230 is formed before one or both of the activation of material 220 and formation of plated material 224.

[0076] The removal of layer 204 (Fig. 9) changes the location of front-side surface 208 so that the surface is now associated with a surface of layer 202 rather than with a surface of layer 204.

[0077] Referring to Fig. 11, a solder 240 is provided within opening 212 and within extended region 230. Solder 240 can be provided by, for example, utilizing wave-solder methodologies which apply the solder from a back side of the component 200. Accordingly, the solder fills opening 212, but does not extend into other typographical features associated with the front side of component 200, including, for example, the opening 232.

[0078] Solder 240 can comprise any suitable solder composition, including, for example, compositions containing 63% tin and 37% lead (by weight), 96.5% tin and 3.4% silver (by weight), or 96.5% tin, 3% silver and 0.5% copper (by weight).

[0079] The solder-wetting material 224 advantageously assists in allowing the solder to flow into narrow opening 212 at relatively low temperatures, while providing a uniform, quality fill within the opening. Exemplary temperatures for provision of the solder within the opening are at or below about 200°C.

[0080] Referring to Fig. 12, a conductive-material layer 250 is formed over exposed conductive materials 100 and 240 on front surface 208. The conductive material 250 can comprise, consist essentially of, or consist of, for example, nickel, and can be formed utilizing electroless-plating technology. The conductive material 250 within gap 232 forms a portion of an outer lead 252. The conductive material 250, together with solder 240, forms an inner lead 254 which extends within opening 212.

[0081] Referring to Fig. 13, polyamide-containing material 202 (Fig. 12) is removed, and a solder ball 260 is formed over the conductive material 250 of outer lead 252. The

removal of material 202 shifts the front-side surface 208 of component 200 to outer surfaces of trace 100, material 114, and exposed materials 250 and 260. Although the solder ball 260 is shown selectively formed over material 250 of outer lead 252, and not over material 250 of inner lead 254, it is to be understood that a solder ball could also be formed over the inner lead.

[0082] The processing of Figs. 6-13 illustrates one exemplary aspect of the invention. Another exemplary aspect is described with reference to Figs. 14-16. In referring to Figs. 14-16, identical numbering will be used as was utilized above in describing Figs. 6-13, where appropriate.

[0083] Fig. 14 illustrates a construction 300 at a processing step subsequent to that of Fig. 7. Expanded region 230 has been formed after formation of conductive material 220, and prior to removal of conductive material 220 from back-side surface 210 of the component.

[0084] Fig. 15 shows activation layer 222 and electroless-plated layer 224 formed along material 220. Fig. 15 also shows material 220 removed from over back-side surface 210. Such removal can occur before or after formation of one or both of activating layer 222 and electroless-plated layer 224. Additionally, Fig. 15 shows removal of insulative material 204 (Fig. 14) from over polyamide-containing material 202, which leaves a gap 232 exposed to a location where an outer lead is to be formed. The removal of material 204 preferably occurs after formation of activating layer 222 and electroless-plated layer 224, in order to avoid formation of an electroless-plated material on the conductive material 100 within opening 232. However, the invention encompasses other aspects (not shown) wherein it is desired to form an electroless-plated material within opening 232 simultaneously to forming

the electroless-plating material 224, and such aspects it can be desired to expose the conductive material 100 within opening 232 to the conditions utilized for forming layers 222 and 224.

[0085] Referring to Fig. 16, solder 240 is provided within opening 212 and extended region 230, conductive-material caps 250 are provided within regions 230 and 232 (the region 232 is labeled in Fig. 15), and a solder ball 260 is provided over the conductive material 250 in opening 232. The construction of Fig. 16 is comparable to the construction of Fig. 13, but differs in that polyamide-containing material 202 has been left over the construction of Fig. 16 during formation of solder ball 260, in accordance with an alternative aspect of the invention relative to that of Fig. 13.

[0086] The low-temperature processing of the present invention can provide numerous advantages. For instance, the process can be utilized in so-called "back-end" processes where heating above the low temperatures utilized in the invention can be detrimental or is simply not possible. Additionally, methodology of the invention can be utilized with metallization of plastics and other materials that may be sensitive to temperature.

CLAIMS

The invention claimed is:

1. A method of fabricating an interconnect for a semiconductor component, comprising:

providing a semiconductor component;

forming an opening which extends entirely through the component, the opening having sidewalls;

depositing a first material along the sidewalls of the opening, the depositing being conducted at a temperature of less than or equal to about 200°C; and

plating a second material within the opening and over the first material.

2. The method of claim 1 wherein the depositing comprises one or both of ALD and CVD.

3. The method of claim 1 wherein the depositing comprises one or both of ALD and CVD, and wherein the depositing utilizes multiple cycles which individually form less than or equal to about 10Å of the first material.

4. The method of claim 3 wherein the first material is formed to a thickness of at least about 100Å.

5. The method of claim 3 wherein the first material is formed to a thickness of from about 100Å to about 300Å.

6. The method of claim 1 wherein the component comprises a semiconductor material wafer.

7. The method of claim 1 wherein the component comprises a monocrystalline silicon wafer.

8. The method of claim 1 wherein the opening has a length through the component and a maximum dimension orthogonal to the length of less than or equal to about 100 microns.

9. The method of claim 1 wherein the first material is an electrically-conductive material.

10. The method of claim 1 wherein the first material comprises a metal nitride.

11. The method of claim 1 wherein the first material consists essentially of a metal nitride.

12. The method of claim 1 wherein the first material consists of a metal nitride.

13. The method of claim 1 wherein the first material comprises one or more of titanium nitride, tungsten nitride, tantalum nitride and hafnium nitride.

14. The method of claim 1 wherein the first material consists essentially of one or more of titanium nitride, tungsten nitride, tantalum nitride and hafnium nitride.

15. The method of claim 1 wherein the first material consists of one or more of titanium nitride, tungsten nitride, tantalum nitride and hafnium nitride.

16. The method of claim 1 wherein the plating is electroless plating.

17. The method of claim 16 wherein the second material comprises nickel.

18. The method of claim 16 wherein the first material comprises a metal nitride, and further comprising activating the metal nitride with one or both of Hf and Pd prior to the electroless plating.

19. The method of claim 18 wherein the activating the metal nitride forms a layer comprising one or both of Hf and Pd over the metal nitride, and wherein the layer comprising one or both of Hf and Pd has a thickness of from about 1 micron to about 7 microns.

20. The method of claim 19 wherein the layer comprising one or both of Hf and Pd has a thickness of at least about 5 microns.

21. The method of claim 1 wherein the component comprises a first side and an opposing second side, wherein the opening extends from the first side to the second side, the method further comprising forming a conductive-material pad over the first side, and wherein the opening is formed through the conductive-material pad.

22. The method of claim 1 wherein the second material is a solder-wetting material, and further comprising forming solder within the opening and along the solder-wetting material.

23. The method of claim 22 wherein the solder-wetting material comprises nickel.

24. A method of fabricating an interconnect for a semiconductor component, comprising:

providing a semiconductor component;

forming an opening which extends entirely through the component, the opening having sidewalls;

depositing a metal nitride along the sidewalls of the opening, the depositing being conducted in a reaction chamber utilizing:

a first precursor containing the metal of the metal nitride;

a second precursor containing the nitrogen of the metal nitride; and

at least one cycle in which the first and second precursors are in the reaction chamber at different and substantially non-overlapping time intervals relative to one another; and

plating a second material within the opening and over the metal nitride.

25. The method of claim 24 wherein the plating is electroless plating.

26. The method of claim 24 wherein the component comprises a semiconductor material wafer.

27. The method of claim 24 wherein the component comprises a monocrystalline silicon wafer.

28. The method of claim 24 wherein the opening has a length through the component and a maximum dimension orthogonal to the length of less than or equal to about 100 microns.

29. The method of claim 24 wherein a temperature of the component during the at least one cycle is less than or equal to about 200°C.

30. The method of claim 24 wherein a temperature of the component during the at least one cycle is less than or equal to about 160°C.

31. The method of claim 24 wherein the metal nitride is titanium nitride, tungsten nitride, tantalum nitride or hafnium nitride.

32. The method of claim 24 wherein the metal nitride is titanium nitride.

33. The method of claim 32 wherein the first precursor is $TiCl_4$ and the second precursor is NH_3.

34. The method of claim 32 wherein the first precursor is TDMAT and the second precursor is NH_3.

35. The method of claim 34 wherein the cycle utilizes, in the following sequential order, a first pulse of the TDMAT into the reaction chamber, a substantial purge of the TDMAT from the reaction chamber, and a second pulse of the NH_3 into the reaction chamber.

36. The method of claim 35 wherein the first pulse is for a time of about 1 second, the purge is for a time of about 10 seconds and utilizes a purge gas which is inert relative to reaction with the TDMAT and the component, and the second pulse is for a time of about 4 seconds.

37. The method of claim 24 wherein, during each of the at least one cycles, the first precursor is introduced into the reaction chamber before the second precursor.

38. The method of claim 24 wherein each of the at least one cycles individually forms a layer of the metal nitride that is less than or equal to about 10Å thick.

39. The method of claim 38 wherein enough of the cycles are utilized so that the depositing forms the metal nitride to be at least about 100Å thick.

40. The method of claim 38 wherein enough of the cycles are utilized so that the depositing forms the metal nitride to be from about 100Å thick to about 300Å thick.

41. The method of claim 24 wherein the second material is a solder-wetting material, and further comprising forming solder within the opening and along the second material.

42. The method of claim 41 wherein the second material comprises nickel.

43. A method of fabricating an interconnect for a semiconductor component, comprising:

providing a semiconductor component, the component comprising a monocrystalline semiconductor material having a pair of opposing sides, the component comprising a front side outwardly of one of the opposing sides of the monocrystalline semiconductor material and a back side outwardly of the other of the opposing sides of the monocrystalline semiconductor material, the component further comprising a conductive-material layer proximate the front side;

forming an opening which extends from the front side to the back side and thus extends entirely through the semiconductor component, the opening having sidewalls and extending through the conductive-material layer;

depositing a first material along the sidewalls of the opening to narrow the opening, the depositing utilizing one or more cycles of a process which forms less than or equal to about 10Å of the first material per cycle and which exposes the component to a temperature of less than or equal to about 200°C;

forming a solder-wetting material within the opening and along the first material; and

forming solder along the solder-wetting material to fill the opening with solder; the solder within the opening electrically connecting with the conductive-material layer.

44. The method of claim 43 wherein the first material is a metal nitride and wherein the process is conducted in a reaction chamber utilizing:

a first precursor containing the metal of the metal nitride;

a second precursor containing the nitrogen of the metal nitride; and

provision of the first and second precursors in the reaction chamber at different and substantially non-overlapping time intervals relative to one another.

45. The method of claim 44 wherein the metal nitride is titanium nitride, tungsten nitride, tantalum nitride or hafnium nitride.

46. The method of claim 44 wherein the metal nitride is titanium nitride.

47. The method of claim 46 wherein the first precursor is $TiCl_4$ and the second precursor is NH_3.

48. The method of claim 46 wherein the first precursor is TDMAT and the second precursor is NH_3.

49. The method of claim 48 wherein the process utilizes, in the following sequential order, a first pulse of the TDMAT into the reaction chamber, a substantial purge of the TDMAT from the reaction chamber, and a second pulse of the NH_3 into the reaction chamber.

50. The method of claim 43 wherein the semiconductor component comprises a first insulative-material layer over the conductive-material layer and a second insulative-material layer over the first insulative-material layer, and wherein the second insulative-material layer has a surface corresponding to the front side of the semiconductor component.

51. The method of claim 50 wherein the first insulative-material layer comprises polyimide and the second insulative-material layer comprises silicon dioxide.

52. The method of claim 43 wherein a gap extends through the conductive-material layer, and wherein the forming the opening comprises:

forming a first opening within the gap, the first opening not extending to the conductive-material layer; and

extending a portion of the first opening to the conductive-material layer.

53. The method of claim 52 wherein the extending occurs prior to the forming of the solder-wetting material.

54. The method of claim 52 wherein the forming of the solder-wetting material comprises electroless plating of the solder-wetting material.

55. The method of claim 54 wherein the first material comprises a metal nitride, and further comprising activating the metal nitride with one or both of Hf and Pd prior to the electroless plating.

56. The method of claim 55 wherein the activating occurs prior to the extending.

57. The method of claim 55 wherein the activating occurs after the extending.

58. The method of claim 54 wherein the extending occurs after the electroless plating.

59. The method of claim 52 further comprising forming an electrically-insulative material over the conductive material and within the gap in the layer of conductive material, wherein the first opening extends through the electrically-insulative material, and wherein the extending comprises removing at least a portion of the electrically-insulative material.

60. The method of claim 59 wherein the electrically-insulative material comprises a silicon dioxide-containing layer.

61. The method of claim 60 further comprising forming a polymide-containing layer over the layer of conductive material, and wherein the silicon dioxide-containing layer is over the polymide-containing layer.

62. The method of claim 43 wherein the first material comprises a metal nitride.

63. The method of claim 43 wherein the first material consists essentially of a metal nitride.

64. The method of claim 43 wherein the first material consists of a metal nitride.

65. The method of claim 43 wherein the first material comprises one or more of titanium nitride, tungsten nitride, tantalum nitride and hafnium nitride.

66. The method of claim 43 wherein the first material consists essentially of one or more of titanium nitride, tungsten nitride, tantalum nitride and hafnium nitride.

67. The method of claim 43 wherein the first material consists of one or more of titanium nitride, tungsten nitride, tantalum nitride and hafnium nitride.

68. The method of claim 43 wherein the forming of the solder-wetting material comprises electroless plating of the solder-wetting material.

69. The method of claim 68 wherein the first material comprises a metal nitride, and further comprising activating the metal nitride with one or both of Hf and Pd prior to the electroless plating.

70. The method of claim 43 wherein the depositing forms the first material along the back side of the semiconductor wafer, and further comprising removing the first material from over the back side of the semiconductor wafer.

71. The method of claim 70 wherein the forming of the solder-wetting material comprises electroless plating of the solder-wetting material, and wherein the removing occurs prior to the electroless plating.

72. The method of claim 71 wherein the first material comprises a metal nitride, and further comprising activating the metal nitride with one or both of Hf and Pd prior to the electroless plating.

73. The method of claim 72 wherein the activating occurs prior to the removing.

74. The method of claim 72 wherein the activating occurs after the removing.

75. The method of claim 70 wherein the forming of the solder-wetting material comprises electroless plating of the solder-wetting material, and wherein the removing occurs after the electroless plating.