PROCESS FOR FABRICATING A SUBSTRATE FOR A FRONT-SIDE IMAGE SENSOR

FIELD OF THE INVENTION

The present invention relates to a process for fabricating a substrate for a front-side image sensor.

PRIOR ART

Semiconductor-on-insulator structures, and in particular Silicon-On-Insulator (SOI) substrates, are advantageous substrates for the fabrication of front-side image sensors.

An SOI substrate has, from its back face to its front face, a carrier substrate made of silicon that is doped to a certain degree, a silicon oxide layer referred to as a "buried oxide layer" (often referred to by the acronym "BOX"), and a layer referred to as an active silicon layer with doping that may be different from that of the carrier substrate. A matrix array of photodiodes, each one defining a pixel of the image sensor, is arranged in the active layer.

In some applications, the buried oxide layer is chosen to be relatively thin (i.e. to be less than 100 nm, and in particular between 20 nm and 50 nm, thick) in order to play the role of the dielectric of a capacitor by allowing the pixel to be biased via the back face. The portion of the carrier substrate located below the buried oxide layer is biased to a voltage that is different from the voltage of the active layer, which allows the interface between the dielectric layer and the active layer to be passivated. The voltage to be applied to the portion of the carrier substrate located below the buried oxide layer depends on the thickness of this layer. The potential difference to be applied is proportional to the thickness of the buried oxide layer: the thinner the buried oxide layer, the smaller the potential difference to be applied.

Another function of this buried oxide layer is to prevent parasitic signals due to the recombination, in the carrier substrate, of photons that were not absorbed during their travel through each pixel from being picked up (crosstalk prevention), with the understanding that the buried oxide layer may, depending on the chosen thickness, be only partially reflective and/or absorbent with respect to incident photons.

One drawback of the processes for fabricating image sensors is how sensitive they are to contamination by metals. Specifically, both the SOI substrate itself and the pixel may be exposed to metals during their fabrication processes. This exposure results in particular in the presence of metal atoms within the active layer. However, even at low concentrations, metal atoms, in particular copper atoms, may lead to an unacceptable loss of image-sensor performance. Specifically, metal atoms are able to interact with the electric charges generated by photons captured in pixels and negatively affect their collection performance.

To overcome this drawback, it is known practice to form a layer for trapping metal atoms within the SOI substrate.

Document US 6,083,324 thus describes the formation of a trapping layer in the active layer of the SOI substrate by ion-implanting gaseous species and then carrying out a heat treatment suitable for forming, from the implanted ions, microbubbles or precipitates. These microbubbles or precipitates form trap sites for metal atoms. However, this trapping layer, due to the cavities and interfaces that it forms in the pixel, may interfere with the trajectory of photons through the pixels and negatively affect the electrical performance of the image sensor.

Document US 2010/0090303 describes the formation of a trapping layer in the carrier substrate. More specifically, when the SOI substrate is formed using a Smart Cut™ layer transfer technique, the process for fabricating the SOI substrate comprises the following steps:

- providing a silicon donor substrate covered with a layer of silicon oxide that is intended to form the BOX and comprising a weakened zone delimiting a thin layer of silicon;
- providing a carrier substrate in which the trapping layer has been formed by ion implantation;
- bonding the donor substrate and the carrier substrate via the oxide layer;
- detaching the donor substrate along the weakened zone in order to transfer the thin layer of silicon and the oxide layer to the carrier substrate;
- epitaxially growing an additional layer of silicon on top of the transferred thin layer until the desired thickness for the active layer of the image sensor has been obtained.

However, the surface state of the carrier substrate that has undergone ion implantation for the purpose of forming the trapping layer is of insufficient quality to provide a good bonding hold if the buried oxide layer is very thin, which is a notable drawback of this process in particular in the context of bonding thin oxides such as those targeted for a near-infrared front-side image sensor.

SUMMARY OF THE INVENTION

There is therefore still a need to form a trapping zone in the carrier substrate of a semiconductor-on-insulator structure for forming a front-side image sensor while guaranteeing good adhesion between the active layer and the carrier substrate.

An aspect of the present invention provides a process for fabricating a substrate for a front-side image sensor, comprising:

providing a donor substrate comprising a semiconductor layer to be transferred;

providing a semiconductor carrier substrate;

bonding the donor substrate to the carrier substrate, an electrically insulating layer being at the bonding interface;

transferring the semiconductor layer to the carrier substrate;

implanting gaseous ions into the carrier substrate through the transferred semiconductor layer and the electrically insulating layer;

after said implantation, epitaxially growing an additional semiconductor layer on top of the transferred semiconductor layer.

Advantageously, said process comprises a heat treatment carried out at a temperature suitable for causing cavities to develop from the implanted gaseous ions, said cavities forming a layer for trapping metal atoms in the carrier substrate.

According to one embodiment, said heat treatment is carried out during the epitaxial growth of the additional semiconductor layer.

Preferably, the density of cavities in the trapping layer is higher than or equal to 10^{15} cavities/cm^3.

According to one embodiment, each semiconductor layer is a silicon layer.

According to one embodiment, the electrically insulating layer is a silicon oxide layer.

Alternatively, the electrically insulating layer consists of a stack of dielectric and/or metal materials.

Preferably, the thickness of the electrically insulating layer is between 5 nm and 400 nm, and preferably between 30 nm and 150 nm.

Preferably, the gaseous ions comprise helium ions.

According to one embodiment, the transfer of the semiconductor layer comprises:

- forming a weakened zone in the donor substrate in order to define said semiconductor layer to be transferred;

- after bonding, the donor substrate is detached along the weakened zone.

There is also disclosed a process for fabricating a front-side image sensor, comprising the fabrication of a substrate using the process as described above, the transferred semiconductor layer and the additional semiconductor layer together forming an active layer of said image sensor, and the formation, in said active layer, of a plurality of electrically isolating trenches in order to define a plurality of pixels.

BRIEF DESCRIPTION OF THE FIGURES

Other features and advantages of the invention will emerge from the detailed description which follows, with reference to the appended drawings in which:

- Figure 1A is a sectional view of an SOI substrate for an image sensor according to one embodiment of the invention;

- Figure 1B is a sectional view of a substrate according to one variant of Figure 1A;

- Figure 2 schematically illustrates the implantation of atomic species into a donor substrate in order to form a weakened zone there delimiting a semiconductor layer to be transferred;

- Figure 3 schematically illustrates the bonding of the weakened donor substrate of Figure 2 to a carrier substrate;

- Figure 4 schematically illustrates the transfer of the semiconductor layer to the carrier substrate in order to form an SOI structure;

- Figure 5 schematically illustrates the implantation of helium into the SOI structure of Figure 4;

- Figure 6 illustrates the substrate obtained after forming electrically isolating trenches in the substrate of Figure 1 in order to singulate each pixel of the image sensor, said substrate having undergone a re-epitaxy step beforehand;

- Figure 7 shows images of a section of the substrate of Figure 5 produced by transmission electron microscopy (the right-hand image being an enlargement of the left-hand image);

- Figure 8 is an image produced by transmission electron microscopy of a section of the substrate of Figure 5 after an additional heat treatment has been applied to the substrate with respect to the images of Figure 7;

- Figure 9 shows a measurement, taken by secondary-ion mass spectrometry (SIMS), of copper concentration illustrating the diffusion thereof within the substrate of Figure 5, superposed over an image of a section of said substrate produced by transmission electron microscopy;

- Figure 10 shows an SIMS measurement of copper concentration illustrating the diffusion thereof within a substrate like that of Figure 5 but without a trapping layer;

- Figure 11 shows an SIMS measurement of copper concentration illustrating the diffusion thereof within the substrate of Figure 5.

To make the drawings clearer, the various layers have not been drawn to scale. Reference signs which are identical from one figure to the next have been used to reference elements that are identical or that perform the same function.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

Figure 1A illustrates an SOI substrate for an image sensor according to one embodiment of the invention.

Said substrate successively comprises, from its back face to its front face, a carrier substrate 1, an electrically insulating layer 2 and a semiconductor layer 3, referred to as the active layer, which is intended for the formation of the pixels of the image sensor.

A layer 4 for trapping metal atoms is arranged at a certain depth in the carrier substrate 1, not necessarily in contact with the electrically insulating layer 2. As will be described in detail below, said layer 4 comprises cavities that develop from gaseous ions implanted into the carrier substrate under the effect of a heat treatment. The density of cavities in said trapping layer 4 is advantageously higher than or equal to 10^{15} cavities/cm^3. Said cavities

make it possible to capture metal atoms that are present in the SOI substrate in the vicinity of the electrically insulating layer 2, which may negatively affect the correct operation of the sensor. These atoms may be initially present in the carrier substrate 1 and/or in the active layer 3 and diffuse through the SOI substrate under the effect of heat treatments until reaching the trapping layer 4, where they are captured.

The carrier substrate is advantageously a silicon, in particular monocrystalline silicon, substrate.

The electrically insulating layer 2 may be a layer of silicon oxide, which is a conventional insulator in the field of silicon-on-insulator substrates.

Alternatively, the electrically insulating layer may consist of a stack of various dielectric and/or metal materials, such as what is known as an "ONO", i.e. oxide-nitride-oxide, stack. The constituent materials of said stack are advantageously chosen so as to increase the reflectivity of the electrically insulating layer in the infrared in comparison with a layer of silicon oxide of the same total thickness. Preferably, a metal layer is encapsulated between two dielectric layers, which thus prevents any metal contamination of the active layer. This makes it possible to avoid the generation of electrical defects at the interface between the active layer and the electrically insulating layer and recombinations between the semiconductor material of the active layer and the metal components of the image sensor, which could dope the active layer.

According to one particular embodiment illustrated in Figure 1B, the electrically insulating layer 2 comprises a layer 22 of silicon nitride between two layers 21, 23 of silicon oxide. The thickness of the layer 21, which is arranged on the carrier-substrate 1 side, is between 50 nm and 500 nm, the thickness of the layer 23, which is arranged on the active-layer 3 side, is between 5 nm and 50 nm and the thickness of the layer 22 is between 10 nm and 100 nm. Such an electrically insulating layer has the advantage of reflecting the photons transmitted through the active layer 3 better than a layer of silicon oxide of the same thickness of the substrate of Figure 1A.

Particularly advantageously, whether it consists of one or of several materials, the electrically insulating layer 2 is thin, i.e. it is between 5 nm and 400 nm, and preferably between 30 nm and 150 nm, thick. Such a layer forms no barrier to the diffusion of metal, in particular copper, atoms. It is therefore not necessary, as in document US 2010/0090303, to damage the electrically insulating layer locally in order to allow atoms to pass through.

The active layer is advantageously monocrystalline. As schematically shown in Figure 1, the active layer 3 is formed by stacking a first layer 3a and an additional layer 3b, the layer 3b being fabricated by epitaxy on top of the layer 3a, which then serves as a seed layer. The materials of the layers 3a and 3b advantageously exhibit similar lattice parameters and coefficients of thermal expansion which make it possible to minimize the formation of crystal defects within the layer 3b as it is epitaxially grown. According to one

preferred embodiment, the layers 3a and 3b consist of the same material, typically silicon or silicon-germanium. The layers 3a and/or 3b may potentially be doped.

The thickness of the layer 3 is typically greater than or equal to 1 µm.

A process for fabricating the substrate of Figure 1A based on the Smart Cut™ method will now be described with reference to Figures 2 to 5.

With reference to Figure 2, a donor substrate 30 covered with the electrically insulating layer 2 is provided. The electrically insulating layer may be formed by thermally oxidizing the material of the donor substrate and/or by depositing one or more dielectric and/or metal layers. A weakened zone, which delimits the semiconductor layer 3a to be transferred, is formed by implanting atomic species (represented by arrows) into the donor substrate 30. The atomic species implanted for this purpose advantageously comprise hydrogen and/or helium.

With reference to Figure 3, the donor substrate 30 is bonded to the carrier substrate 1, the electrically insulating layer 2 being at the bonding interface.

With reference to Figure 4, the donor substrate 30 is detached along the weakened zone 31 in order to transfer the semiconductor layer 3a to the carrier substrate 1.

With reference to Figure 5, gaseous (for example helium) ions are implanted into the carrier substrate 1 through the semiconductor layer 3a and the electrically insulating layer 2. A person skilled in the art is capable of defining the implantation parameters, in particular the dose and implantation energy, so as to localize said gaseous ions 40 in a layer in the thickness of the carrier substrate 1. By way of indication, a dose of between 1E16 atoms/cm^2 and 5E17 atoms/cm^2 is suitable for obtaining a density of cavities of at least 10E15 cavities/cm^3. The implantation energy is typically between a few keV and 120 keV. A person skilled in the art will choose a suitable energy according to the thicknesses of the layers through which the ions have to pass for said ions to be localized in the carrier substrate below the electrically insulating layer.

A heat treatment is next carried out to develop cavities from the implanted gaseous ions in order to form a layer for trapping metal atoms. Generally speaking, this treatment involves heating the substrate to a temperature of between 850°C and 1200°C for a duration of between 30 minutes and 180 minutes. This heat treatment may be carried out as a specific step in the process. However, it may be advantageous to use the thermal budget of another step in the process, for example a step of finishing the SOI substrate (such as an anneal for smoothing or for healing defects) or the epitaxy step carried out in order to grow the additional semiconductor layer 3b on top of the transferred layer 3a.

As an alternative to the Smart Cut™ process described above, the semiconductor layer may be transferred, after bonding the donor substrate to the carrier substrate, by thinning the donor substrate from its face opposite the bonding interface, for example by

etching, until the desired thickness for the transferred semiconductor layer is obtained. The formation of the weakened zone is not necessary in this case.

Forming the trapping layer after bonding the donor substrate to the carrier substrate, rather than before as described in document US 2010/0090303, makes it possible to ensure that the surfaces to be bonded are of optimum quality and consequently that the adhesion between the two substrates is good, even if the electrically insulating layer is thin. Additionally, implanting the gaseous ions before the epitaxy of the additional semiconductor layer makes it possible to minimize the implantation energy and to avoid damaging the active layer.

With reference to Figure 6, the additional semiconductor layer 3b is grown by epitaxy on top of the transferred layer 3a until the desired thickness for the active layer 3 is obtained. As mentioned above, the thermal budget of this epitaxy may be used to develop the cavities that form the trapping layer 4. Next, trenches are formed through the active layer 3 down into the electrically insulating layer 2, and said trenches 5 are filled with a dielectric material in order to electrically isolate the pixels of the image sensor.

Experimental results

SOI substrates such as illustrated in Figure 5 have been produced and the trapping layer has been formed by developing cavities from the implanted gaseous ions by heating some of said SOI substrates to a temperature of 950°C for 40 minutes (see Figure 7).

Said substrates then underwent heat treatments that SOI substrates including the layer for trapping metal atoms may undergo in order to check that the trapping layer is stable and remains operational even after having undergone a heat treatment with a high thermal budget (see Figure 8). It is assumed that the thermal budget of a treatment at 1100°C for two hours is the maximum thermal budget that allows the trapping properties of the cavity layer to be conserved. This thermal budget is compatible with finishing steps and potentially epitaxy.

Figure 7 shows images of a section of the substrate of Figure 5 produced by transmission electron microscopy (the right-hand image being an enlargement of the left-hand image) after a heat treatment for developing the cavities has been carried out. Within the carrier substrate 1 it is possible to see the cavities arranged in a layer 4 forming a layer for trapping metal atoms. In the example illustrated, the thickness of the layer 4 is 179 nm and it is buried at a depth of 205 nm below the interface between the carrier substrate 1 and the electrically insulating layer 2.

Figure 8 is an image produced by transmission electron microscopy of a section of the substrate of Figure 5 after an additional heat treatment has been applied to the substrate with respect to the images of Figure 7, said heat treatment being carried out at a temperature of up to 1100°C for a duration of less than or equal to two hours. In the

thickness of the carrier substrate 1, at the implantation depth of the gaseous ions, it is possible to see cavities arranged in the layer 4 which forms a layer for trapping metal atoms.

Figure 9 shows a measurement, taken by secondary-ion mass spectrometry (SIMS), of copper concentration in the substrate of Figure 5, superposed over an image of a section of said substrate produced by transmission electron microscopy. To carry out this measurement, a layer of copper was deposited on top of the semiconductor layer 3a and a heat treatment (800°C for two hours) was carried out to diffuse the copper atoms into the substrate. This heat treatment was chosen for demonstration purposes to ensure, taking into account the physical diffusion properties of copper in silicon and silicon oxide, complete dispersion of this element into the material. This measurement thus reflects the ability of copper atoms to pass through the electrically insulating layer 2 and be trapped by the trapping layer 4. Thus, while the concentration of copper atoms in the layer 3a is about 1.1E11 atoms/cm^3 and about 1.8E9 atoms/cm^3 in the electrically insulating layer, the curve shows a peak at the layer 4 with a concentration of copper atoms of about 2.3E13 atoms/cm^3. The concentration of copper atoms below the layer 4 is very low.

Figures 10 and 11 show an SIMS measurement of copper concentration within a substrate like that of Figure 5 without and with the trapping layer 4, respectively. To carry out this measurement, a layer of copper was deposited on the back face of the carrier substrate 1 and a heat treatment (800°C for two hours) was carried out to diffuse the copper atoms into the substrate. In the case of Figure 10 (no trapping layer), a high concentration of copper atoms is observed in the carrier substrate 1 below the electrically insulating layer (peak P1) and a high concentration of copper atoms is observed in the transferred layer in the vicinity of the free surface of said layer (peak P2). In the case of Figure 11 (a trapping layer according to the invention being present), it is observed that the copper-atom concentration peak P3 is localized in the trapping layer.

REFERENCES

US 6,083,324

US 2010/0090303

CLAIMS

1. A process for fabricating a substrate for a front-side image sensor, comprising:

- providing a donor substrate comprising a semiconductor layer to be transferred;
- providing a semiconductor carrier substrate;
- bonding the donor substrate to the carrier substrate, an electrically insulating layer being at the bonding interface;
- transferring the semiconductor layer to the carrier substrate;
- implanting gaseous ions into the carrier substrate through the transferred semiconductor layer and the electrically insulating layer;
- after said implantation, epitaxially growing an additional semiconductor layer on top of the transferred semiconductor layer.

2. Process according to Claim 1, comprising a heat treatment carried out at a temperature suitable for causing cavities to develop from the implanted gaseous ions, said cavities forming a layer for trapping metal atoms in the carrier substrate.

3. Process according to Claim 2, wherein said heat treatment is carried out during the epitaxial growth of the additional semiconductor layer.

4. Process according to either of Claims 2 and 3, wherein the density of cavities in the trapping layer is higher than or equal to 10^{15} cavities/cm^3.

5. Process according to one of Claims 1 to 4, wherein each semiconductor layer is a silicon layer.

6. Process according to one of Claims 1 to 5, wherein the electrically insulating layer is a silicon oxide layer.

7. Process according to one of Claims 1 to 6, wherein the electrically insulating layer consists of a stack of dielectric and/or metal materials.

8. Process according to one of Claims 1 to 7, wherein the thickness of the electrically insulating layer is between 5 nm and 400 nm, and preferably between 30 nm and 150 nm.

9. Process according to one of Claims 1 to 8, wherein the gaseous ions comprise helium ions.

10. Process according to one of Claims 1 to 9, wherein the transfer of the semiconductor layer comprises:

- forming a weakened zone in the donor substrate in order to define said semiconductor layer to be transferred;

- after bonding, detaching the donor substrate along the weakened zone.

11. Process for fabricating a front-side image sensor, comprising the fabrication of a substrate using the process according to one of Claims 1 to 10, the transferred semiconductor layer and the additional semiconductor layer together forming an active layer of said image sensor, and the formation, in said active layer, of a plurality of electrically isolating trenches in order to define a plurality of pixels.