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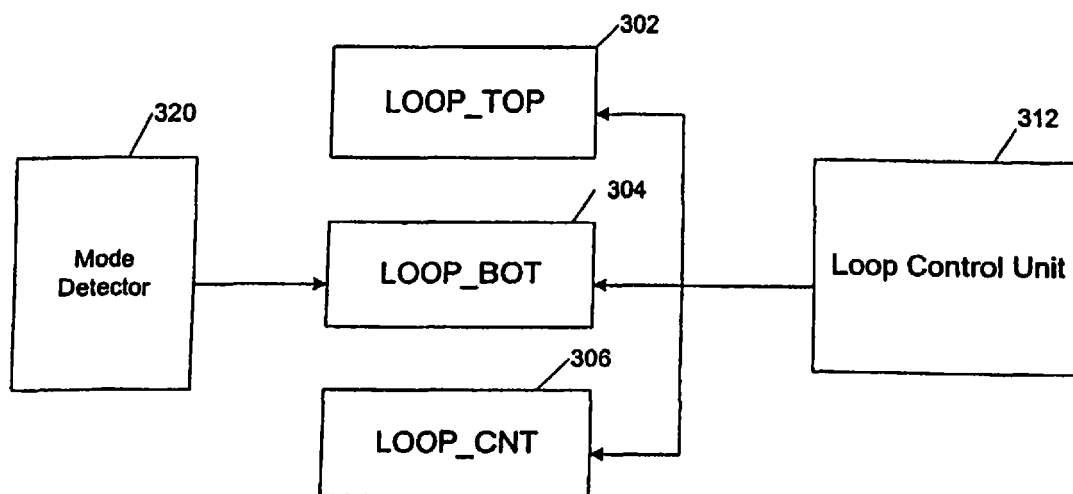
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(54) Title: SECURITY OF HARDWARE LOOPS



(57) Abstract: In an embodiment, a processor may be operable in a user mode and in a supervisor mode. The processor may initialize hardware loops in the user mode by loading a top instruction address in LOOP\_TOP register and a bottom instruction address in a LOOP\_BOT register. A user program could conceivably gain access to the supervisor mode by loading the target address of an event service routine, in the supervisor instruction address space, in the LOOP\_BOT register an address in the user instruction address space in the LOOP-TOP register. If the event occurred in the supervisor mode, the program flow could branch to the address in the LOOP\_TOP register, giving the user program control in the supervisor mode. To avoid this potential security hazard, the processor may disable hardware loop operations when the processor exits the user mode

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