electrically conductive interlayer 228 via the bonding material 230, the partially processed CMOS device layer 204 is attached to a handle wafer such that the surface of the partially processed CMOS device layer 204 on which the at least one transistor 205 is formed is facing the handle wafer. In the present embodiment, the handle wafer is the same handle wafer as the one previously attached to the partially processed CMOS device layer 204 as described in the step 502 so that no additional step is required to attach the handle wafer at this stage. In an embodiment, a bonding oxide and/or nitride may also be deposited on a bottom side of the partially processed CMOS device layer 204 (i.e. an opposite side to the handle wafer with respect to the partially processed CMOS device layer 204).

In a step 510, the electrically conductive interlayer 228 is bonded to the partially processed CMOS device layer 204. In the present embodiment, the partially processed CMOS device layer 204 is bonded to the electrically conductive interlayer 228 via the bonding material 230. In an embodiment where another bonding oxide or nitride layer is deposited on the bottom side of the partially processed CMOS device layer 204 as discussed above, this another bonding oxide or nitride layer is bonded to the bonding material 230 deposited on the electrically conductive interlayer 228 so as to bond the partially processed CMOS device layer 204 to the electrically conductive interlayer 228. In the present embodiment where the partially processed CMOS device layer 204 is attached to the handle substrate prior to this bonding step 510, the handle substrate is removed after this bonding step 510. In some embodiments as described above, the electrically conductive interlayer 228 is bonded directly to the partially processed CMOS device layer 204.

In a step 512, vias and metal lines/interconnects are formed to electrically connect the at least one transistor 205 of the CMOS device layer 204 to the III-V device 217, 304, 406. In the present embodiments as shown in Figures 2 to 4, contact plugs 232 (e.g. tungsten plugs) are formed on the III-V device contacts such that a top surface of the contact plugs 232 are approximately co-planar with the at least one transistor 205 formed on the partially processed CMOS device layer 204. Following this, a back-end CMOS process can commence to form interconnects between the at least one transistor 205 of the partially processed CMOS device layer 204 and the III-V devices 217, 304, 406 to form an integrated circuit. For example, the interconnects can be formed on contact pads of the at least one transistor 205 and the contact plugs 232 of the III-V devices to connect

transmissible substrate 404 is bonded to the bottom device surface 405 of the III-V device 406 directly. In either case, it can be said that the light transmissible substrate 404 is bonded to the bottom device surface 405, and that the bottom device surface 405 is a surface previously attached to the substrate layer 208. Optionally, a bonding material such as a bonding oxide or a bonding nitride or a combination of the two can be formed to a bottom side of the III-V device 406 prior to the step 516 to aid in this bonding process step. In an embodiment, another bonding material can also be formed on a surface of the light transmissible substrate 404 prior to the step 516 to enhance a bonding strength of the light transmissible substrate 404 to the bottom device surface 405 of the III-V device 406. In this case, the light transmissible substrate 404 is bonded to the bottom device surface 405 of the III-V device 406, via the bonding material formed on the bottom side of the III-V device 406 and the another bonding material formed on the surface of the light transmissible substrate 404. After performing the step 516, the support wafer or structure attached to the top side 412 of the semiconductor device 402 may be optionally removed since the light transmissible substrate 404 provides sufficient structural support to the semiconductor device 402.

Figures 6 and 7 demonstrate how a size of a pixel footprint can be reduced by an implementation of the present disclosure, for example, by using the embodiments as shown in Figure 3 or 4.

Figure 6 shows a top plan-view of a circuit layout 600 according to the side-by-side configuration used in the prior art of Figure 1. In this prior art configuration, CMOS drivers 602 and CMOS control circuitry 604 cannot be placed on top of the pixel as the side-by-side configuration is adopted. In this case, the LED CMOS control circuitry 604 and drivers 602 are placed adjacent to the LED active area 606, creating a total pixel footprint of about 100μm x 100μm.

Figure 7 shows a top plan-view of a circuit layout 700 using the embodiments as shown in Figure 3 or 4 which incorporates an electrically conductive interlayer 228 between the partially processed CMOS device layer 204 and the device layer of the III-V semiconductor material layer. In this embodiment, the III-V device 304, 406 is an optoelectronic device such as a LED, and the pixel 706 contains the CMOS drivers 702, the CMOS control circuitry 704 and the LED active area. As shown in Figure 7, the CMOS control circuitry 704 in the present embodiment can be placed on top of the LED pixel

Claims

1. A method of fabricating a semiconductor device, comprising

(i) forming a III-V semiconductor material layer comprising a substrate layer and a device layer attached to the substrate layer, the device layer having a III-V device comprising a top device electrode layer and a bottom device electrode layer and an active layer formed between the top device electrode layer and the bottom device electrode layer;

(ii) forming an electrically conductive interlayer to the device layer;

(iii) bonding the electrically conductive interlayer to a bottom side of a partially processed CMOS device layer having at least one transistor formed at a top side of the partially processed CMOS device layer; and

(iv) forming a contact plug on each of the top device electrode layer and the bottom device electrode layer of the III-V device, wherein a top surface of each of the contact plugs is approximately co-planar with the at least one transistor for use in a back-end CMOS process to interconnect the at least one transistor and the III-V device to form an integrated circuit.

2. The method according to claim 1, wherein forming the III-V semiconductor material layer includes epitaxially depositing the device layer on the substrate layer.

3. The method according to any preceding claim, wherein the III-V device includes an optoelectronic device having a top device surface, a bottom device surface and an active optical area between the top device and bottom device surfaces; the bottom device surface being attached to the substrate layer and passage of light is via the bottom device surface.

4. The method according to claim 3, wherein the substrate layer includes a light transmissible substrate.

5. The method according to claim 3, further comprising removing the substrate layer after the partially processed CMOS device layer is bonded to the electrically conductive interlayer.

6. The method according to claim 5, further comprising bonding a light transmissible substrate to the bottom device surface of the optoelectronic device after removal of the substrate layer.

7. The method according to any one of claims 3 to 6, further comprising forming vias and metal lines in the back-end CMOS process to electrically connect the at least one transistor of the partially processed CMOS device layer to the optoelectronic device.

8. The method according to any preceding claim, further comprising depositing a bonding material to the electrically conductive interlayer prior to bonding the partially processed CMOS device layer to the electrically conductive interlayer, and the method further comprises chemo-mechanically polishing the bonding material.

9. The method according to any preceding claim, wherein the electrically conductive interlayer includes indium tin oxide.

10. A semiconductor device, comprising

a partially processed CMOS device layer having at least one transistor formed at a top side of the partially processed CMOS device layer;

a III-V semiconductor material layer comprising a substrate layer and a device layer attached to the substrate layer, the device layer having a III-V device, the III-V device comprises a top device electrode layer and a bottom device electrode layer and an active layer formed between the top device electrode layer and the bottom device electrode layer; and

an electrically conductive interlayer attached to a bottom side of the partially processed CMOS device layer and sandwiched between the partially processed CMOS device layer and the device layer,

wherein a contact plug is formed on each of the top device electrode layer and the bottom device electrode layer of the III-V device, a top surface of each of the contact plugs being approximately co-planar with the at least one transistor for use in a back-end CMOS process to interconnect the at least one transistor and the III-V device to form an integrated circuit.

11. The semiconductor device according to claim 10, wherein the III-V device includes an optoelectronic device having a top device surface, a bottom device surface, and an active optical area between the top device and bottom device surfaces, the bottom device surface being attached to the substrate layer and passage of light is via the bottom device surface.

12. The semiconductor device according to claim 11, wherein the substrate layer includes a light transmissible substrate.